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CHENNAI



Circuit Simulation Project

<https://esim.fossee.in/circuit-simulation-project>

Name of Participant: Abhimanyu Pundir

Project Guide: Dr. Maheshwari. R

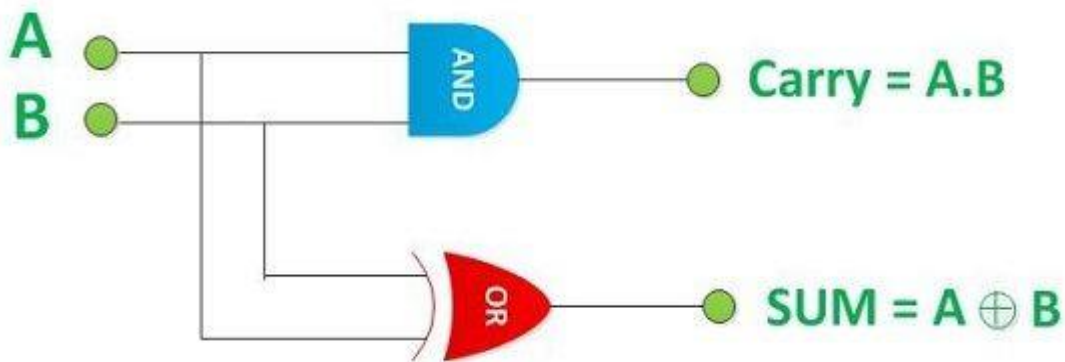
Project Name: Design of Half Adder using NAND gates

Theory :-

Half Adder is the digital circuit which can generate the result of the addition of two 1-bit numbers. It consists of two input terminal through which 1-bit numbers can be given for processing. After this, the half adder generates the sum of the numbers and carry if present.

Half Adder Circuit:-

The circuit of half adder can be designed with the help of basic building blocks of digital electronics realm i.e. logic gates. Half adder can also be designed with the help of universal gates.



Logic Circuit Of Half Adder

Half Adder Truth table:-

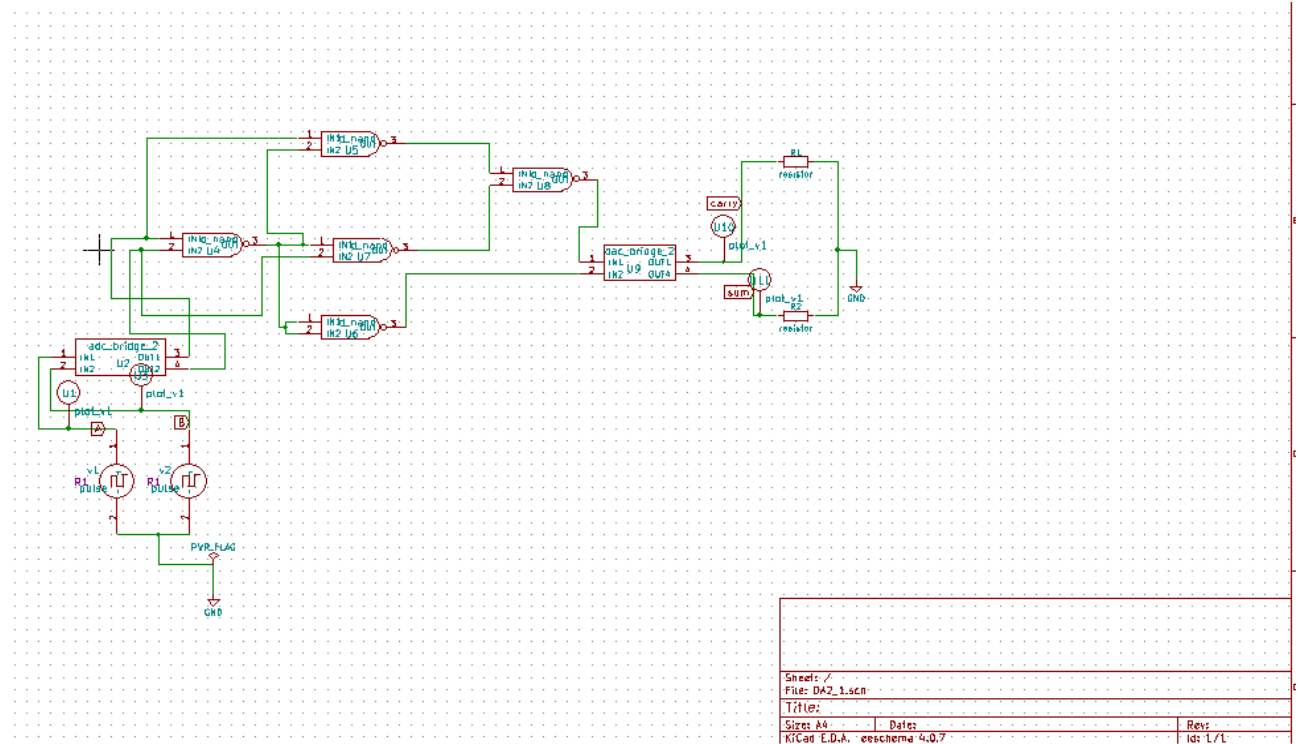
The truth table of any digital circuit is significant to understand its operations. The truth table consists of all possible combination of input that can be given to the digital circuit and all the resulting outputs.

INPUTS		OUTPUTS	
A	B	Sum(S)	Carry(C)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

The NAND operation can be understood more clearly with the help of equation given below. These equations are written in the form of operation performed by NAND gates.

$$\text{SUM, } S = \overline{\overline{A \cdot B}} \cdot \overline{\overline{B \cdot A}}$$
$$\text{SUM, } S = A\bar{B} + \bar{A}B$$
$$\text{Carry, } C = AB = \overline{\overline{AB}}$$

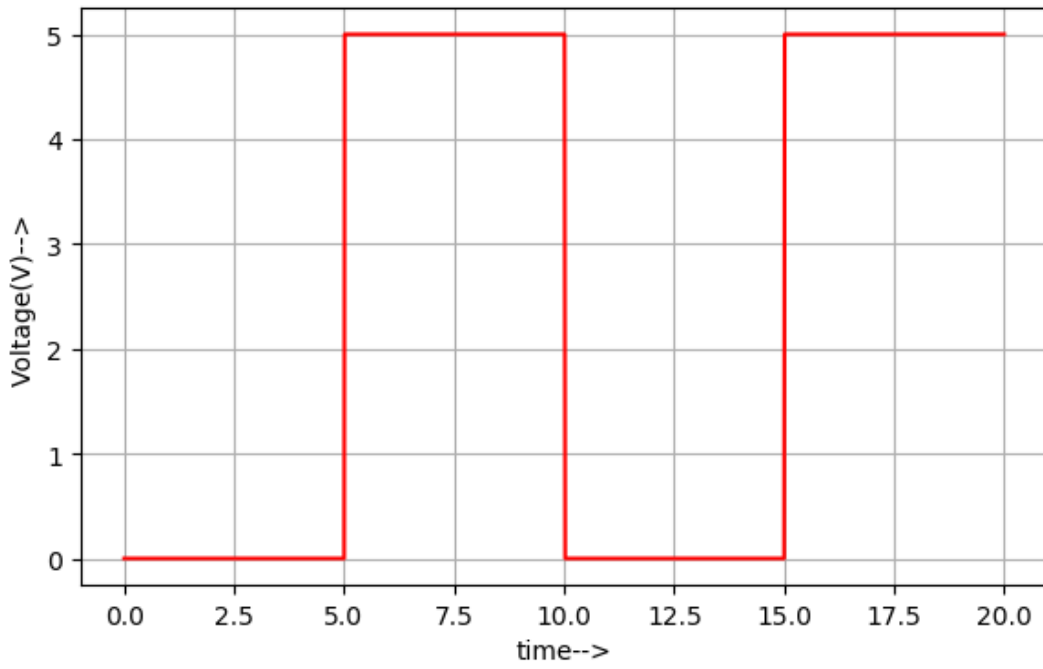
Circuit Diagram:-



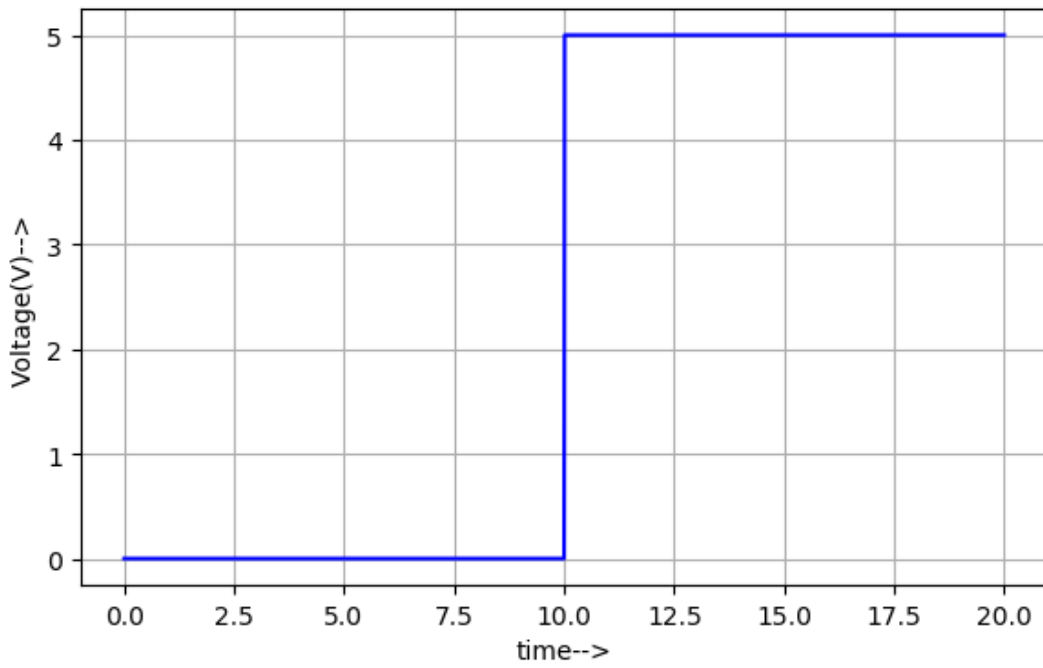
Python Plots:-

Inputs :-

A

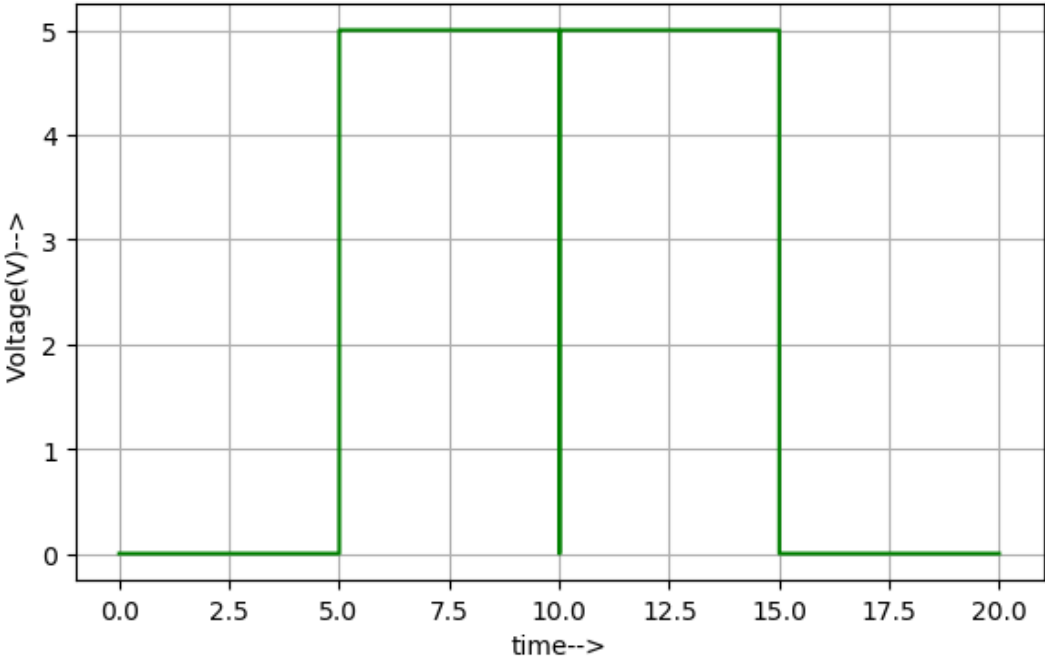


B

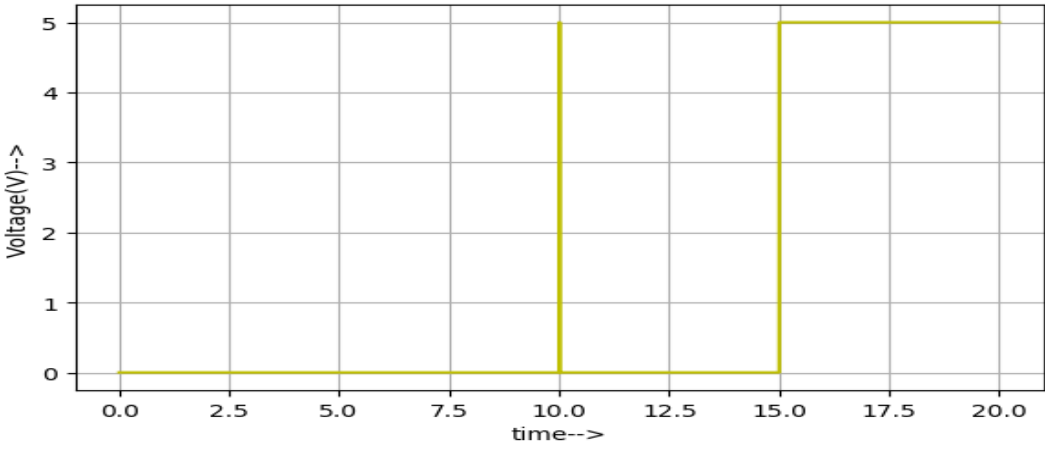


Outputs:-

Carry :-



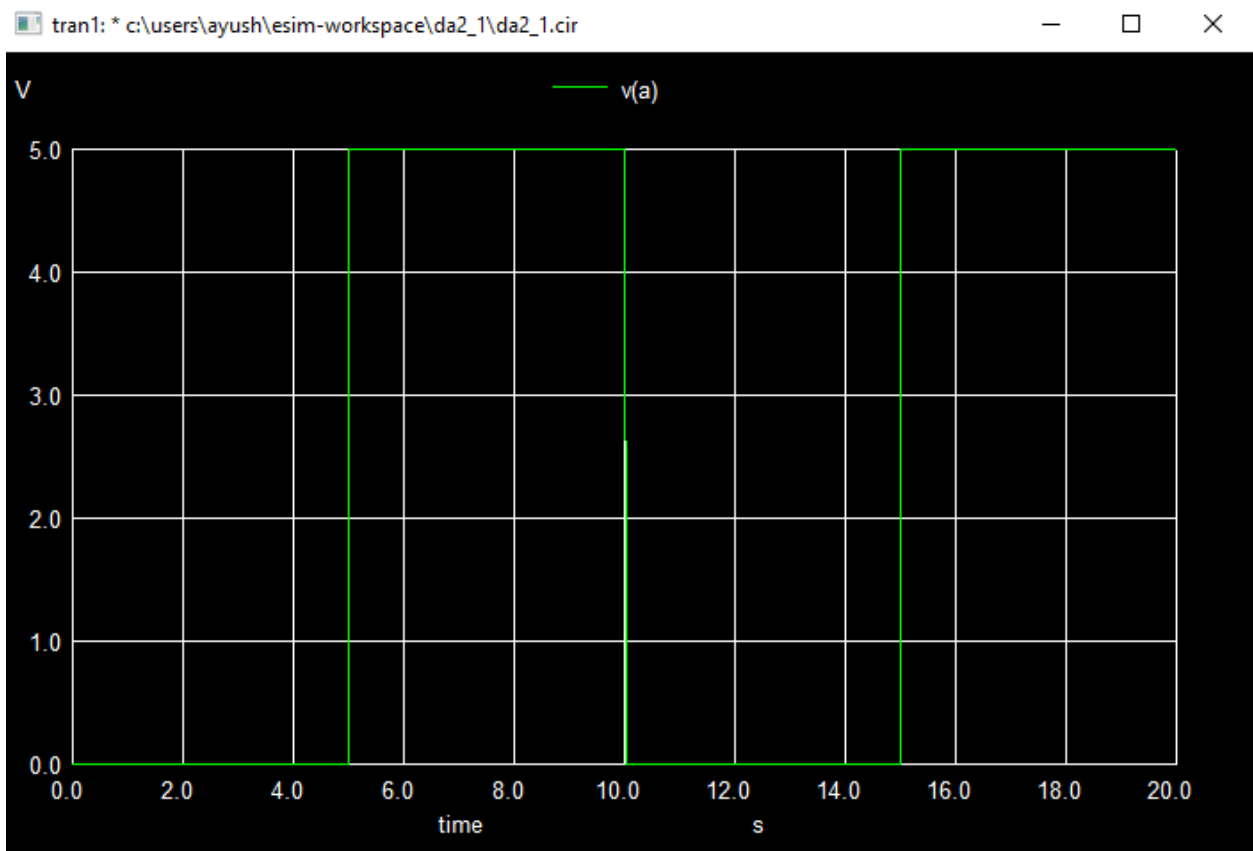
Sum:-



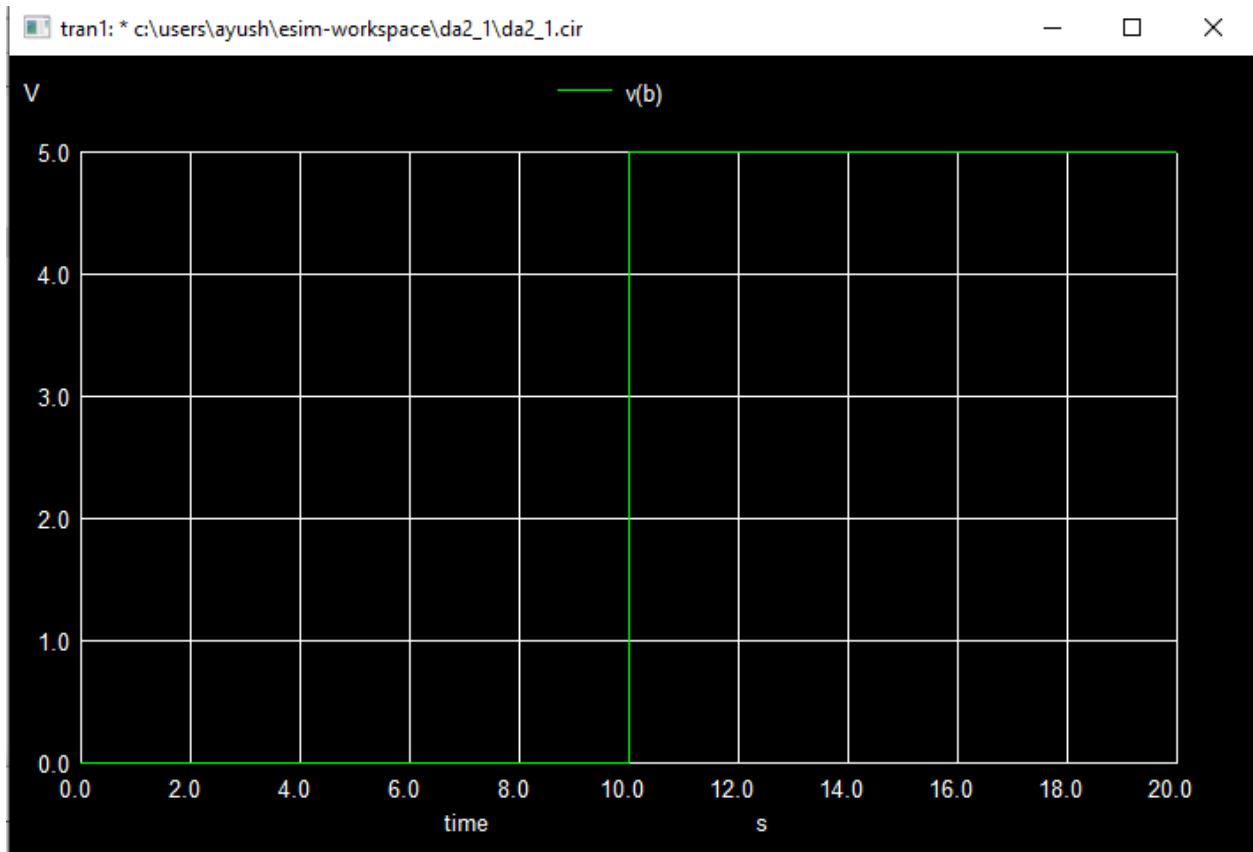
Ngspice Plots:-

Inputs:-

A

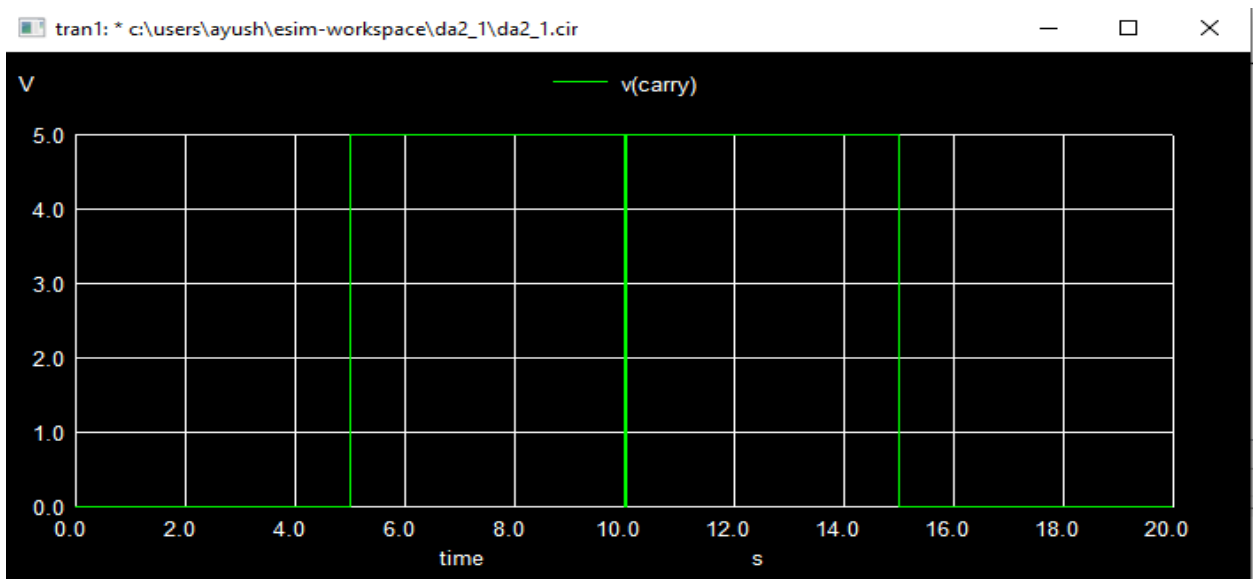


B

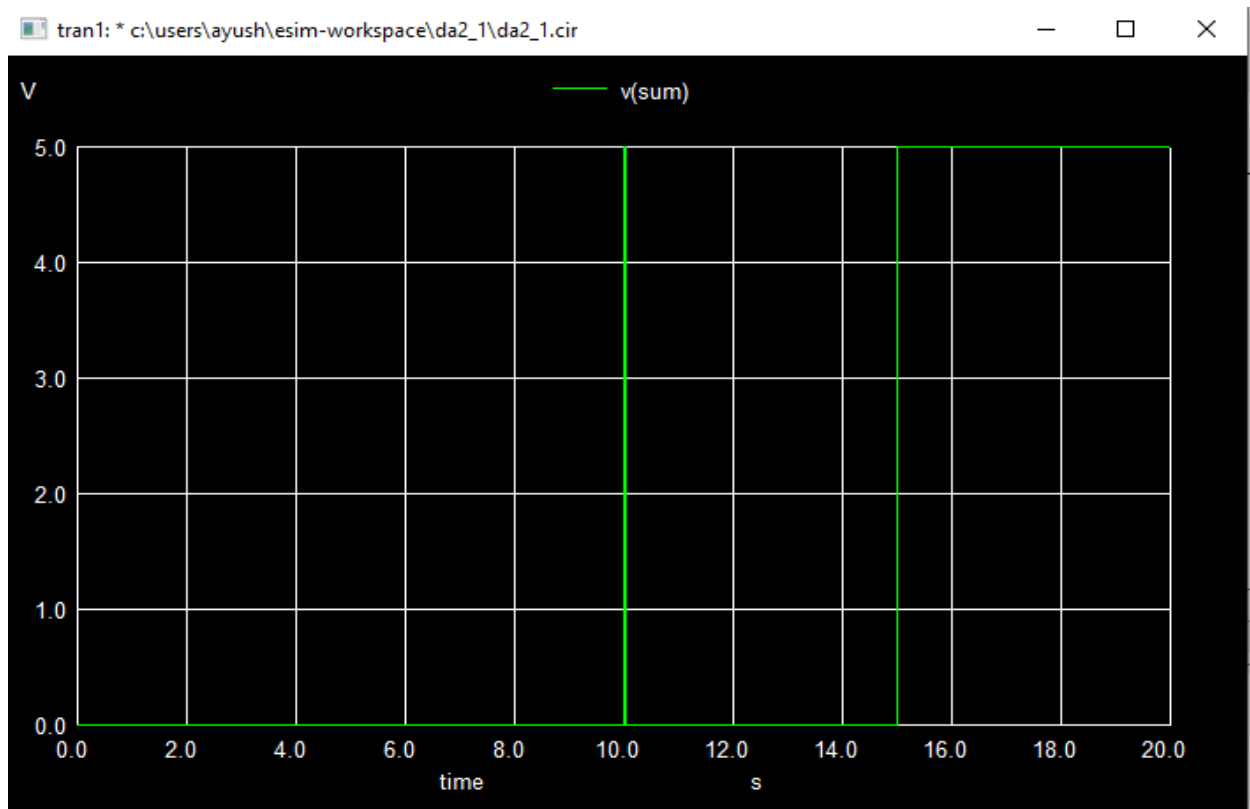


Outputs:-

Carry:-



Sum:-



References:-

- <https://electronicscoach.com/half-adder.html>
- <https://de-iitr.vlabs.ac.in/exp/half-full-adder/theory.html>
- <https://www.geeksforgeeks.org/half-adder-half-subtractor-using-nand-nor-gates/>
- <https://www.gatevidyalay.com/tag/half-adder-using-only-nand-gates/>