Circuit Simulation Project

https://esim.fossee.in/circuit-simulation-project

Name of the participant : Siddharth Bhuthapuri

Project Guide: Dr. R. Maheswari

Title of the circuit : Design Of 8 to 1 Multiplexer with enable

Theory/Description : A multiplexer is a device that has 2^n Input Lines and one output line were n= number of input selector line. At a time only one Input Line will connect to the output line.An 8-to-1 multiplexer consists of eight data inputs D0 through D7, three input select lines S0 through S2 and a single output line Y. Depending on the select lines combinations, multiplexer selects the inputs. Since the number data bits given to the MUX are eight, then 3 bits (2^3 = 8) are needed to select one of the eight data bits.

Truth Table:

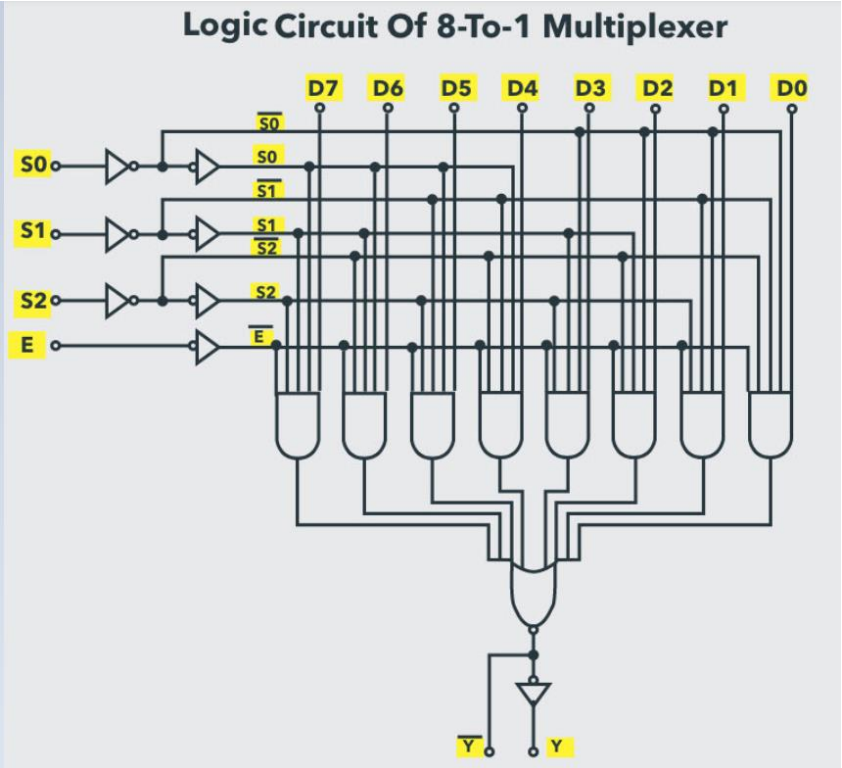
Select Lines			Input								Output
S0	S1	S2	D0	D1	D2	D3	D4	D5	D6	D7	Y
0	0	0	0	X	X	X	X	X	X	X	0
0	0	0	1	X	X	X	X	X	X	X	1
0	0	1	X	0	X	X	X	X	X	X	0
0	0	1	X	1	X	X	X	X	X	X	1
0	1	0	X	X	0	X	X	X	X	X	0
0	1	0	X	X	1	X	X	X	X	X	1
0	1	1	X	X	X	0	X	X	X	X	0
0	1	1	X	X	X	1	X	X	X	X	1
1	0	0	X	X	X	X	0	X	X	X	0
1	0	0	X	X	X	X	1	X	X	X	1
1	0	1	X	X	X	X	X	0	X	X	0
1	0	1	X	X	X	X	X	1	X	X	1
1	1	0	X	X	X	X	X	X	0	X	0
1	1	0	X	X	X	X	X	X	1	X	1
1	1	1	X	X	X	X	X	X	X	0	0
1	1	1	X	X	X	X	X	X	X	1	1

From the above truth table, the Boolean equation for the output is given as:

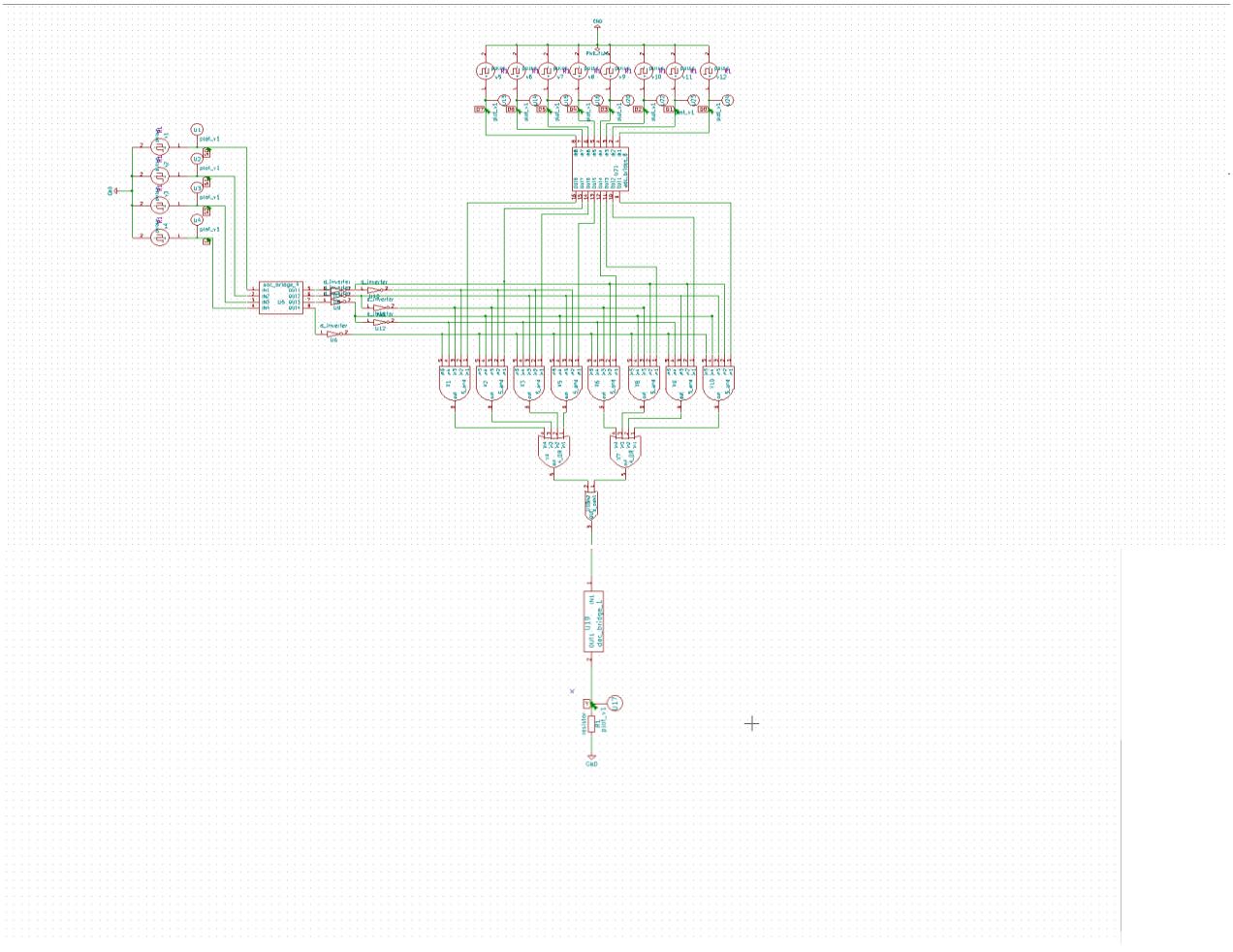
$$Y = \overline{S0}\,\overline{S1}\,\overline{S2}\,D0 + \overline{S0}\,\overline{S1}\,S2\,D1 + \overline{S0}\,S1\,\overline{S2}\,D2 + \overline{S0}\,S1\,S2\,D3 + S0\,\overline{S1}\,\overline{S2}\,D4 + S0\,\overline{S1}\,S2\,D5 + S0\,S1\,\overline{S2}\,D6 + S0\,S1\,S2\,D7$$

From the above Boolean equation, the logic circuit diagram of an 8-to-1 multiplexer can be implemented by using 8 AND gates, 1 OR gate and 7 NOT gates as shown .

Logic Circuit:



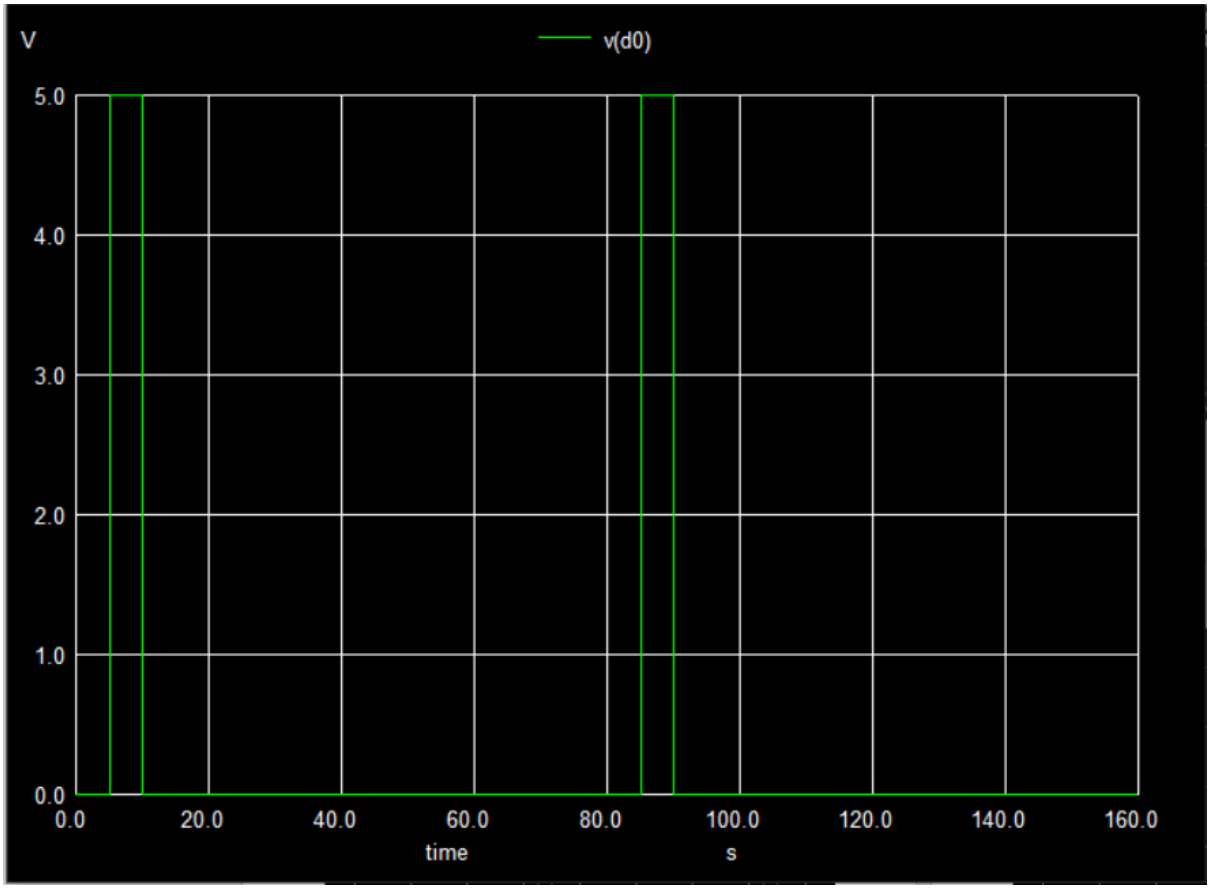
Circuit Diagram:



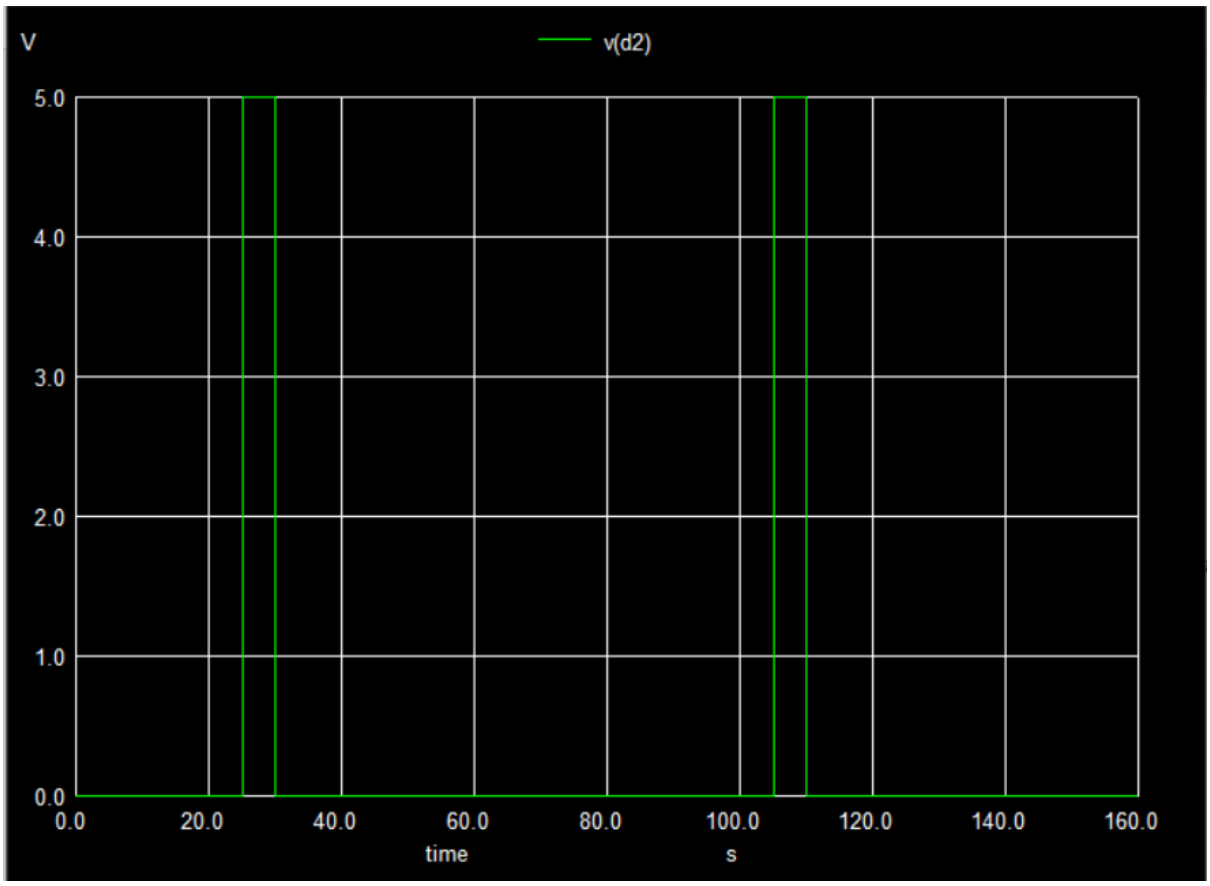
Results:

Ngspice plot-Input Waveforms:

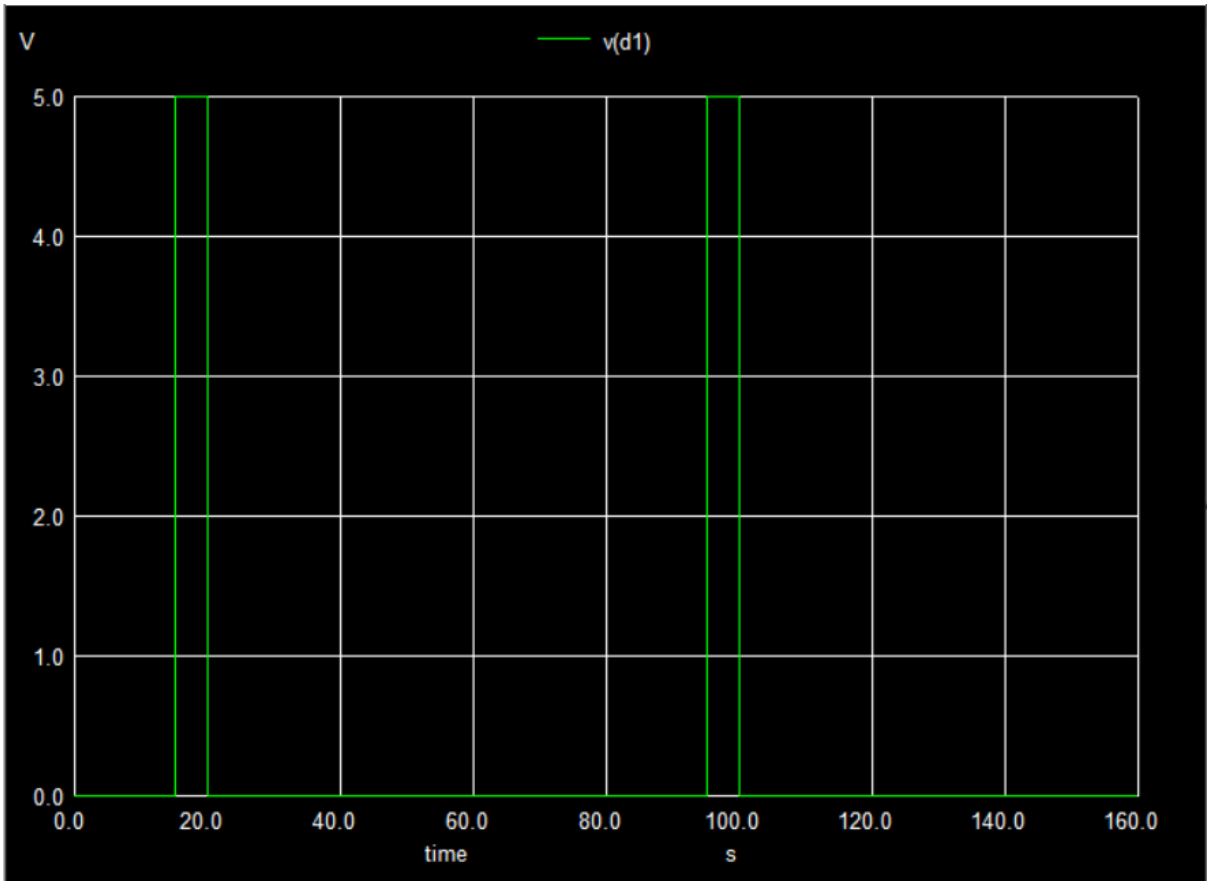
D0:



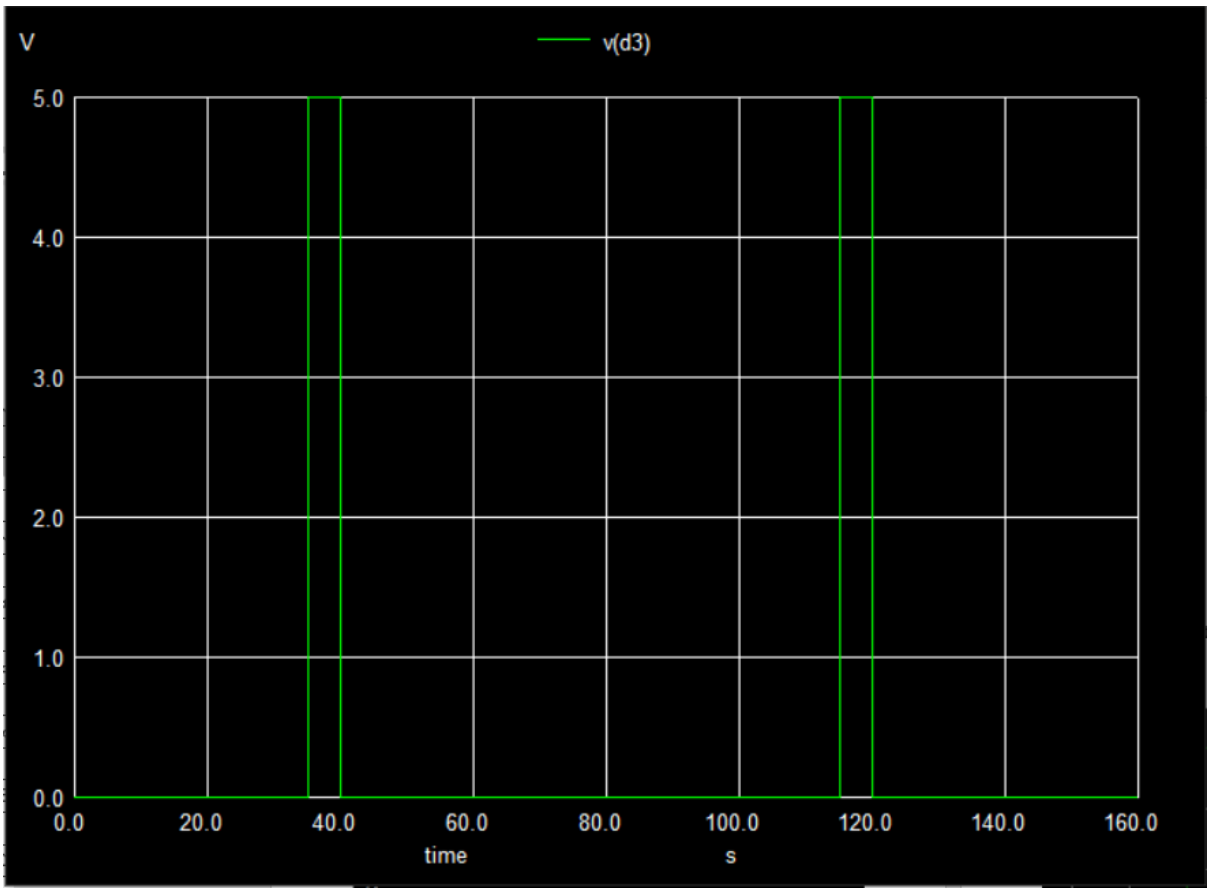
D1:


V
v(d2)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
time
s

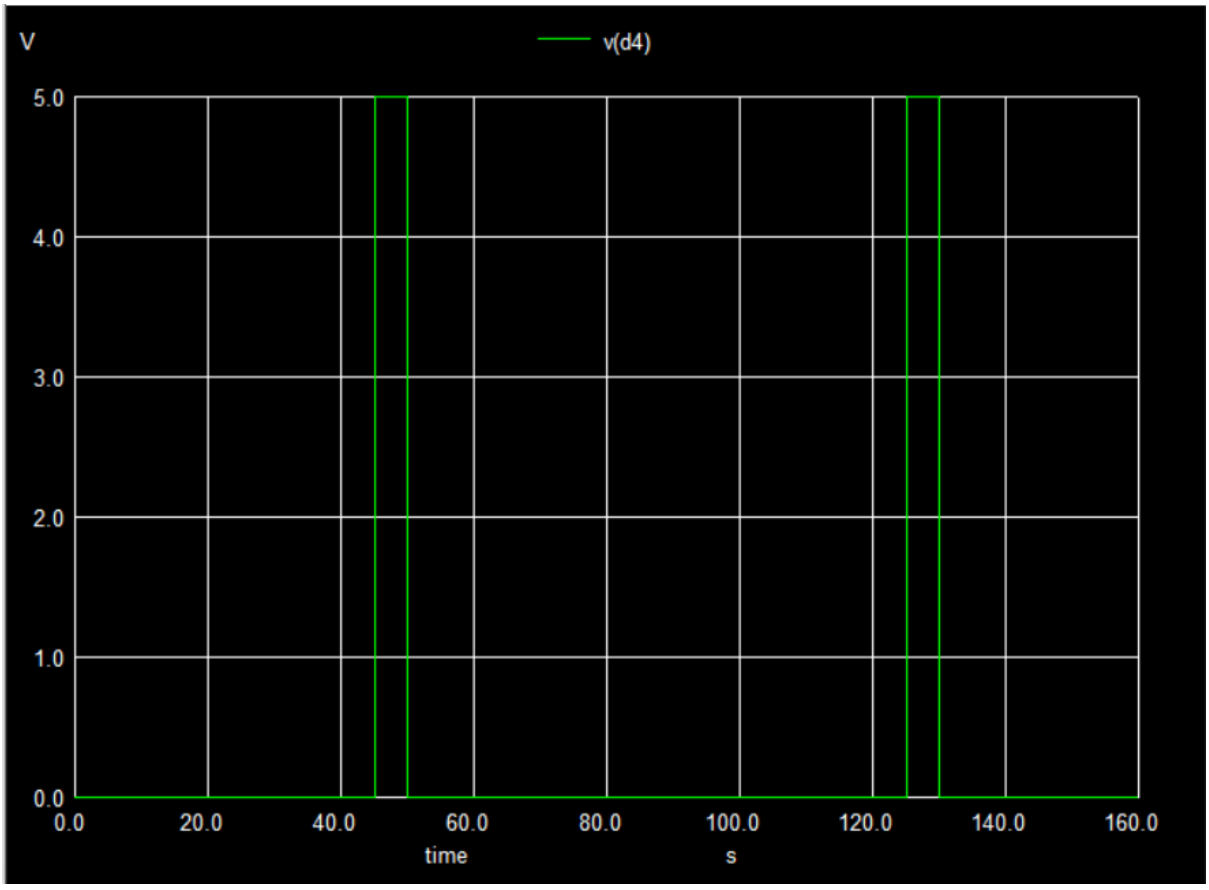
D2:


V
v(d1)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
time
s

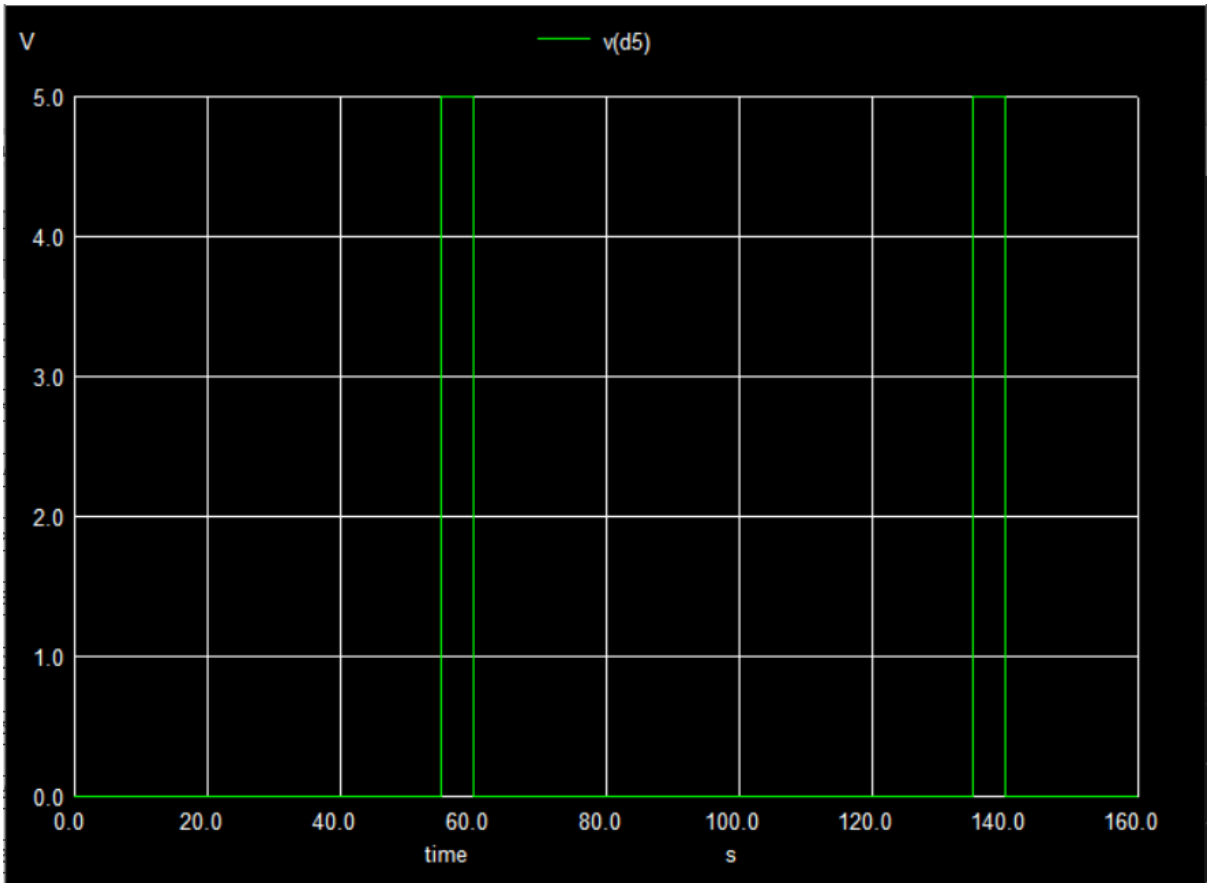
D3:


V
v(d3)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
time
s

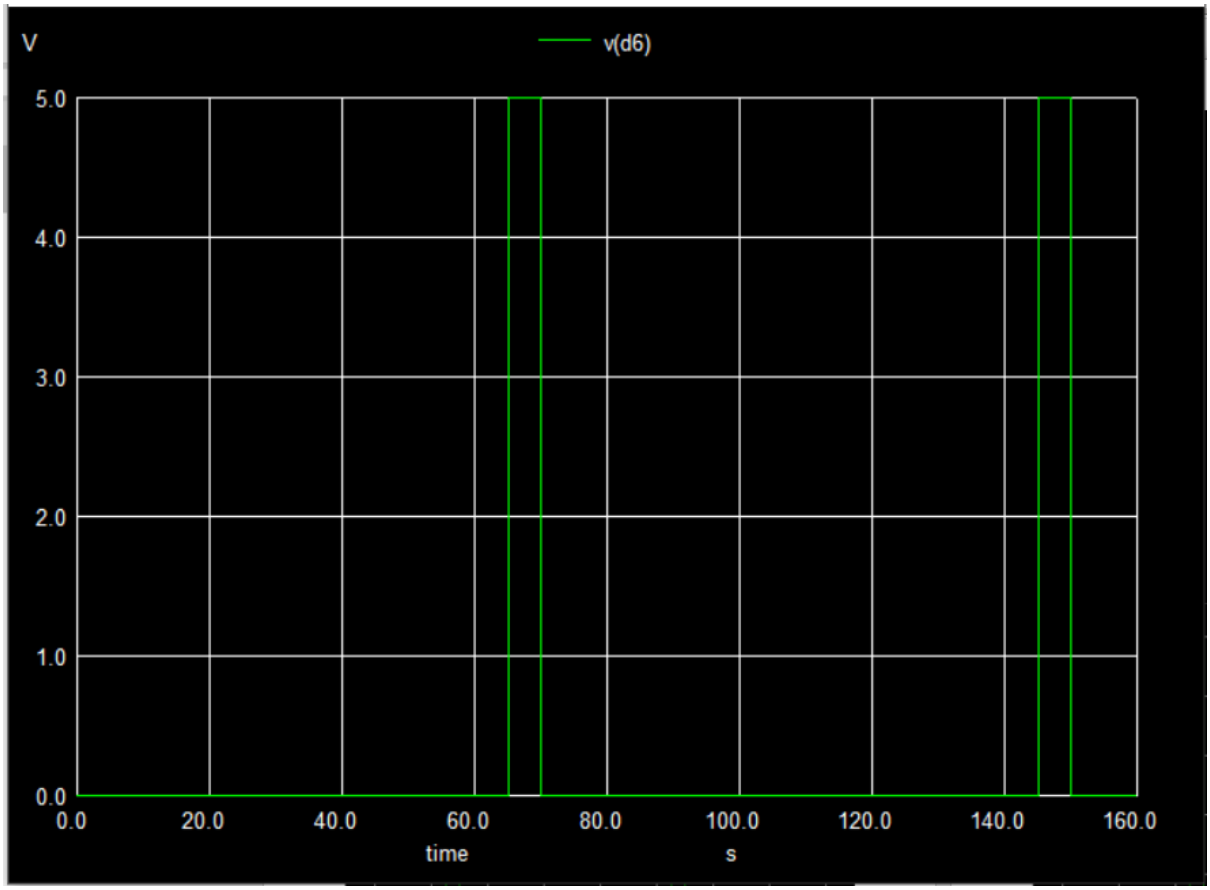
D4:


V
v(d4)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
time
s

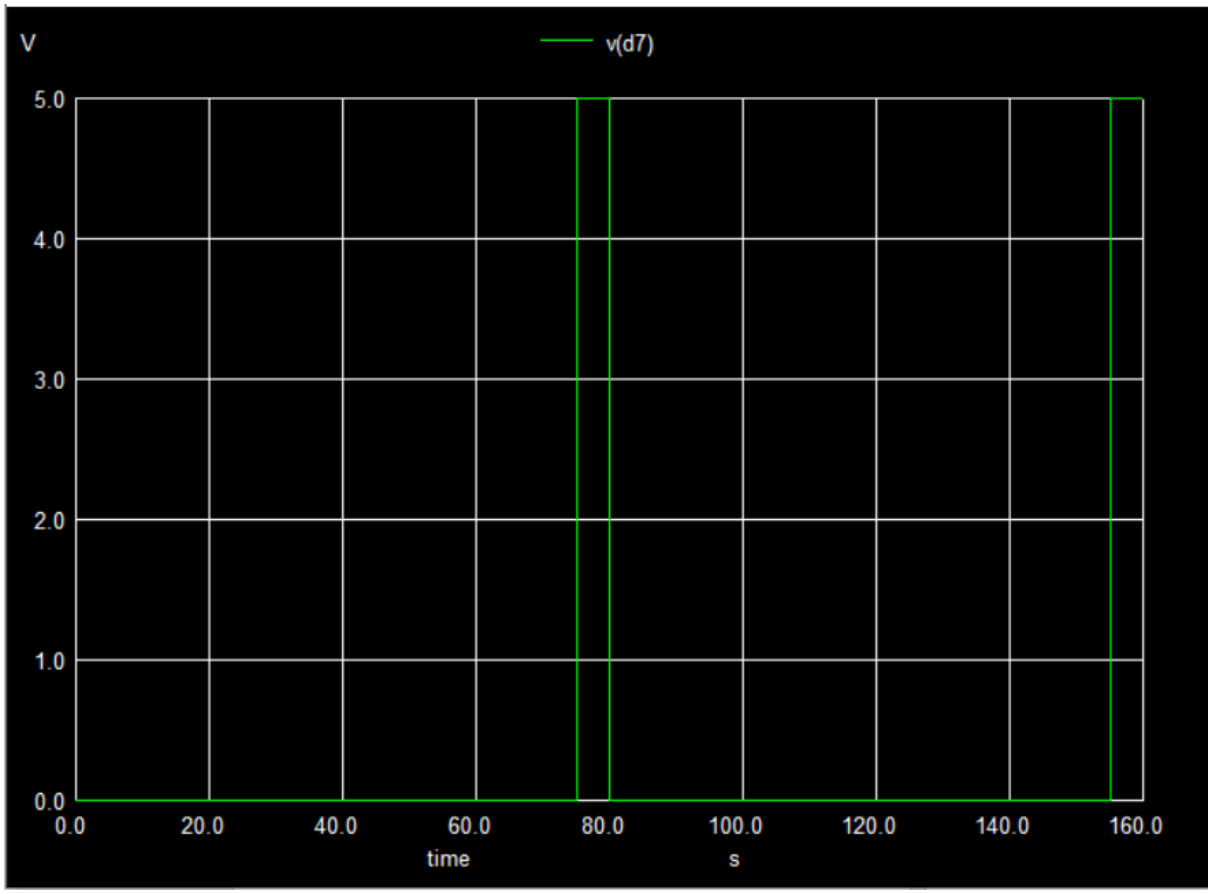
D5:


V
v(d5)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
time
s

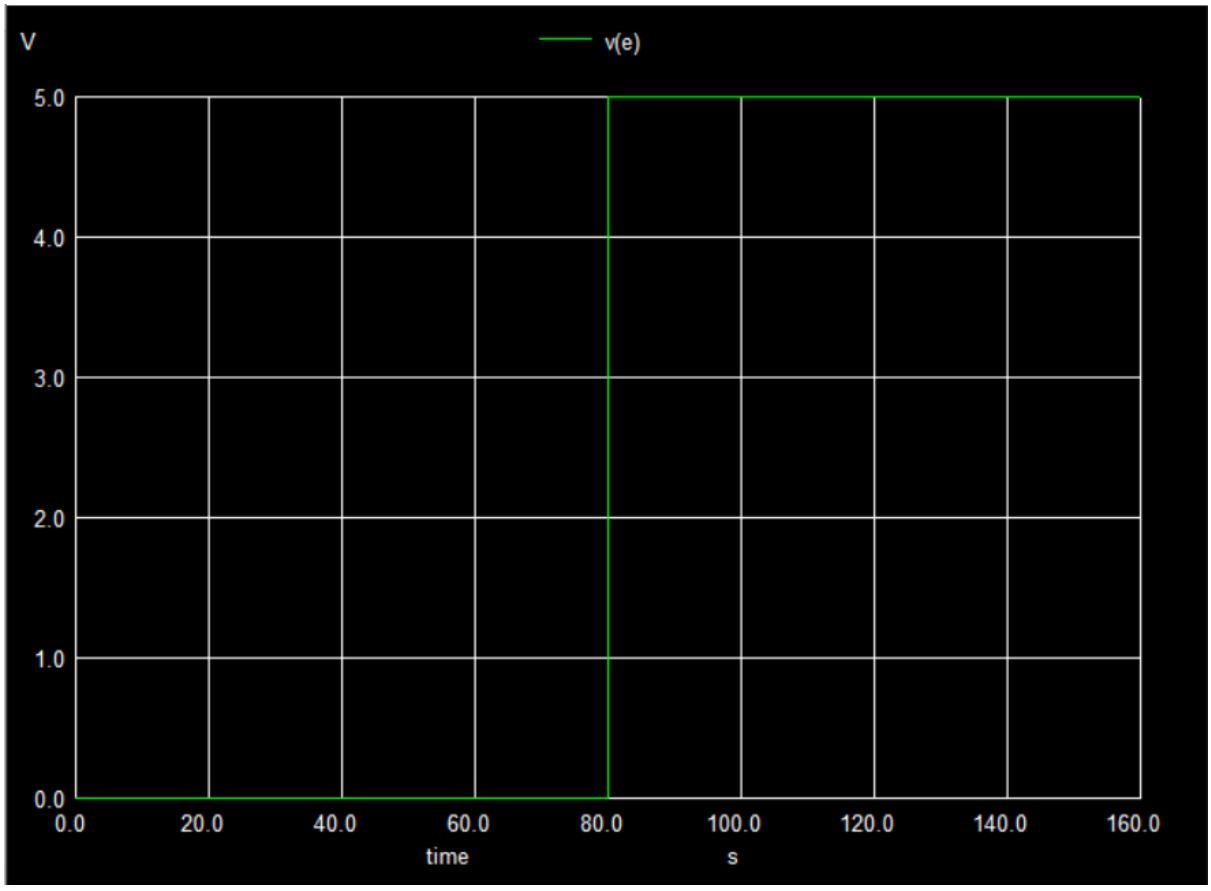
D6:


V
v(d6)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
time
s

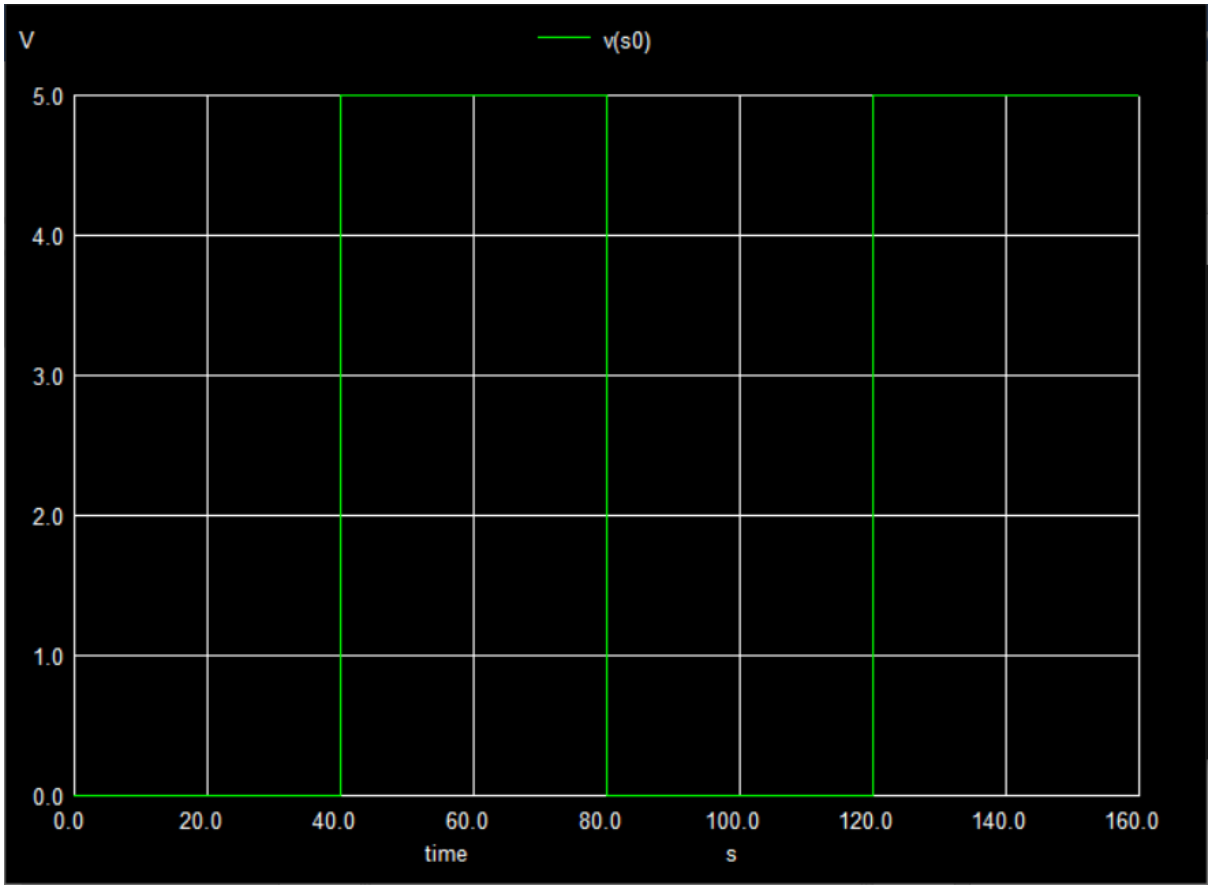
D7:


V
v(d7)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
time
s

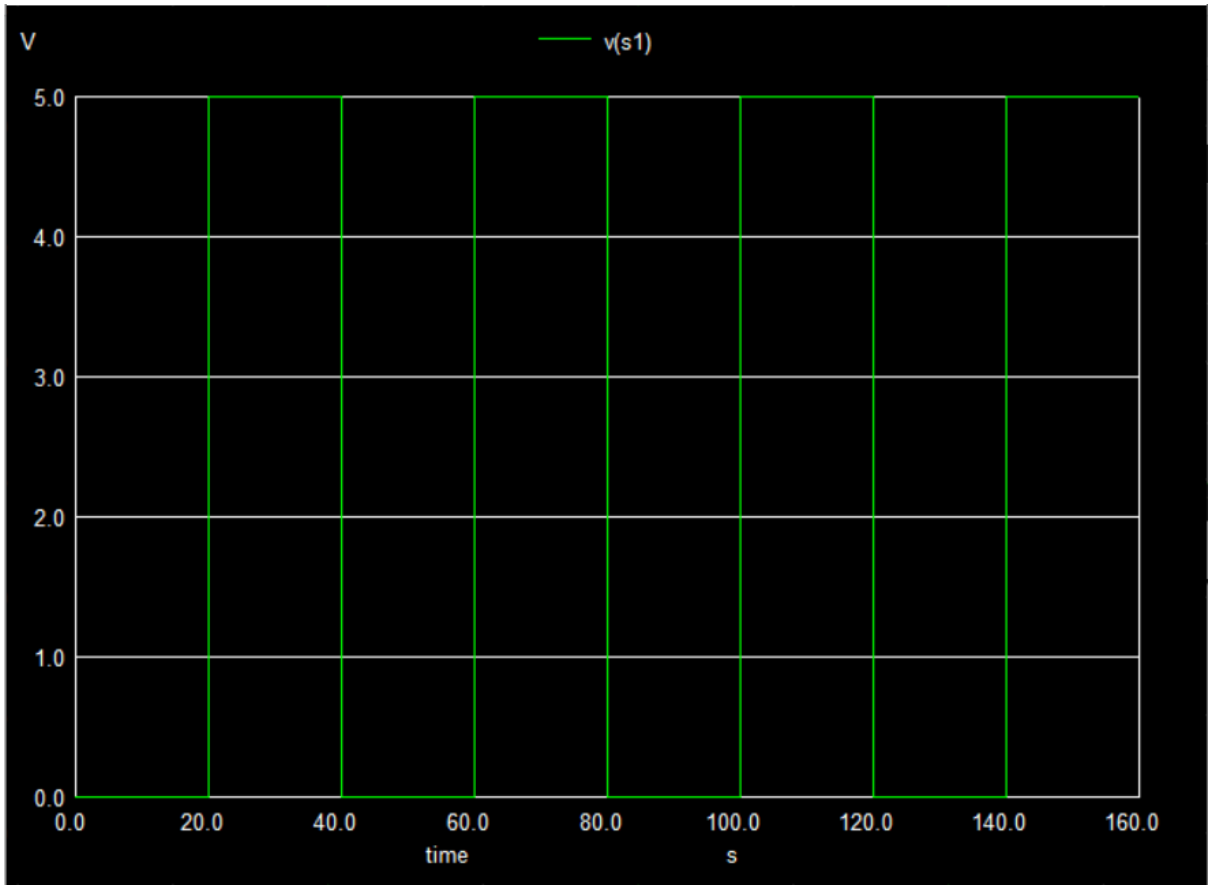
E:


V
v(e)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
time
s

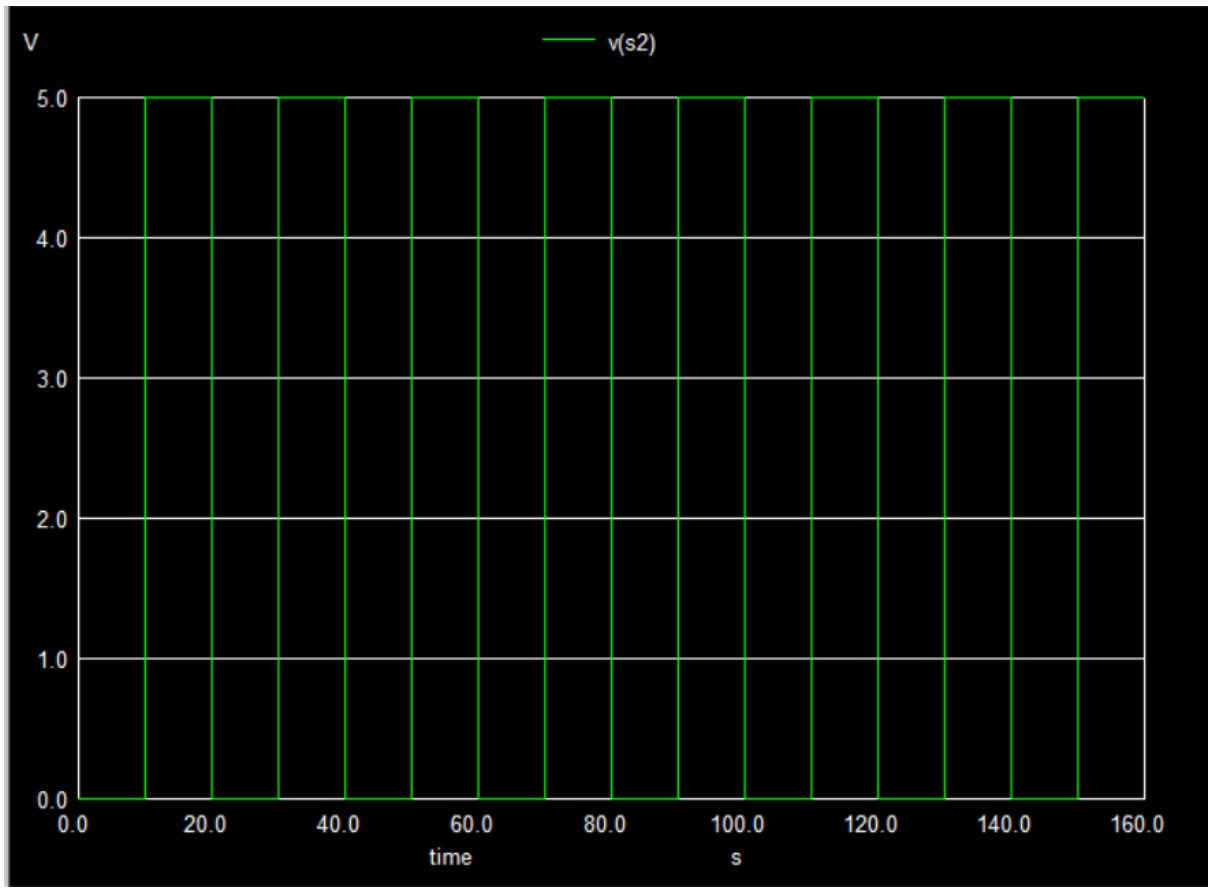
S0:


V
v(s0)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
time
s

S1:

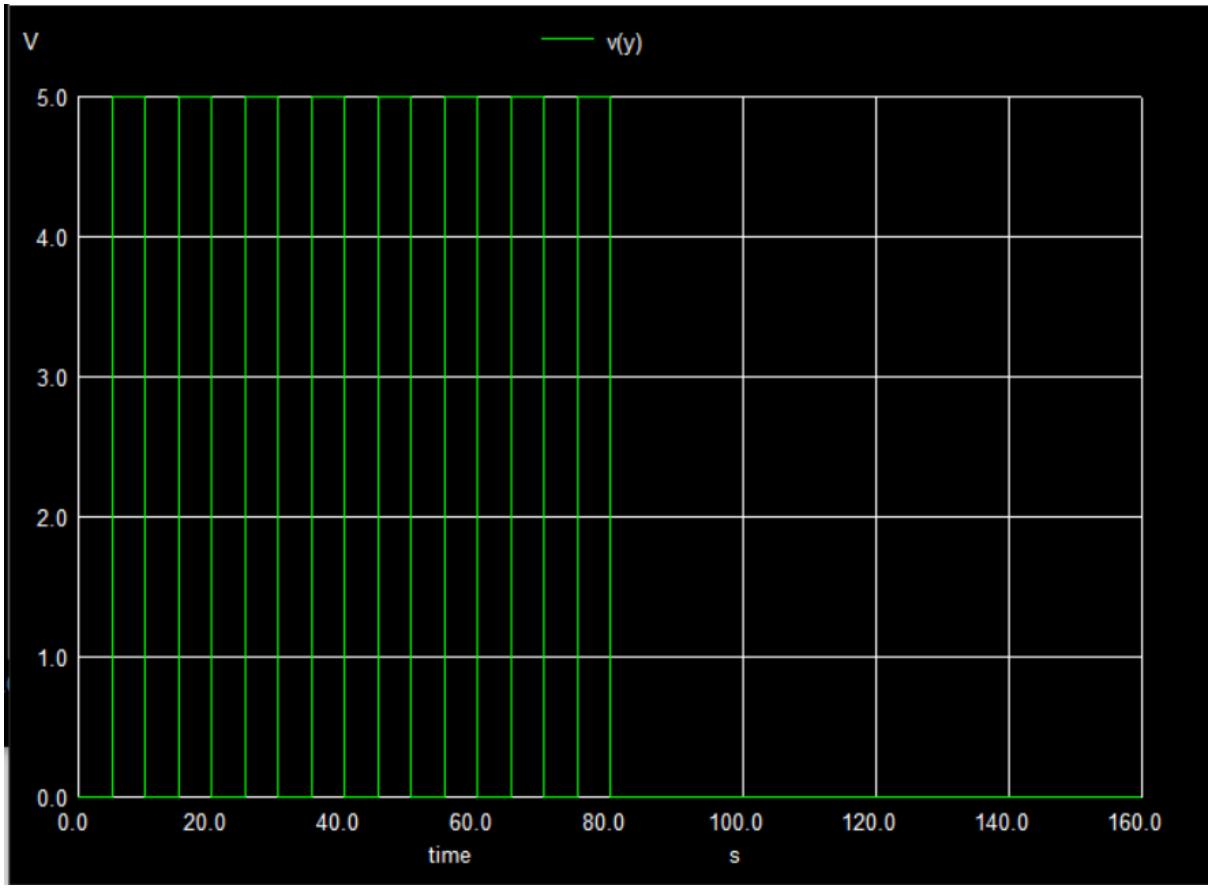

V
v(s1)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
time
s

S2:



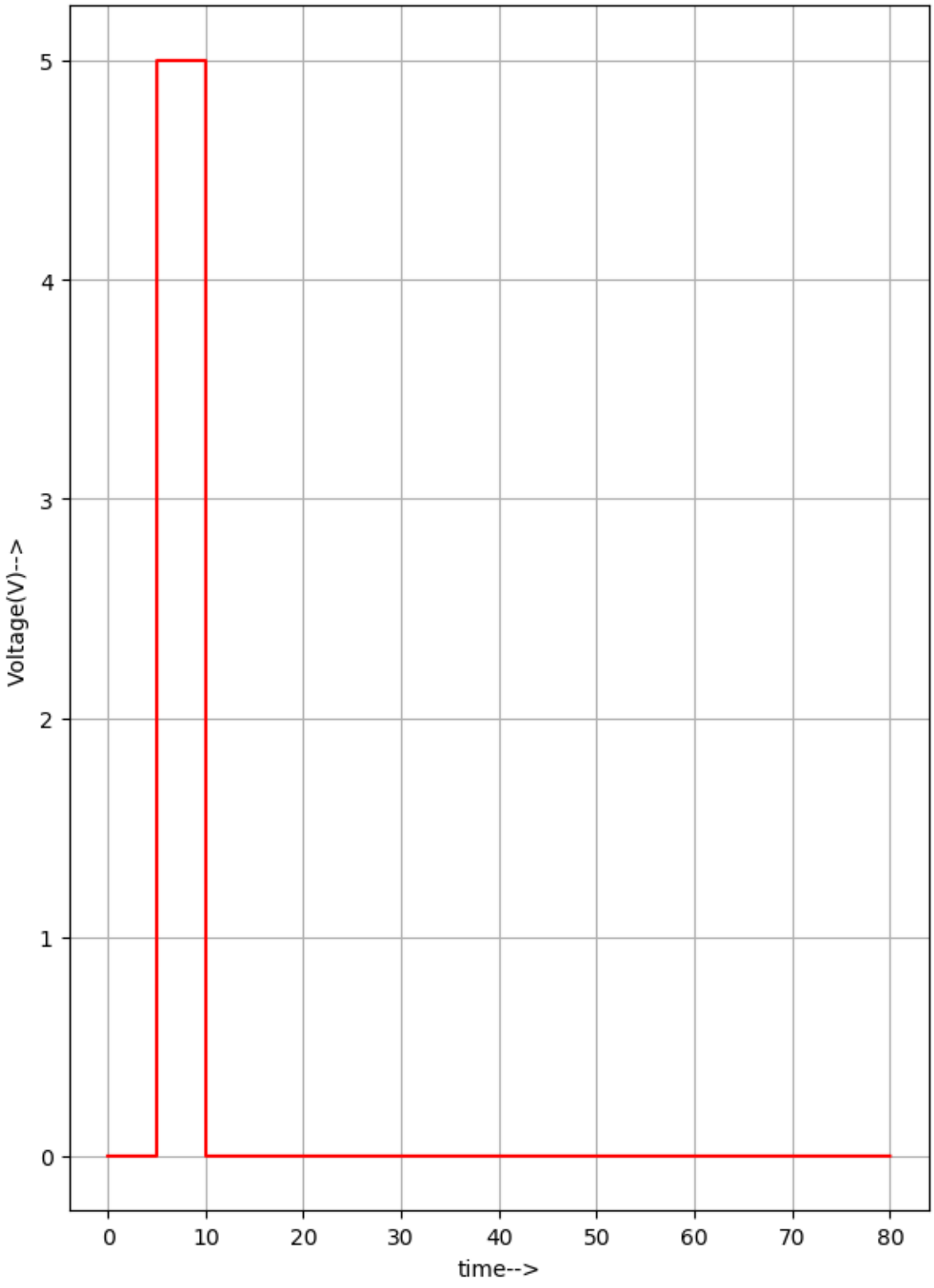
Ngspice plot-Output Waveforms:

Y:

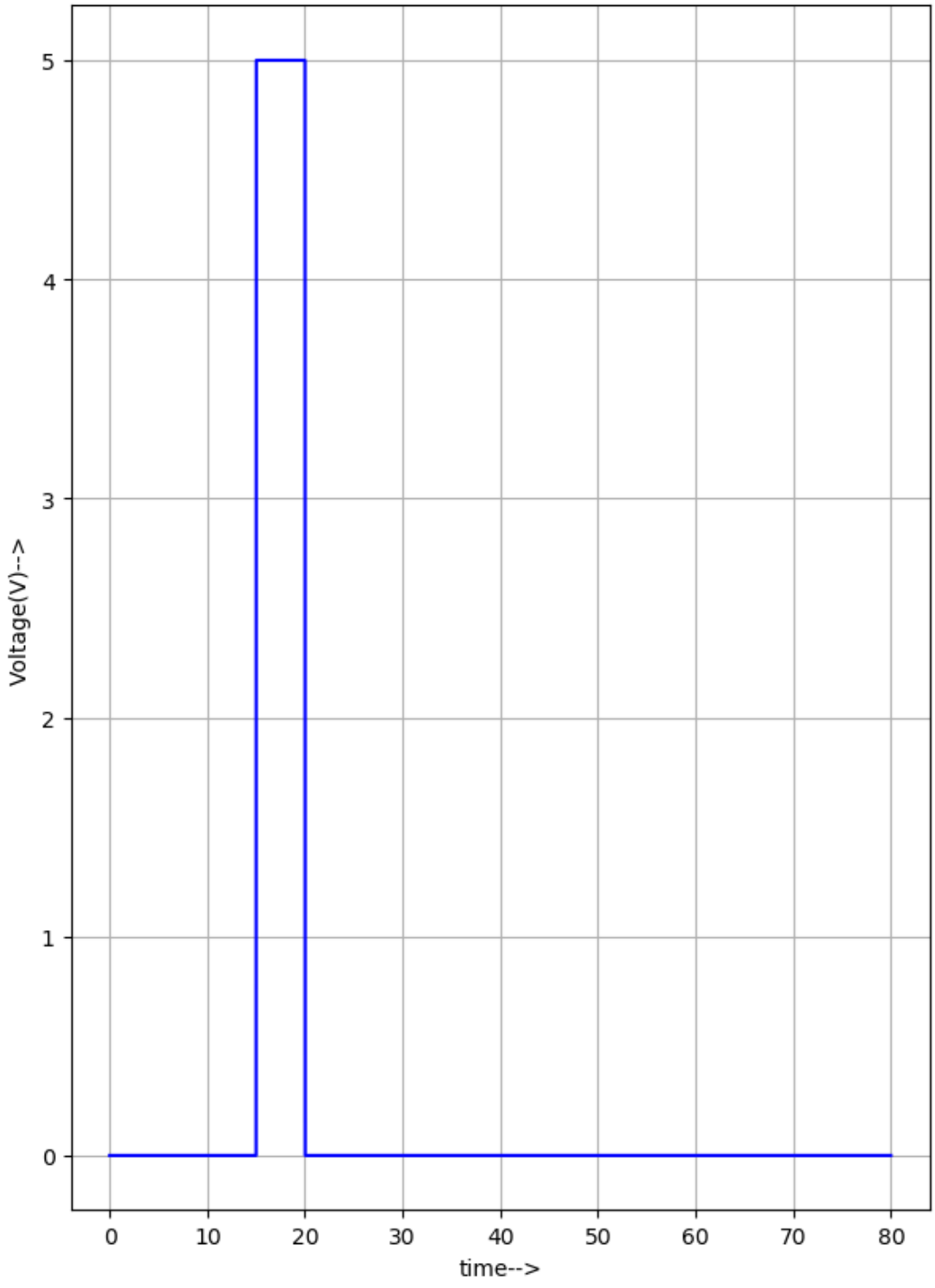


Python plot-Input Waveforms:

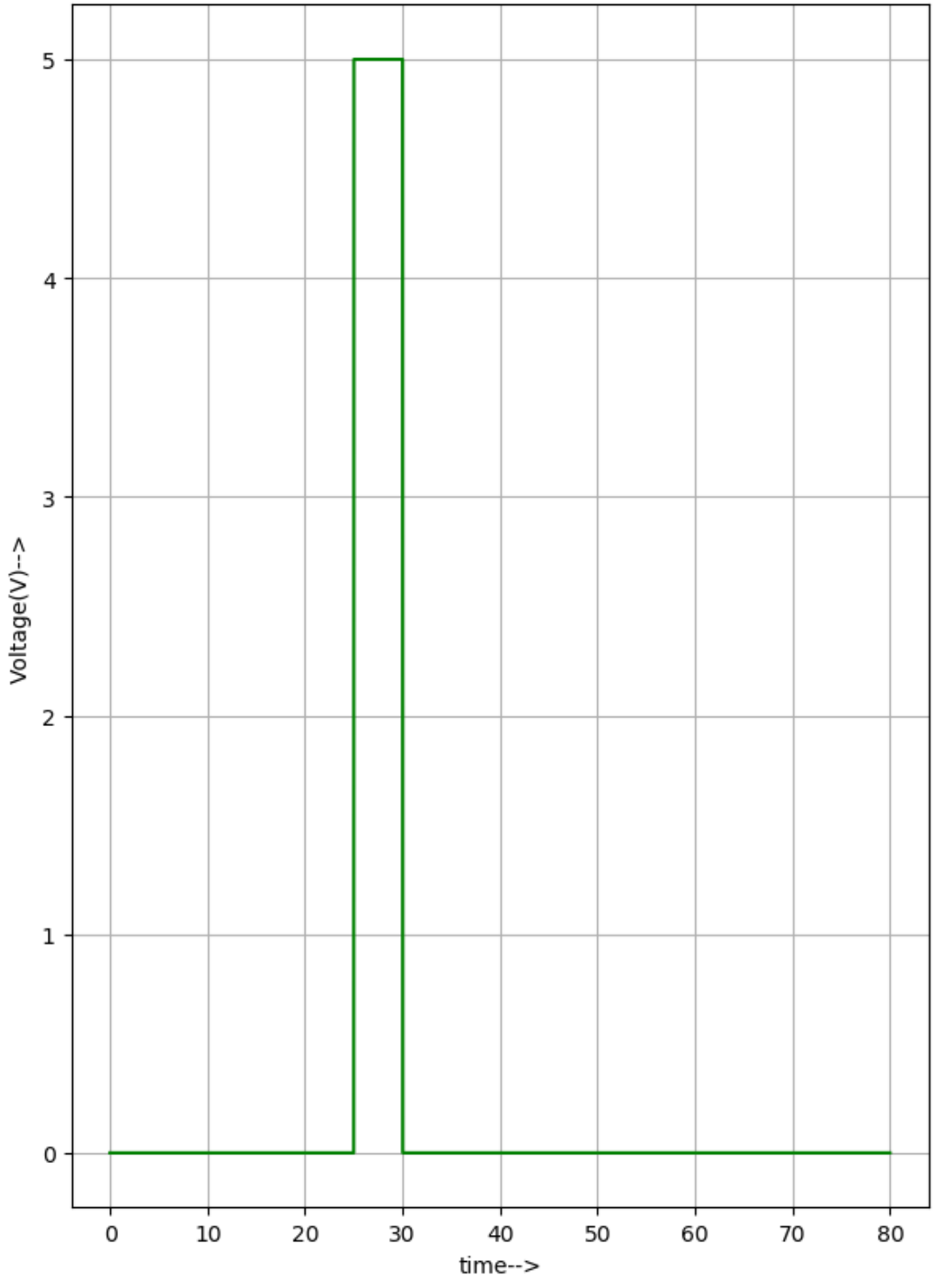
D0:



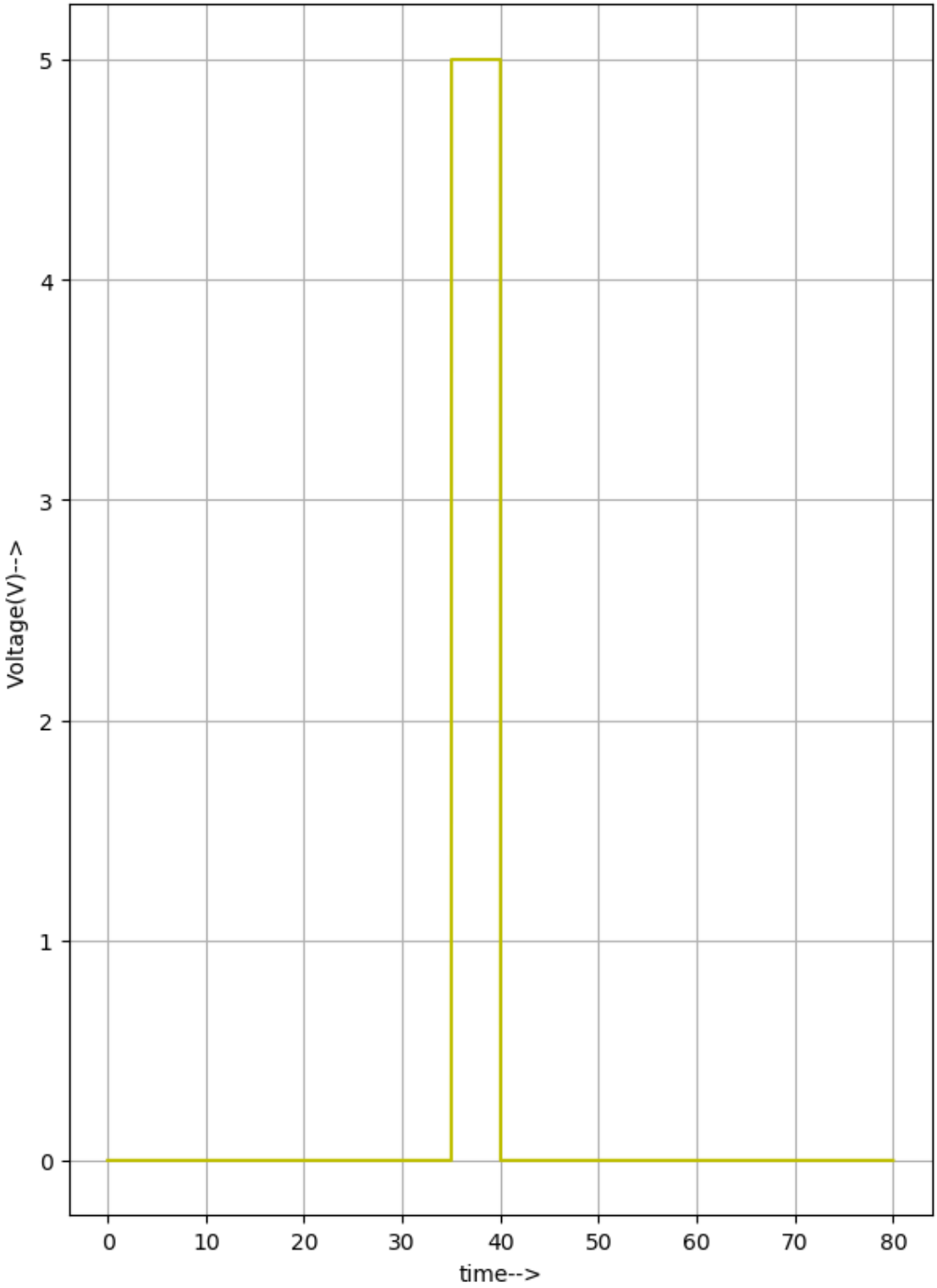
D1:



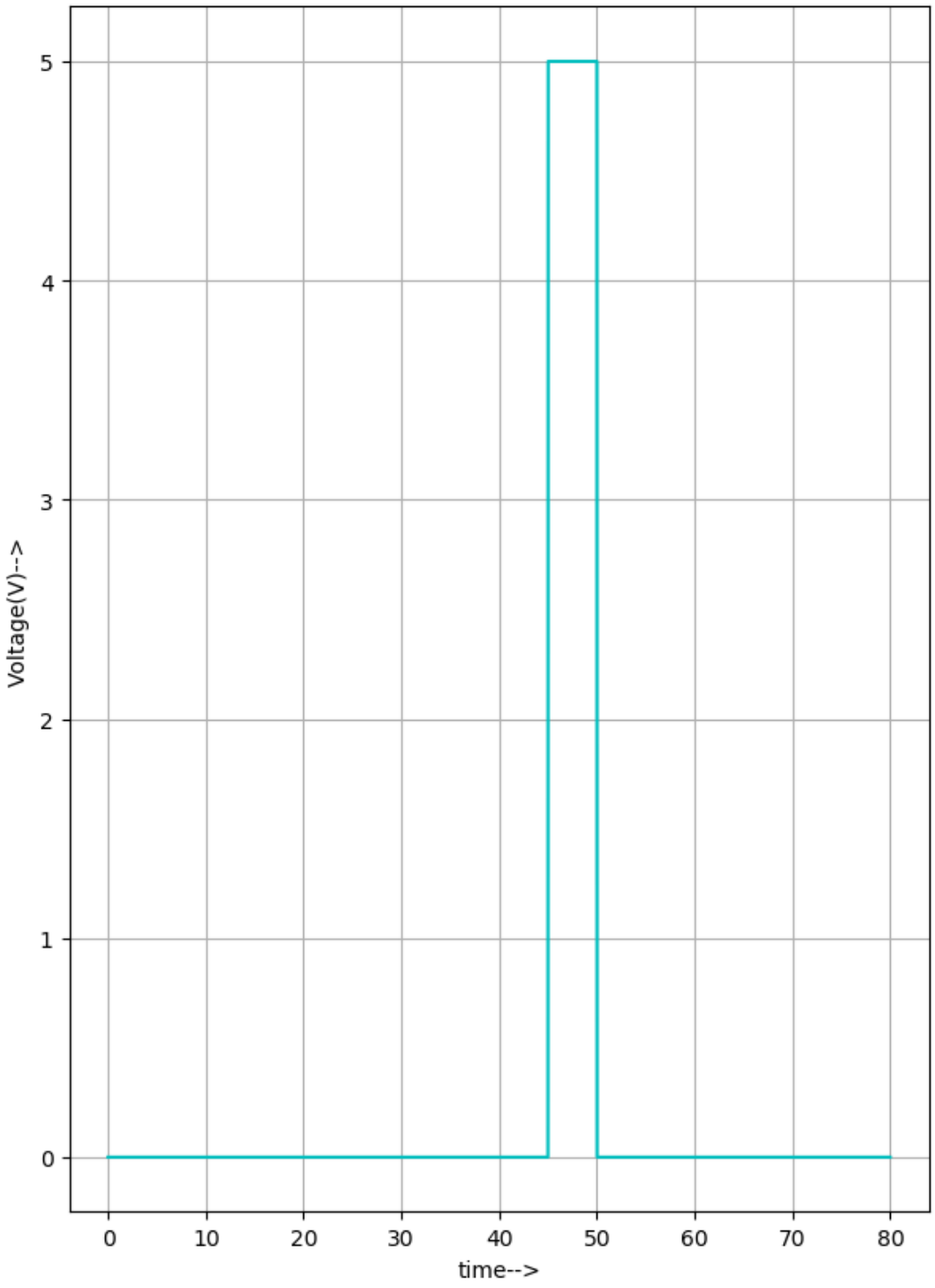
D2:



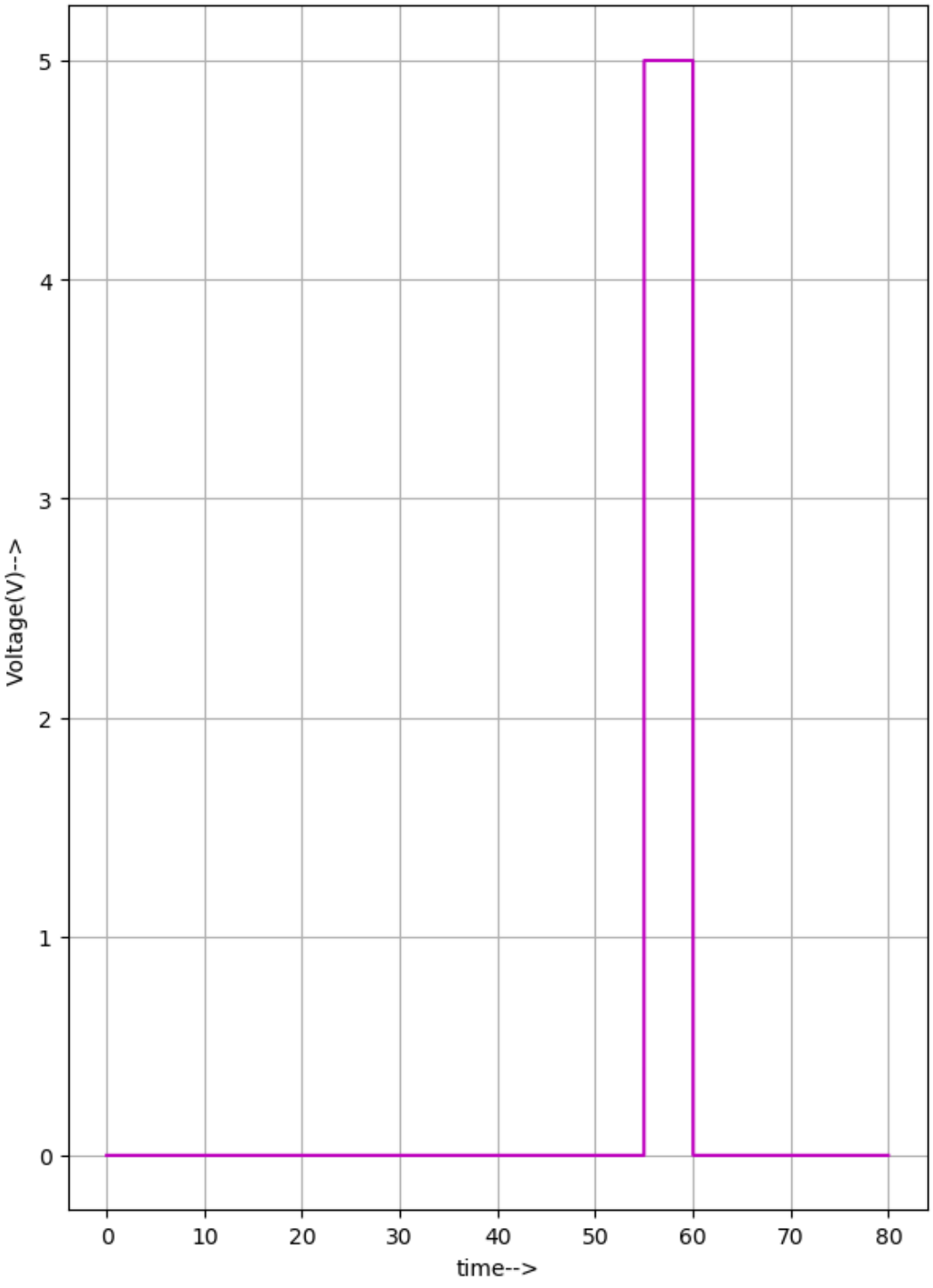
D3:



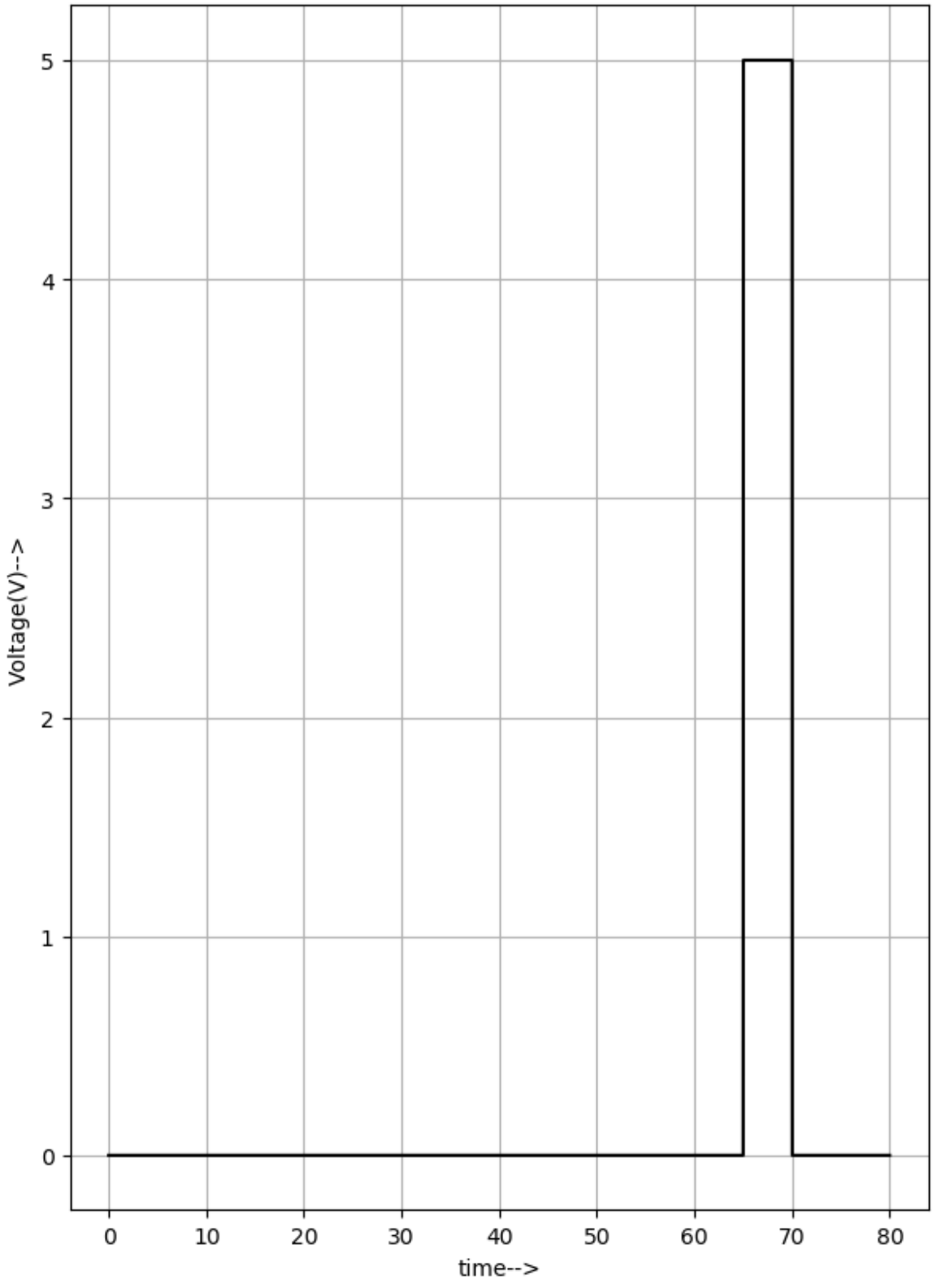
D4:



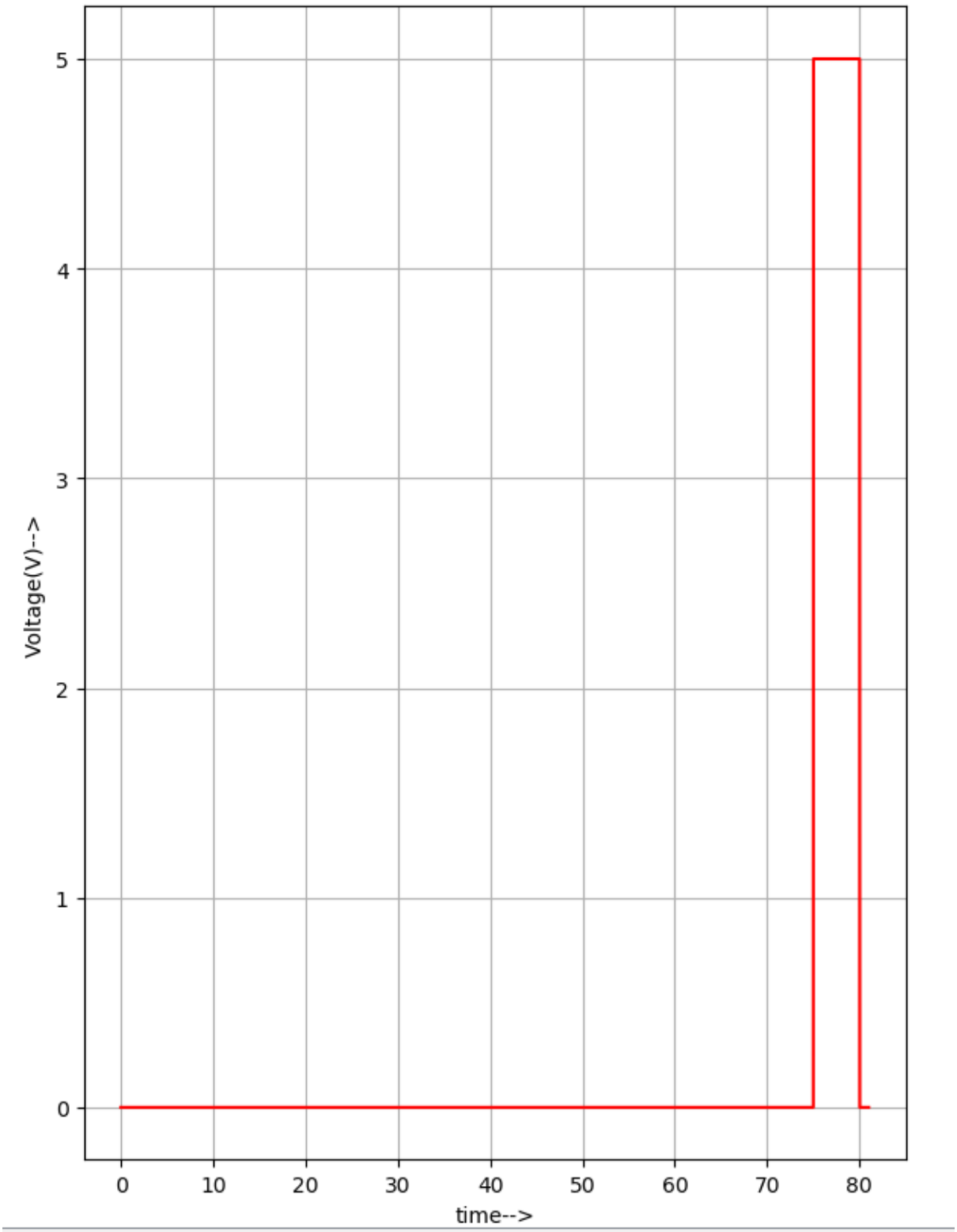
D5:



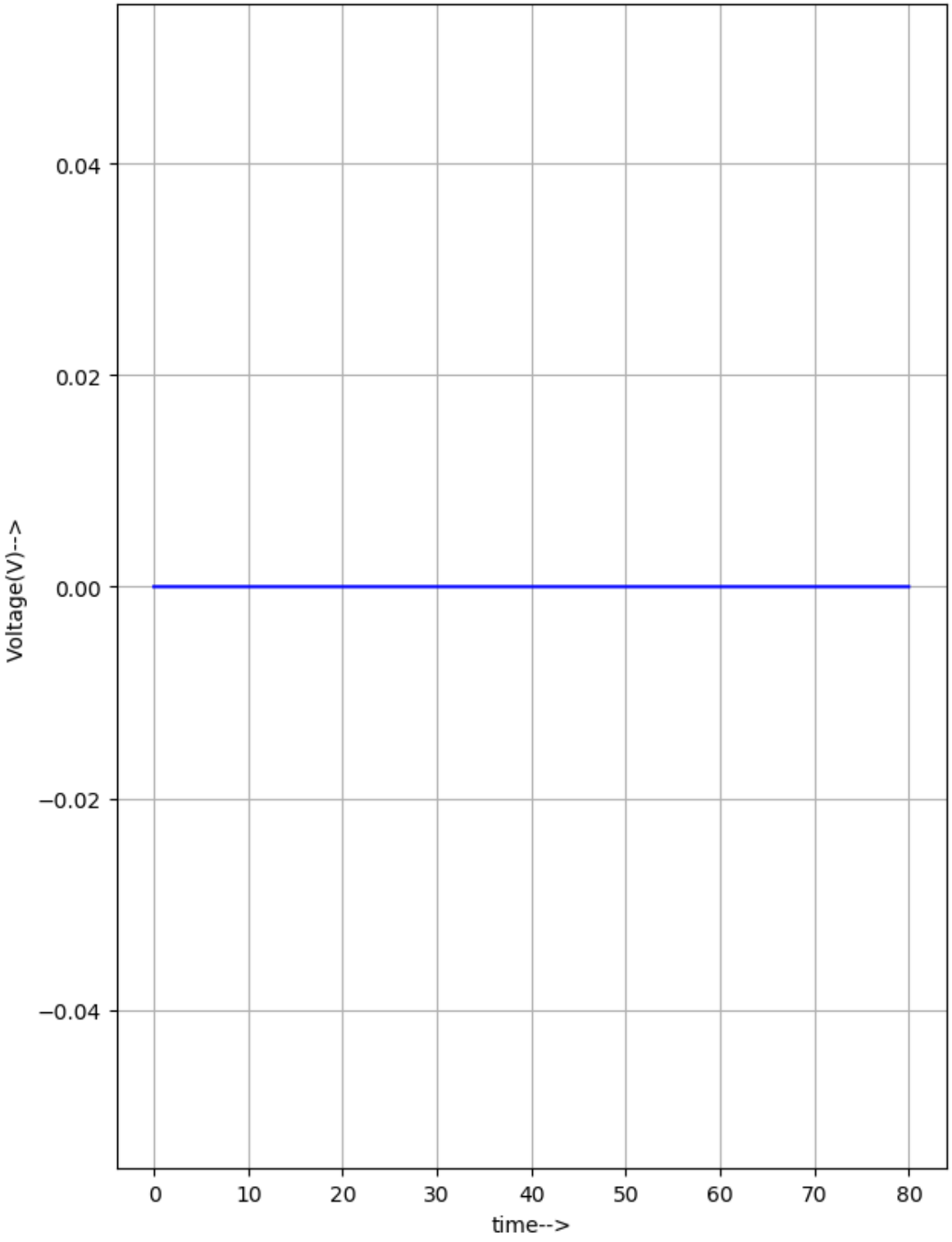
D6:



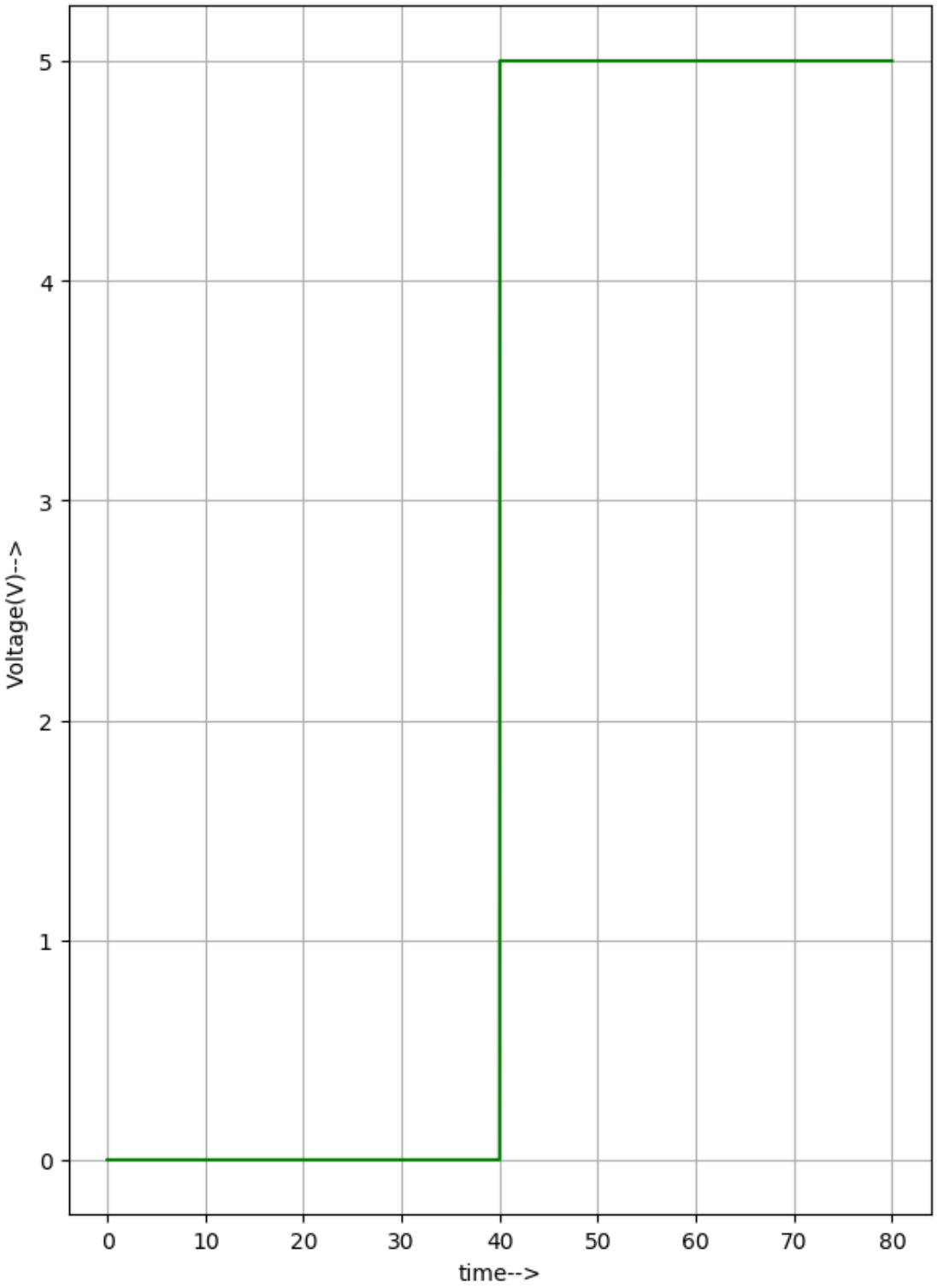
D7:



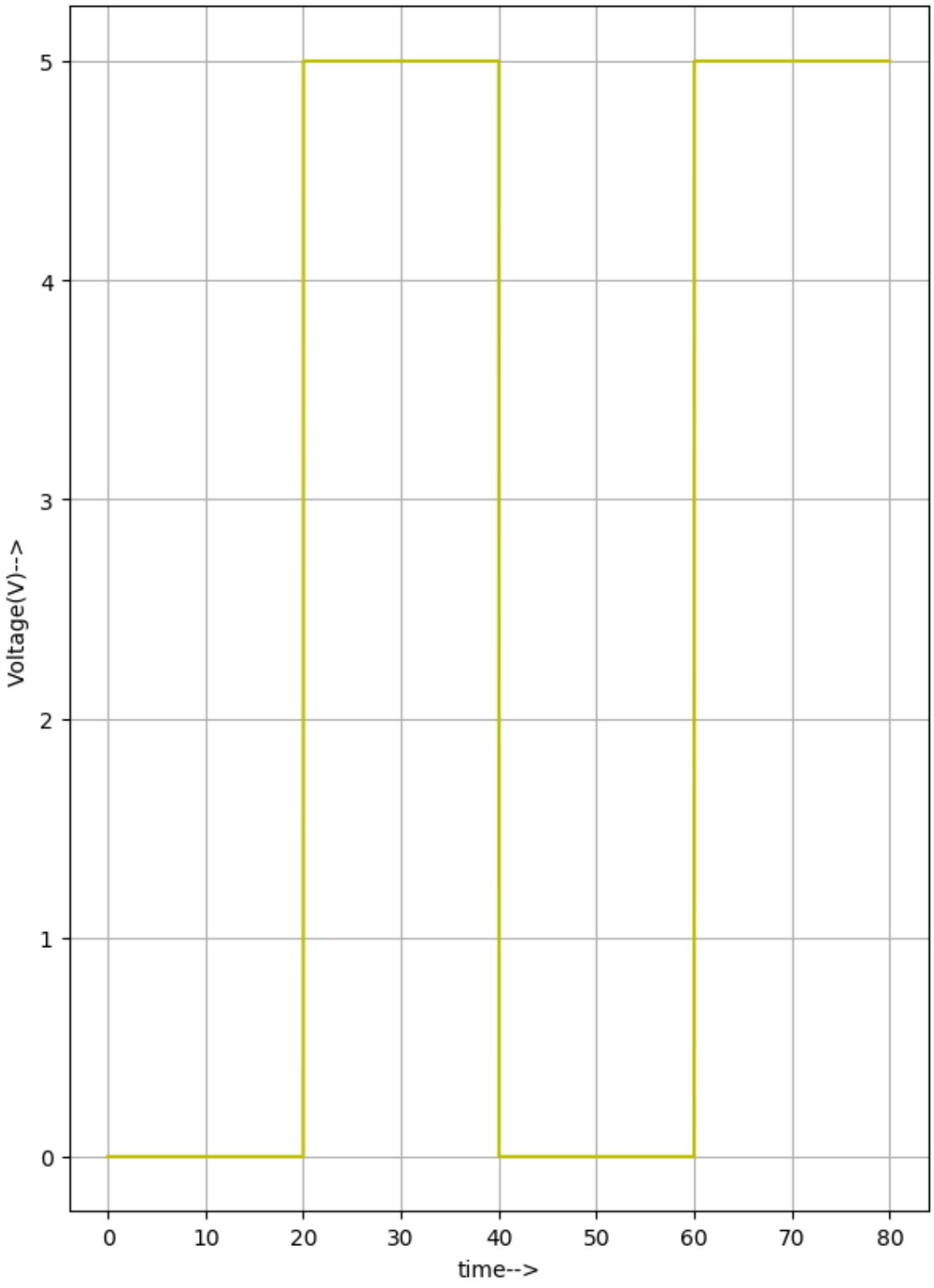
E:



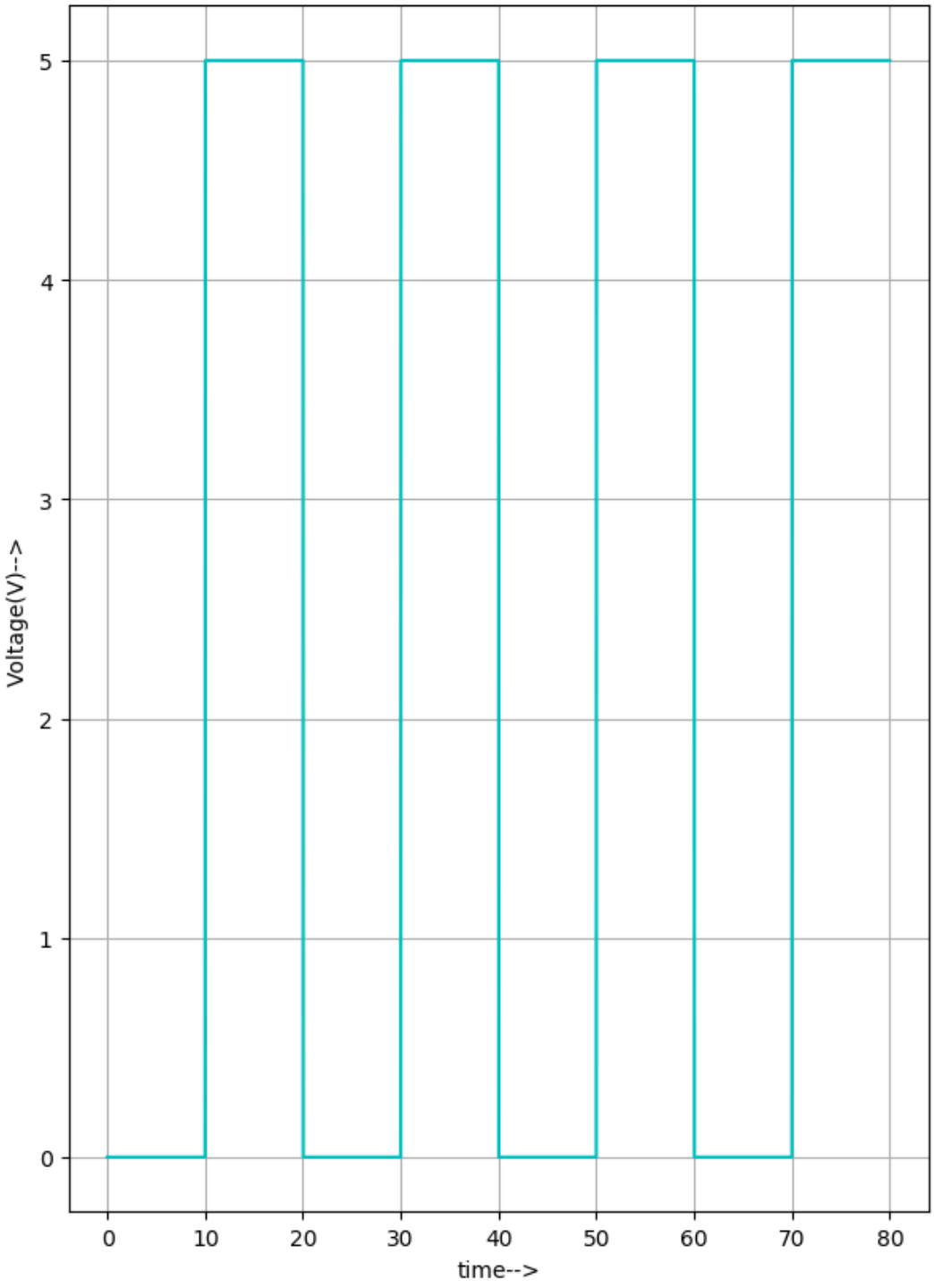
S0:



S1:

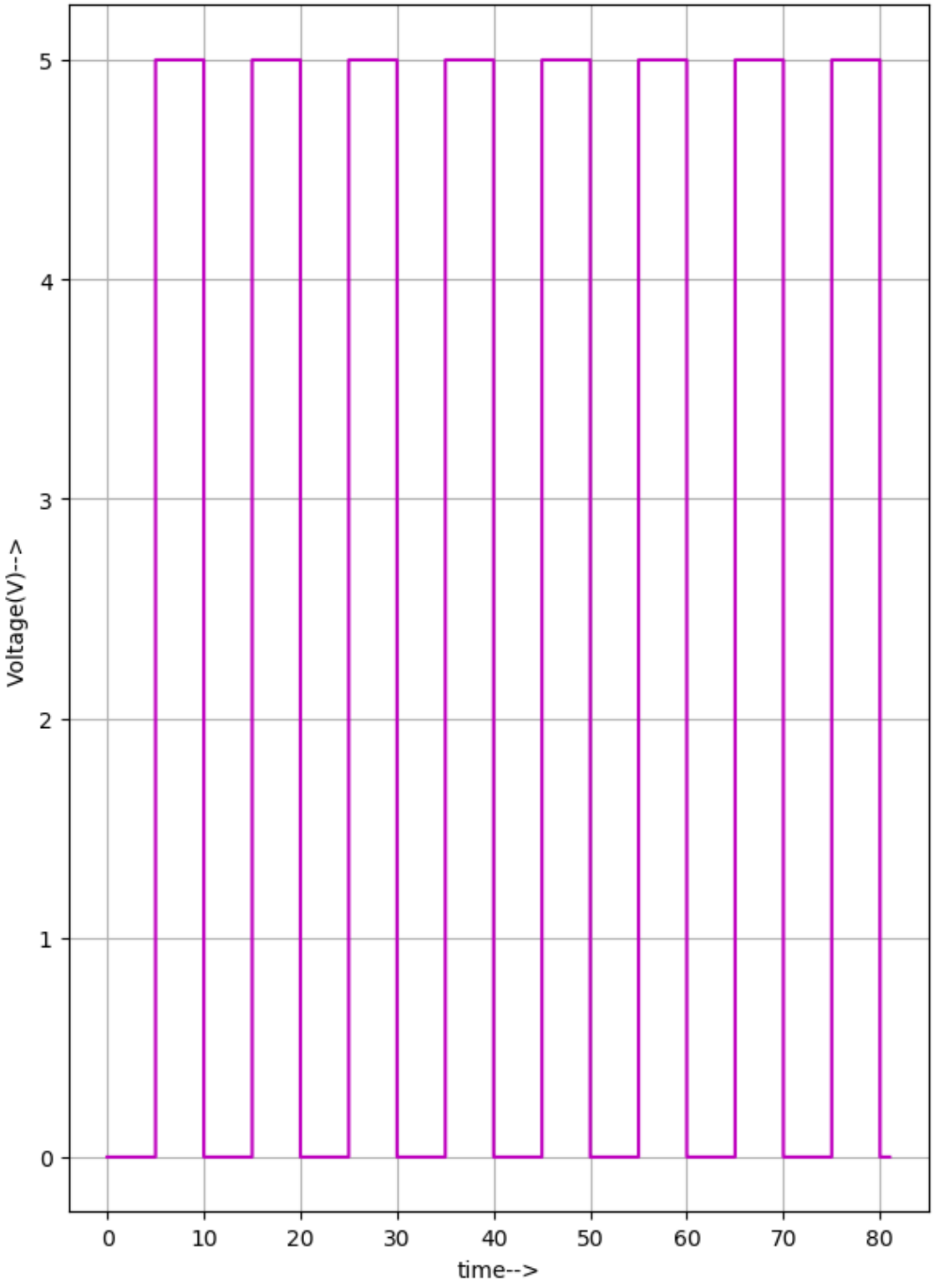


S2:



Python plot-Output Waveforms:

Y:



Source/Reference(s):
https://www.electronicshub.org/multiplexerandmultiplexing/#8-to-1_Multiplexer

https://www.eccircuit.com/2018/10/8-to-1-multiplexer-mux-logic-diagram.html