Circuit Simulation Project

https://esim.fossee.in/circuit-simulation-project

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Project Guide: Dr. Maheswari. R

Title: Design of Half Adder using 4×1 multiplexer as a subcircuit

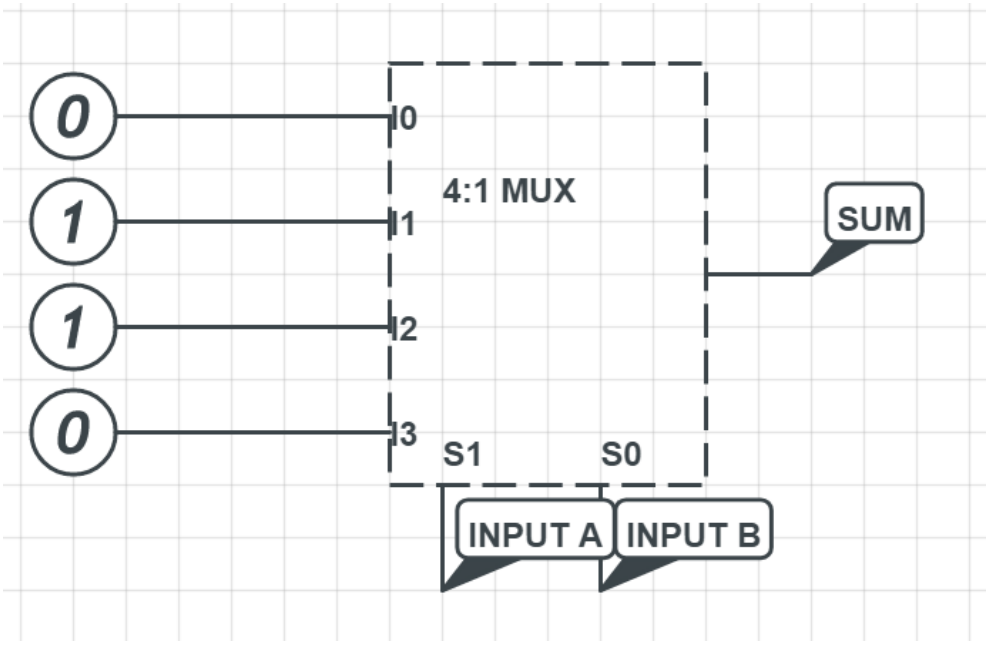
Theory:

A half adder is used to add two single-digit binary numbers and results into a two-digit output. It is named as such because putting two half adders together with the use of an OR gate results in a full adder. In other words, it only does half the work of a full adder. This circuit has two inputs and two outputs. The two inputs A, B denote the two numbers to be added respectively. The two outputs, C and D represent the sum and carry, respectively.
We can implement a half adder using two 4×1 multiplexers.
The truth table for adding two single digit binary digits A and B is shown below:

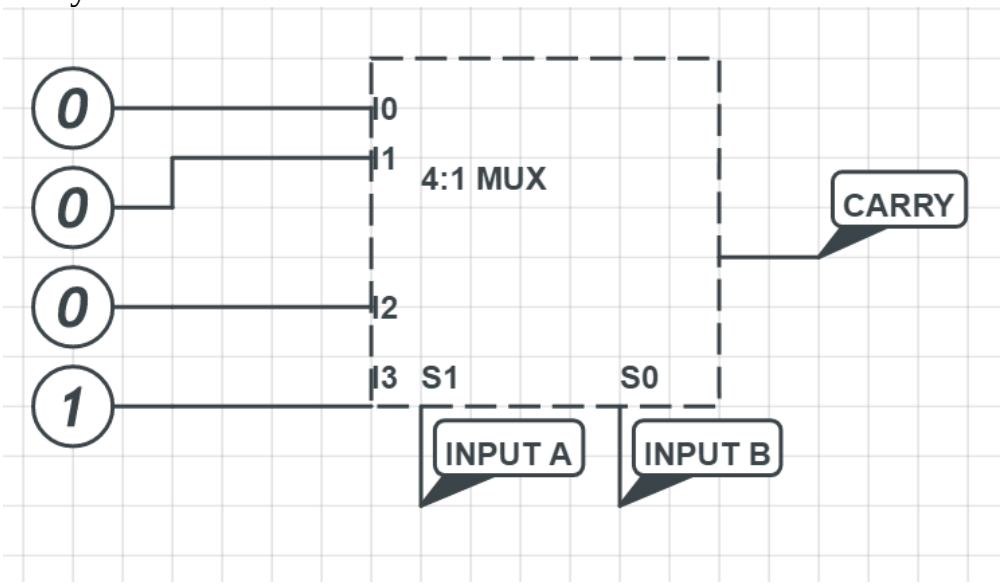
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

We can use the multiplexers to get the sum and carry as shown below:

Sum:

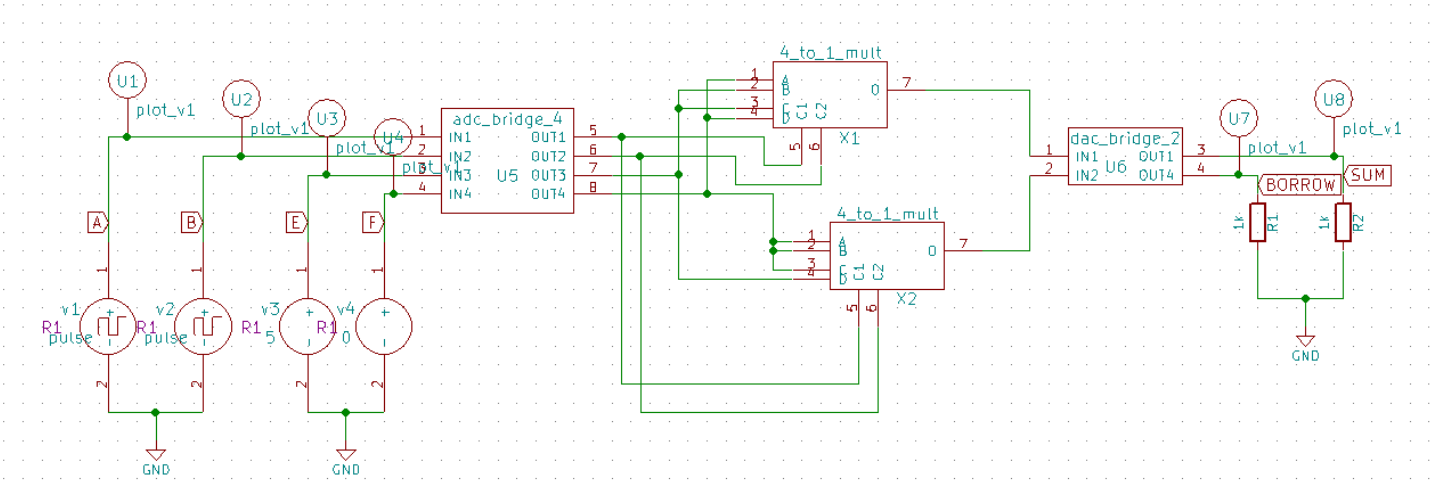


Carry:

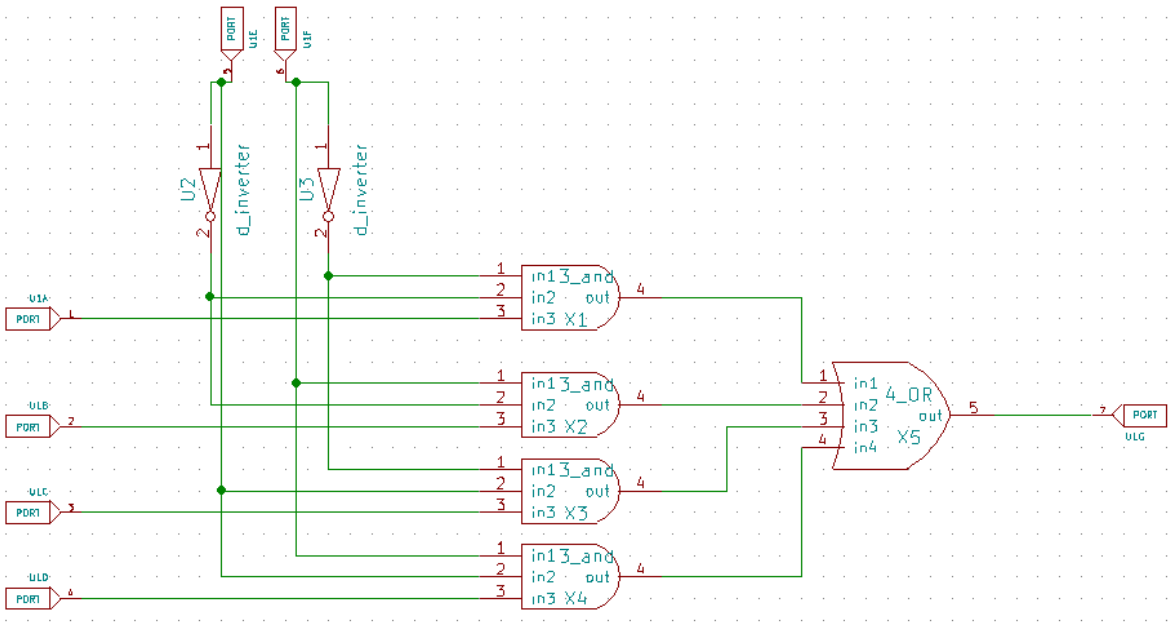


Circuit Diagrams: -

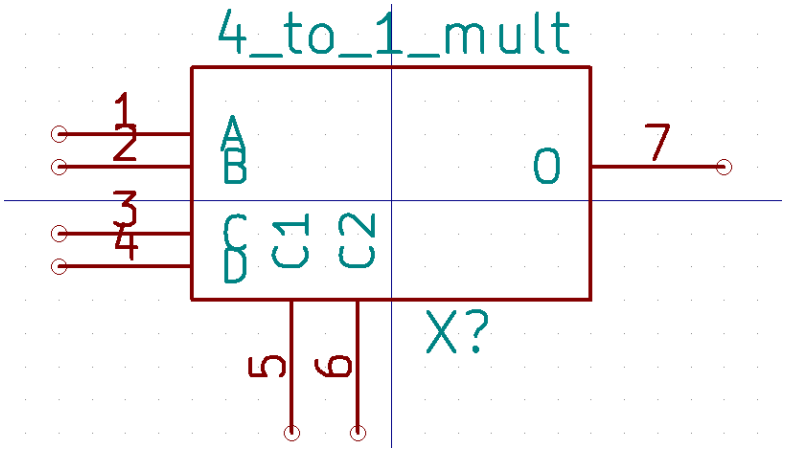
This is the main functional circuit schematic for the half adder which uses a subcircuit (4×1 multiplexer):



The structure of the 4×1 multiplexer subcircuit used:



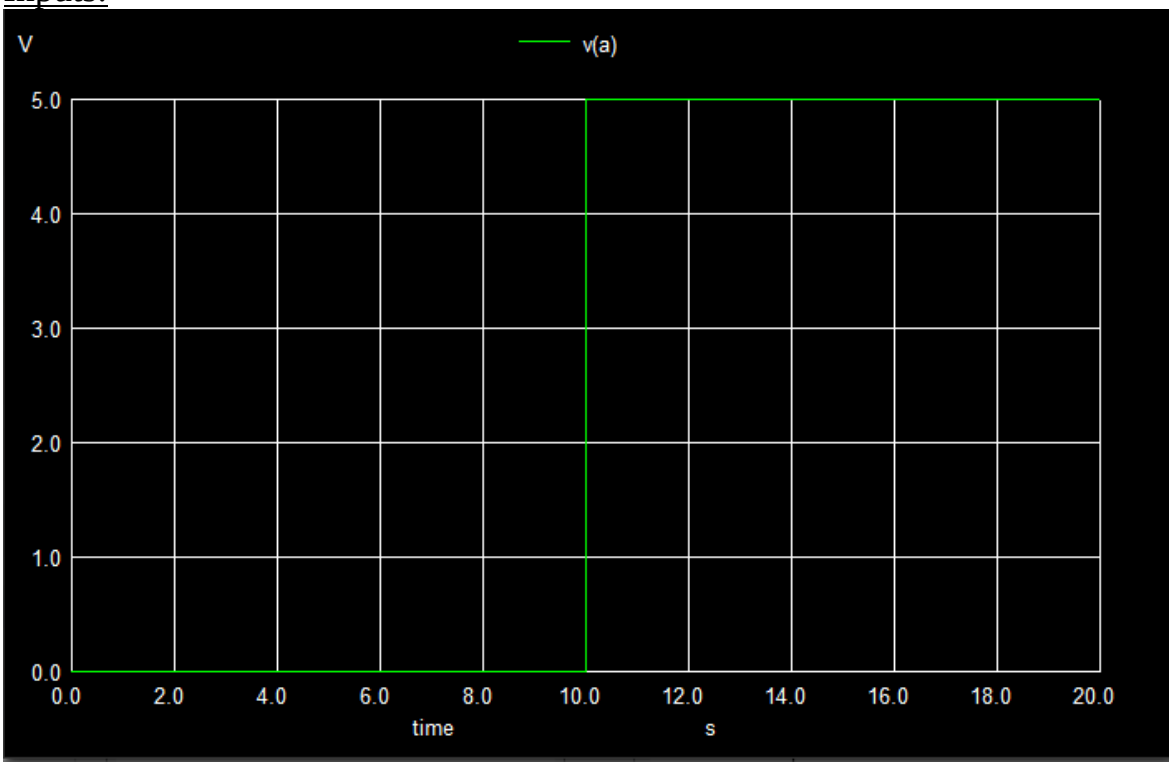
The symbol defined for the subcircuit:

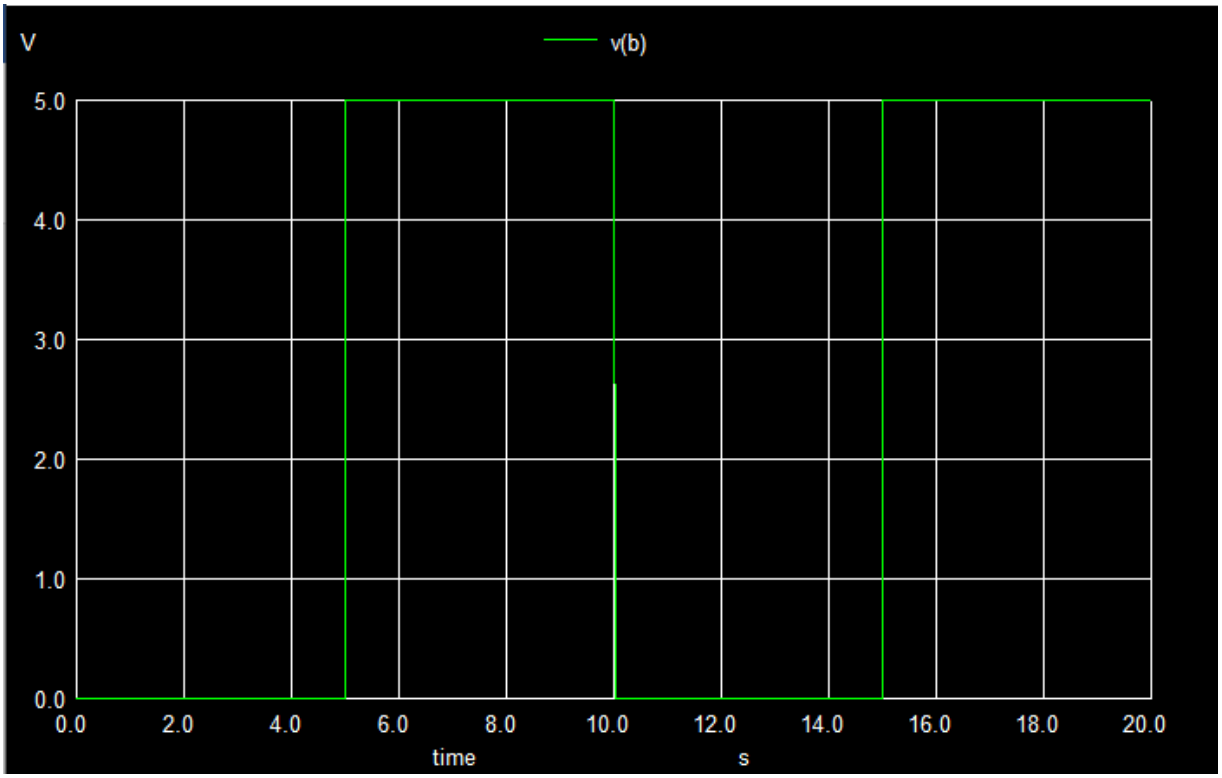


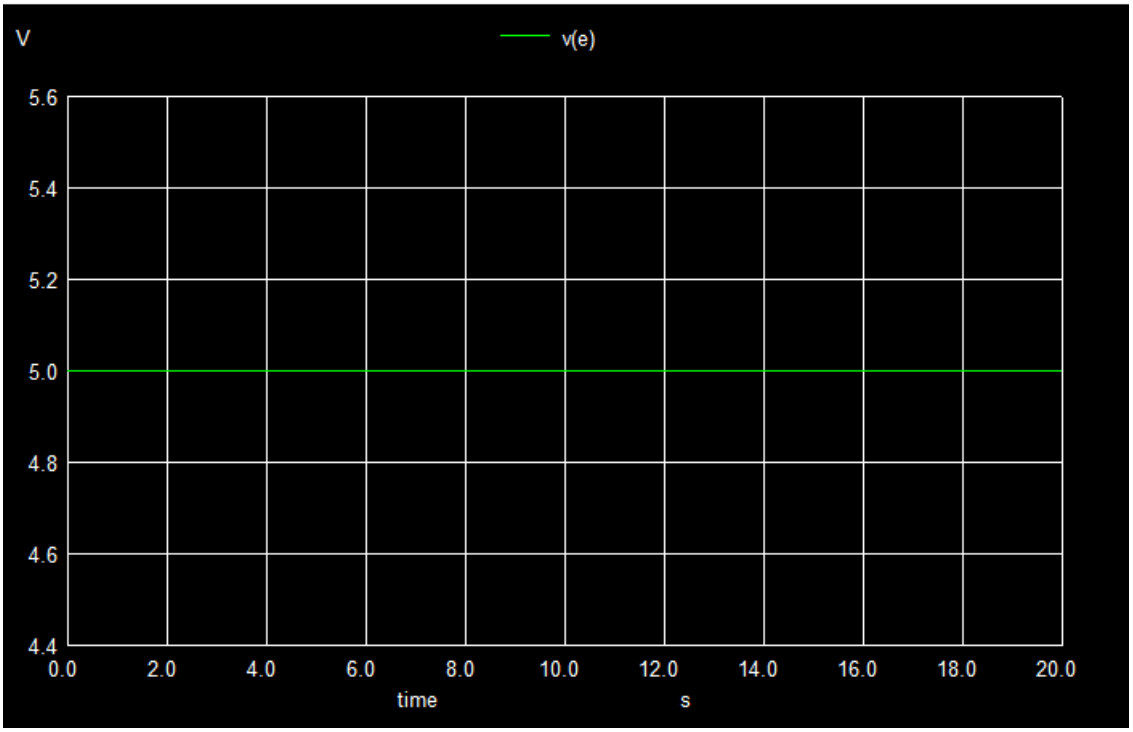
Result:

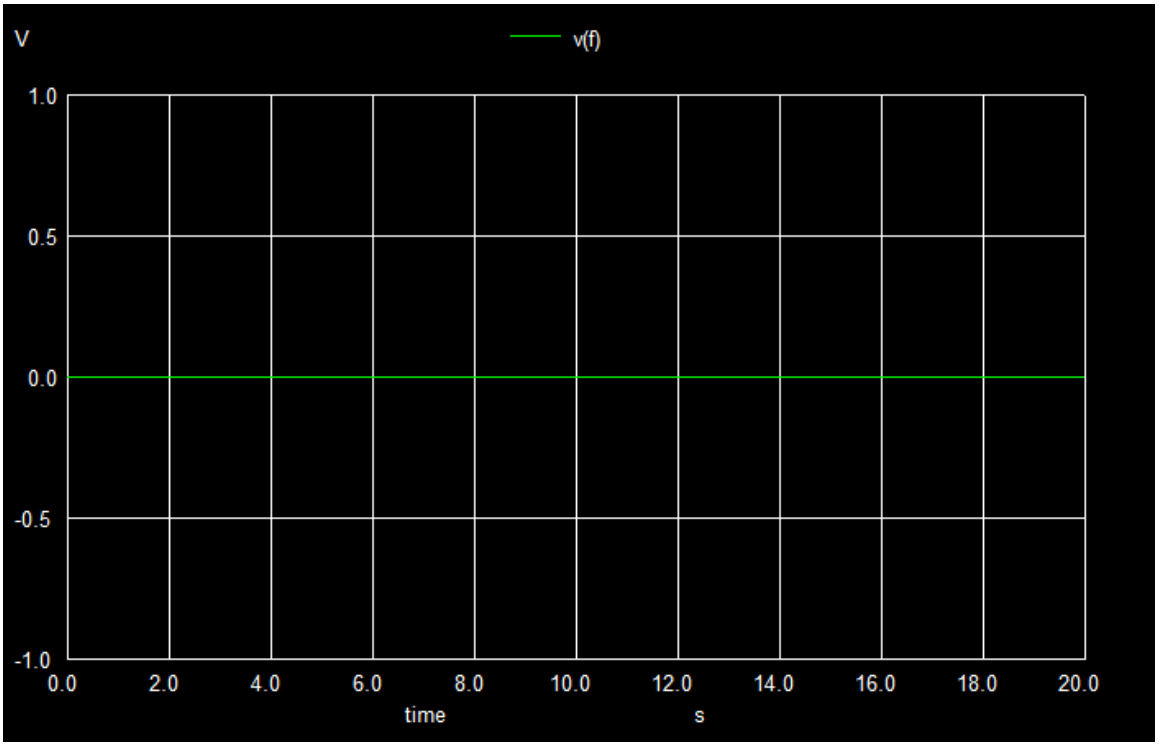
Ngspice Plots:

Inputs:



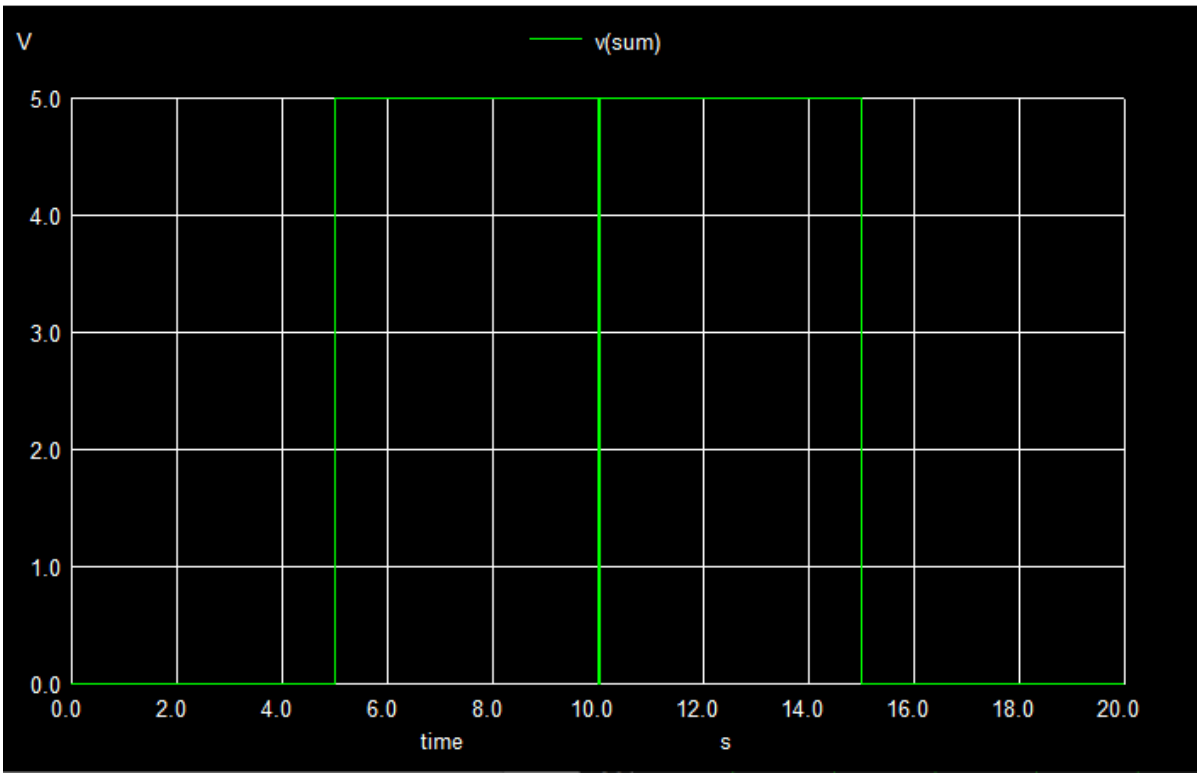



V
v(e)
5.6
5.4
5.2
5.0
4.8
4.6
4.4
0.0
2.0
4.0
6.0
8.0
10.0
12.0
14.0
16.0
18.0
20.0
time
s

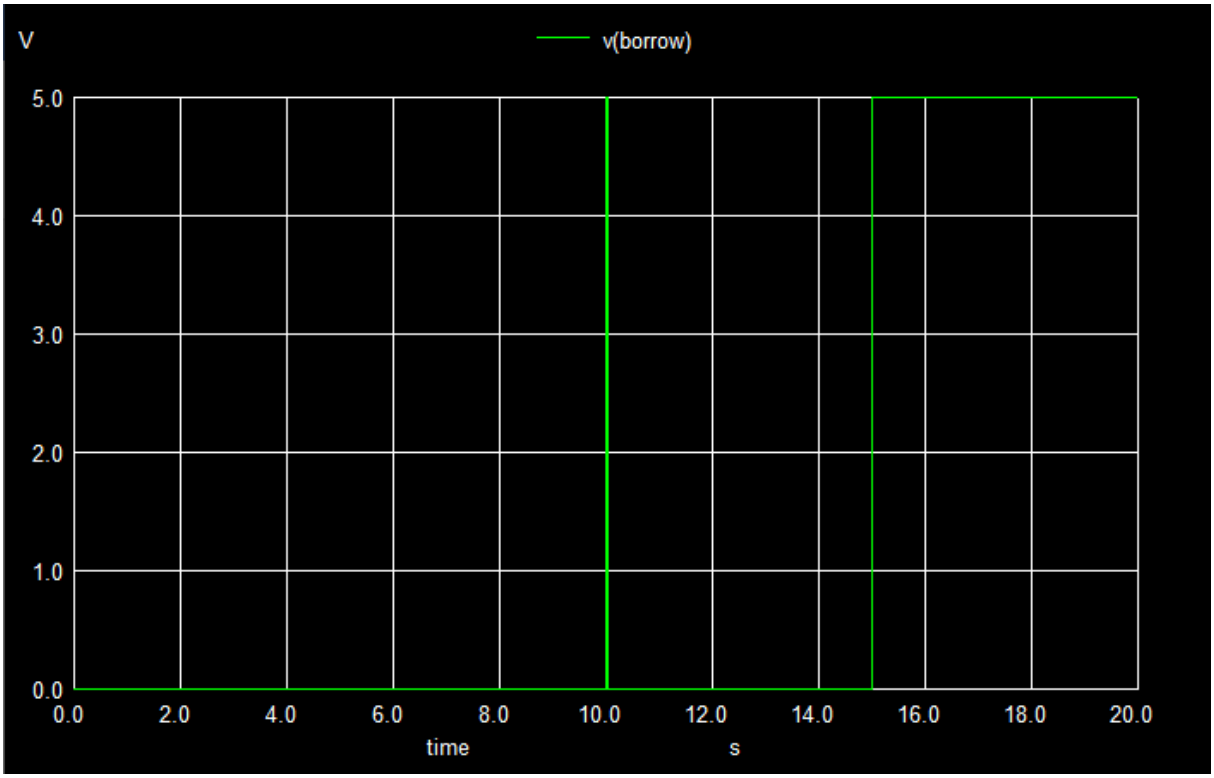

V
v(f)
1.0
0.5
0.0
-0.5
-1.0
0.0
2.0
4.0
6.0
8.0
10.0
12.0
14.0
16.0
18.0
20.0
time
s

Outputs:

Sum:



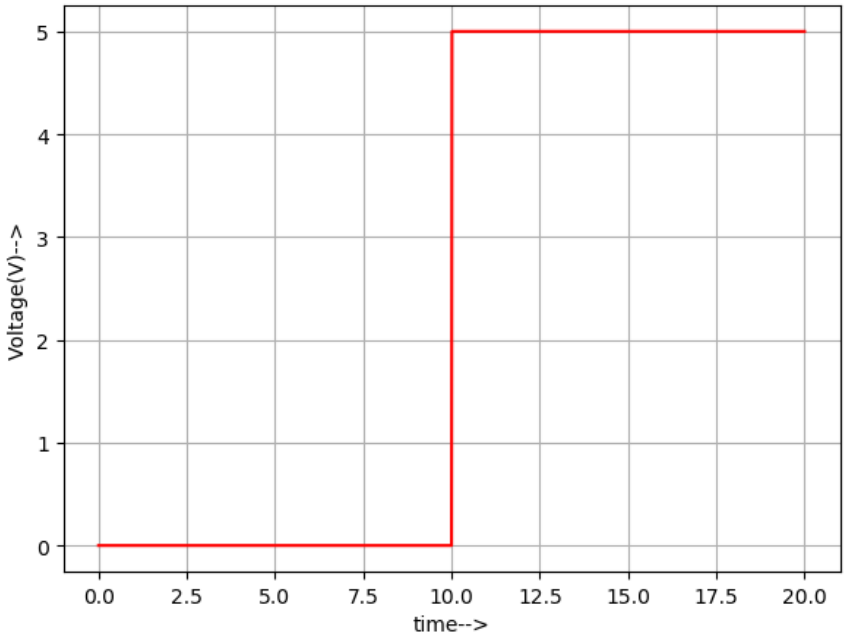
Borrow:



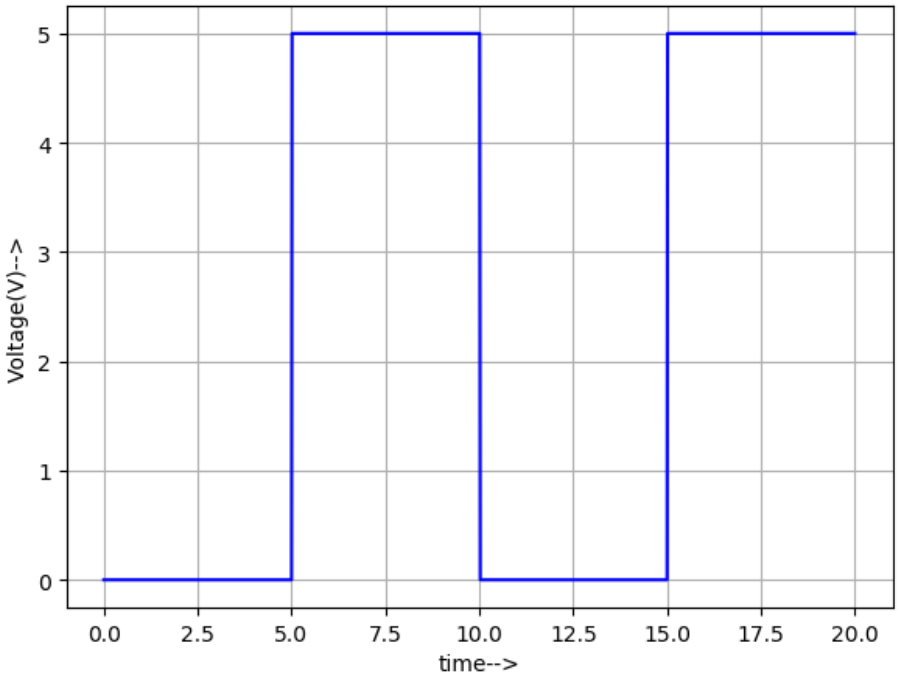
Python Plots:

Inputs:

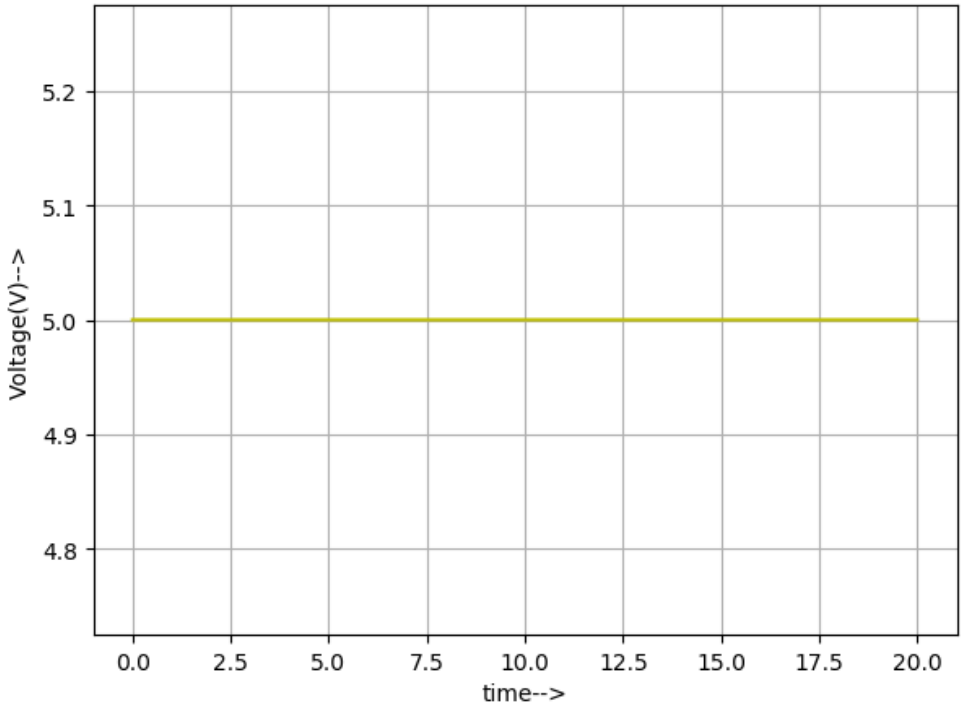
A



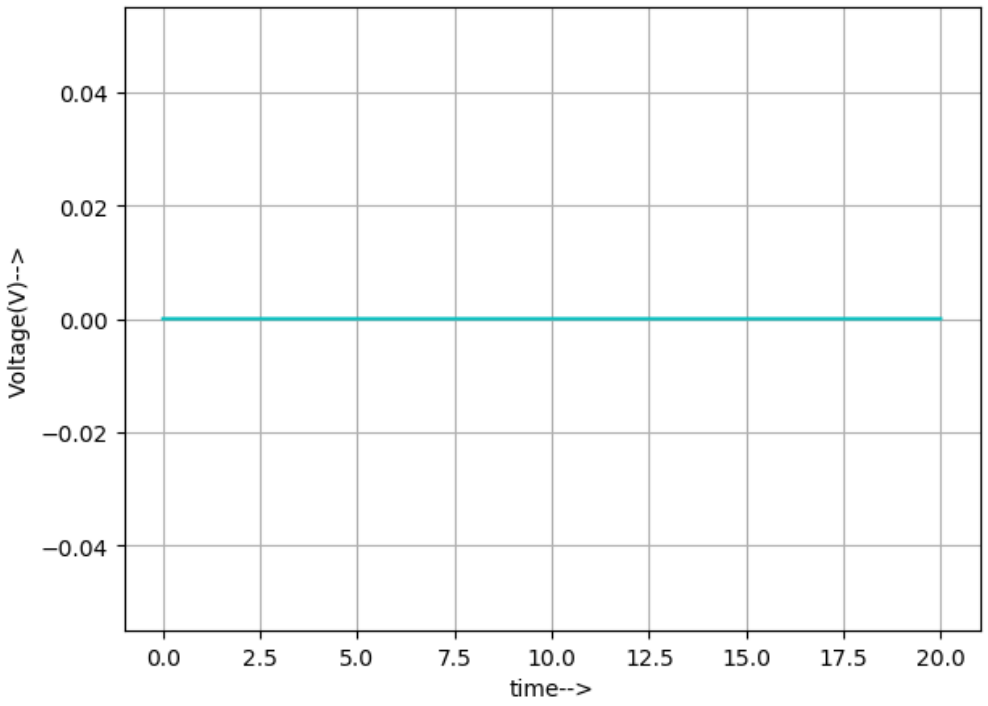
B



E

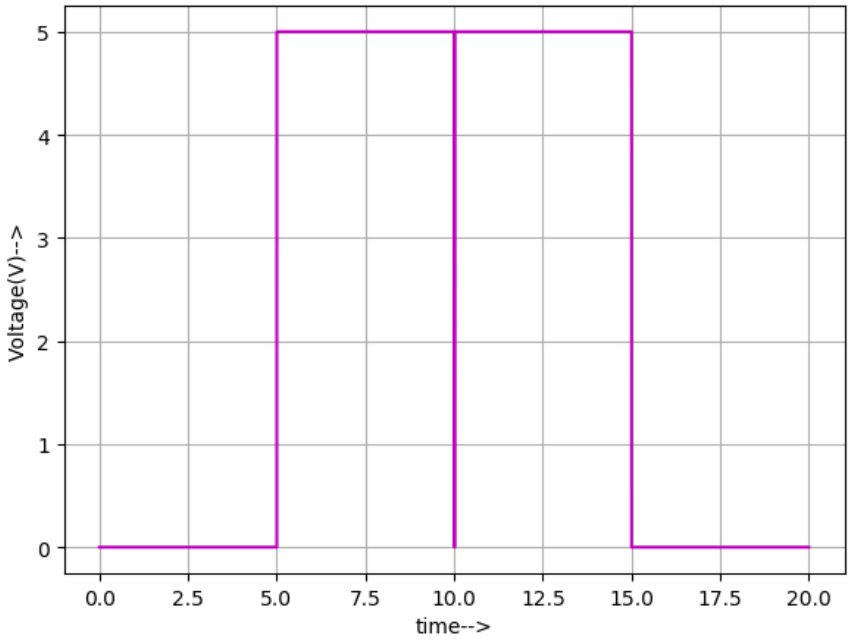

5.2
5.1
5.0
4.9
4.8
Voltage(V)-->
0.0
2.5
5.0
7.5
10.0
12.5
15.0
17.5
20.0
time-->

F

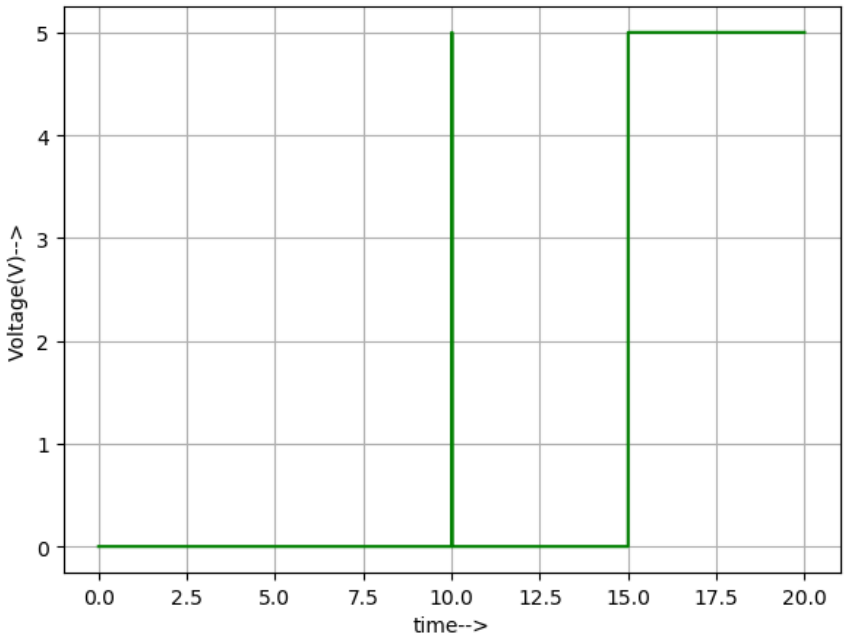

0.04
0.02
0.00
−0.02
−0.04
Voltage(V)-->
0.0
2.5
5.0
7.5
10.0
12.5
15.0
17.5
20.0
time-->

Outputs:

Sum:



Borrow:



References: -

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- https://www.geeksforgeeks.org/half-adder-in-digital-logic/
- https://www.techopedia.com/definition/7509/half-adder