Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

Circuit Simulation Project

https://esim.fossee.in/circuit-simulation-project

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Project Guide: Dr R. Maheshwari

Title of the Circuit: Implementation of AND gate using NOR gates

Theory:

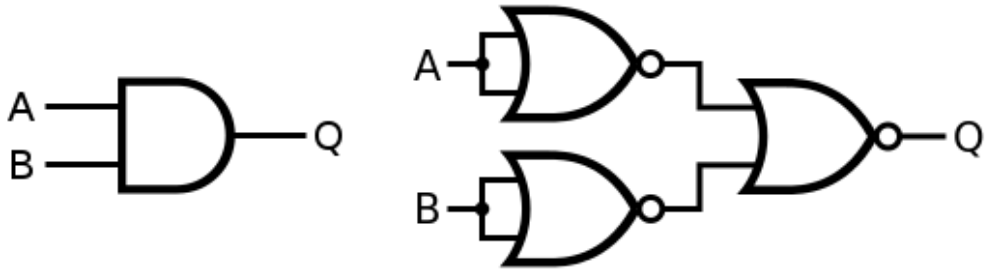
An AND gate gives a 1 output when both inputs are 1. Therefore, an AND gate is made by inverting the inputs of a NOR gate. Again, note that a NOT gate is equivalent to a NOR with its inputs joined.

From De Morgan's theorems: (A+B)' = A'B' => (A'+B')' = A''B'' = AB

So, give the inverted inputs to a NOR gate, obtain AND operation at output

CIRCUIT DIAGRAM:

Desired AND Gate **NOR Construction**



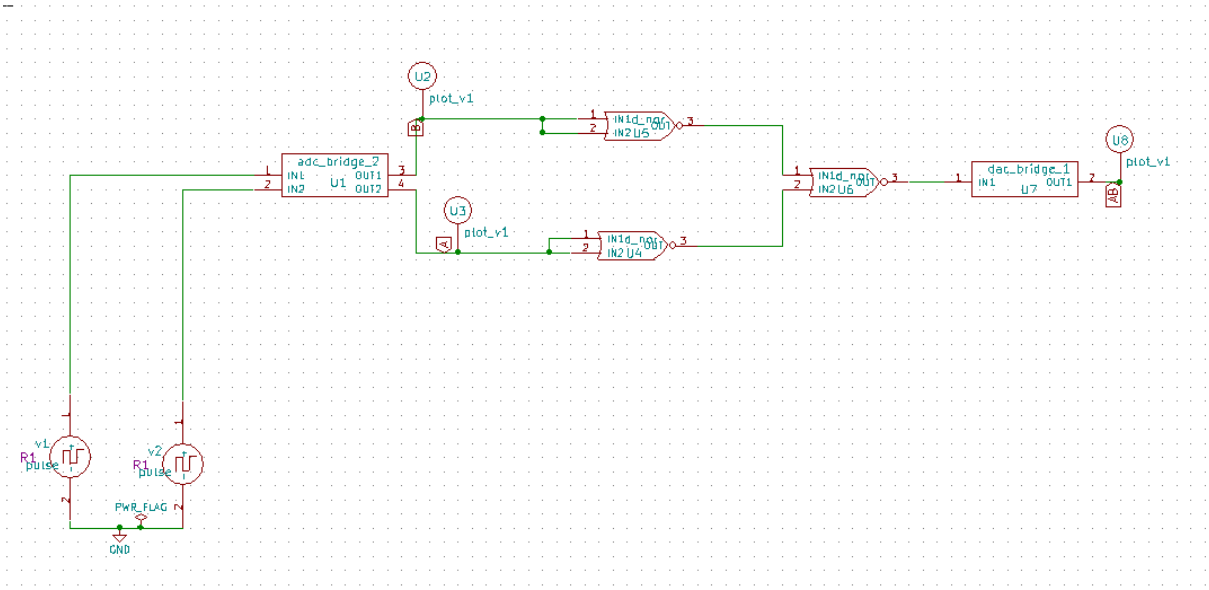
Q = **A** AND **B** = (**A** NOR **A**) NOR (**B** NOR **B**)

Truth Table:

Truth Table

Input A	Input B	Output Q
0	0	0
0	1	0
1	0	0
1	1	1

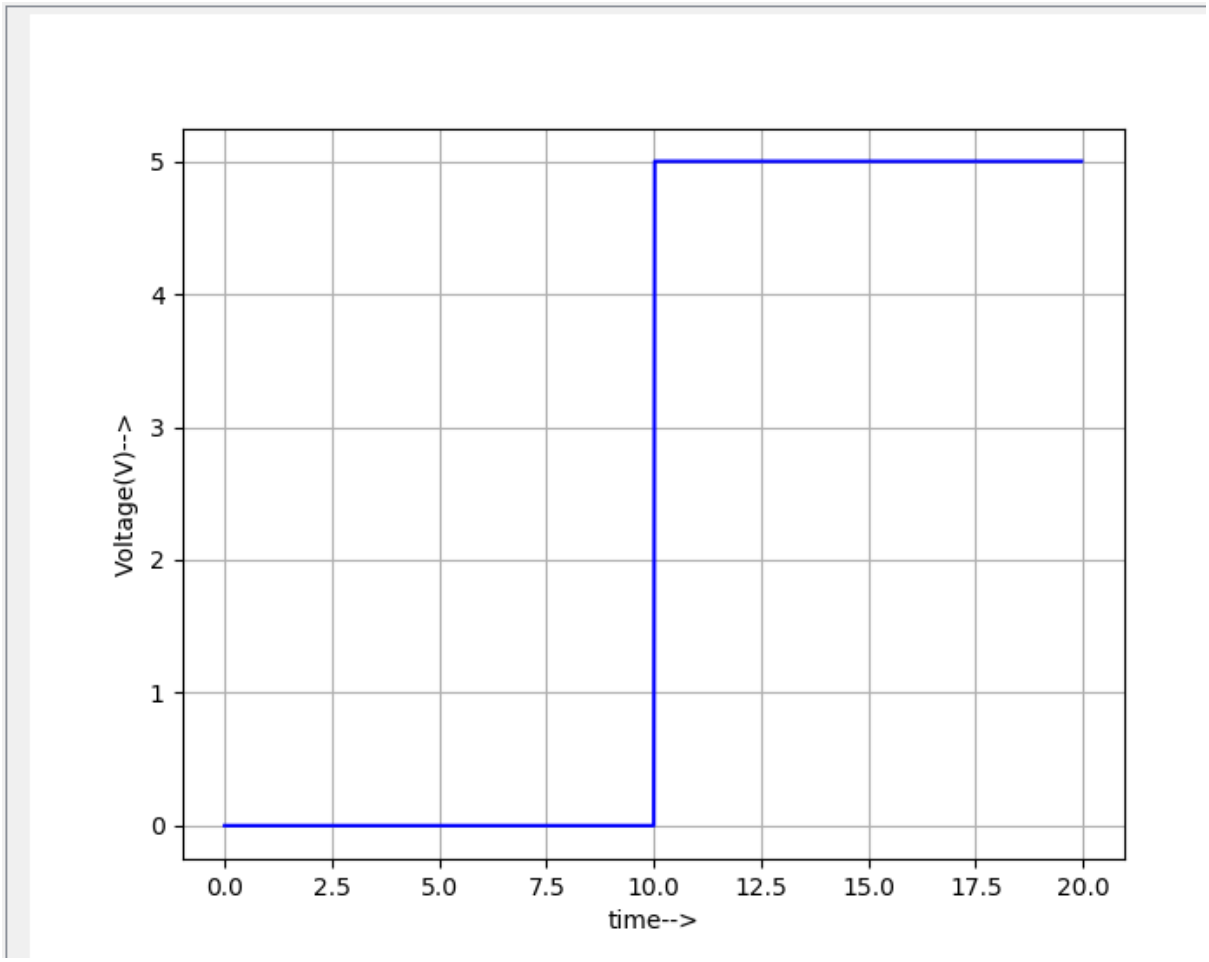
e-Sim Schematic:



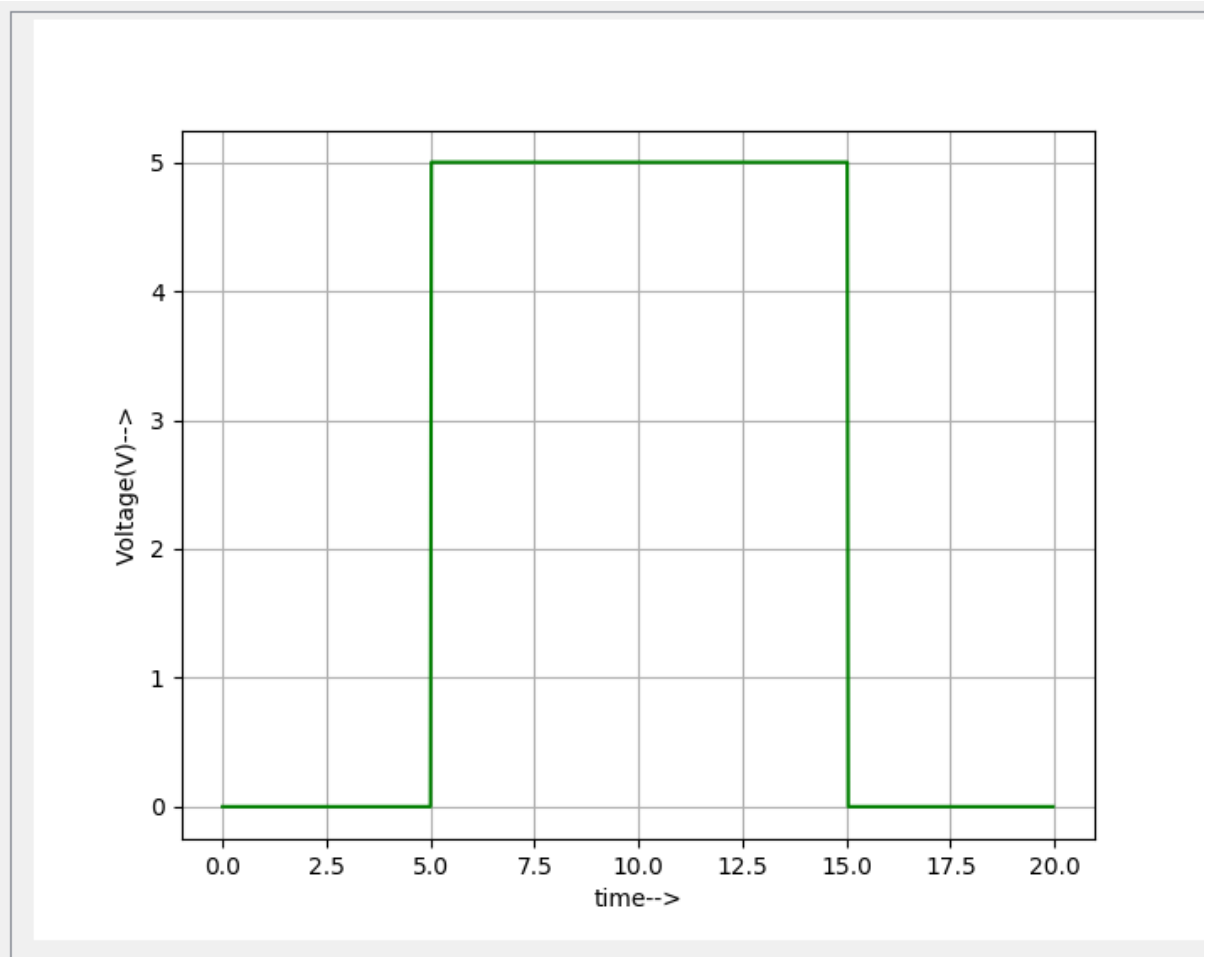
Simulation Results:

1. **Python Waveforms:**

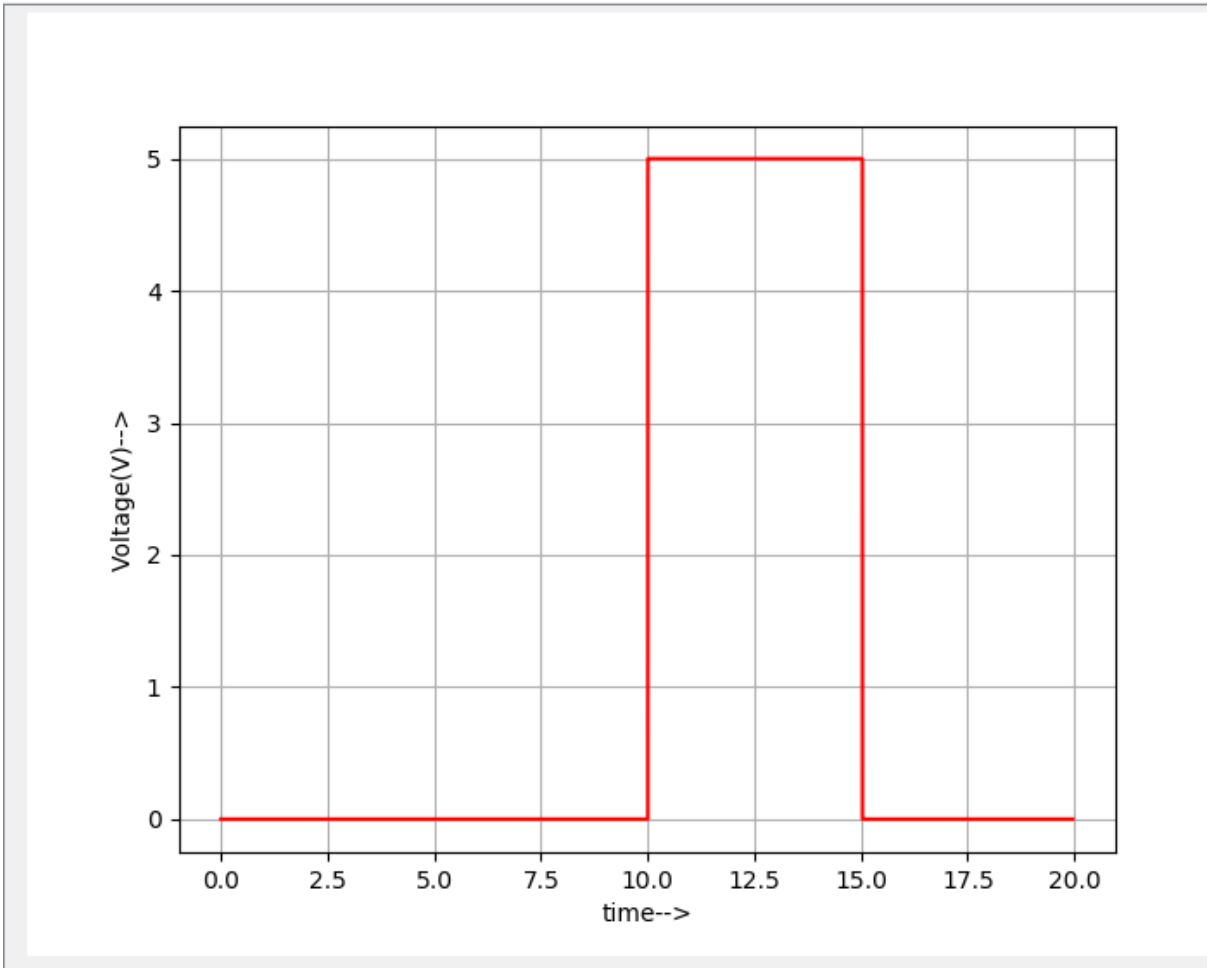
A



B

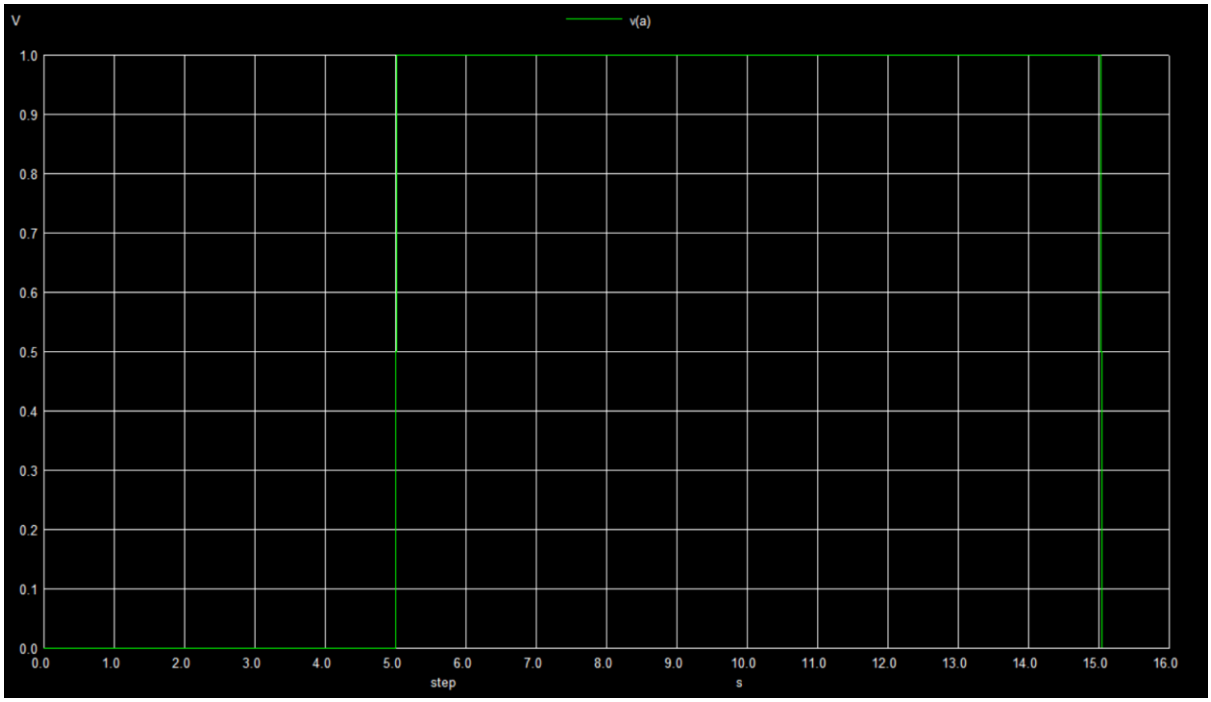


A.B

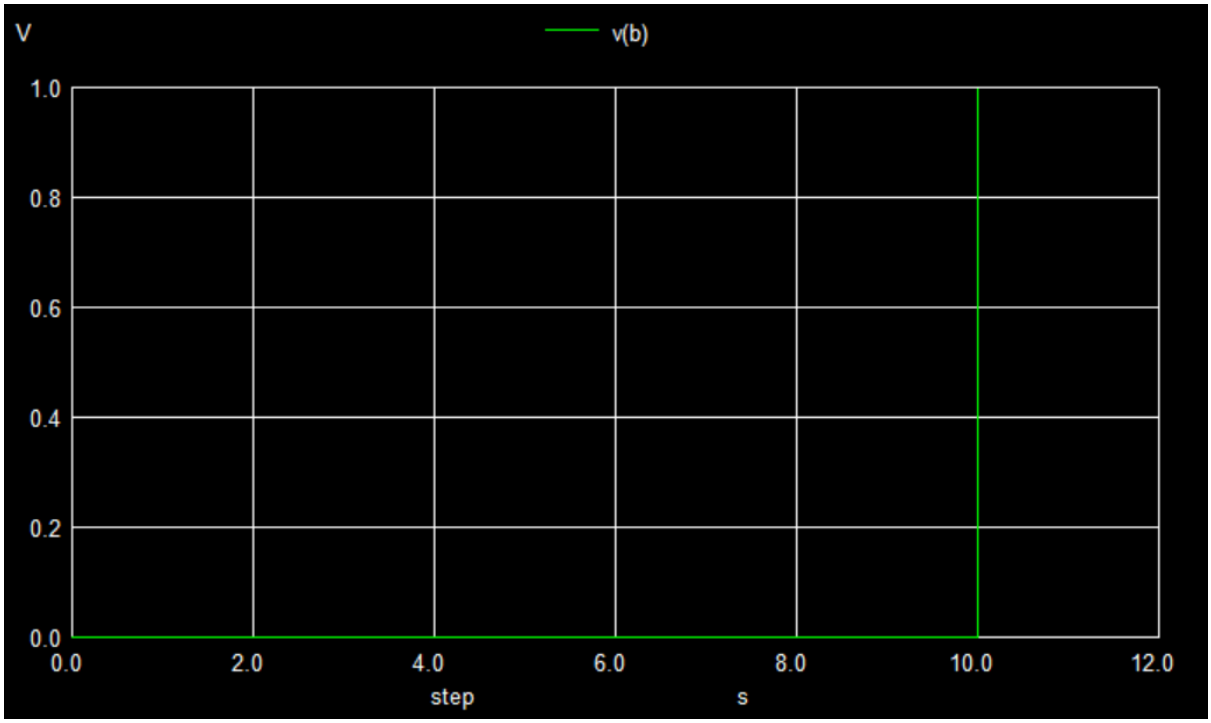


NG Spice Waveforms:

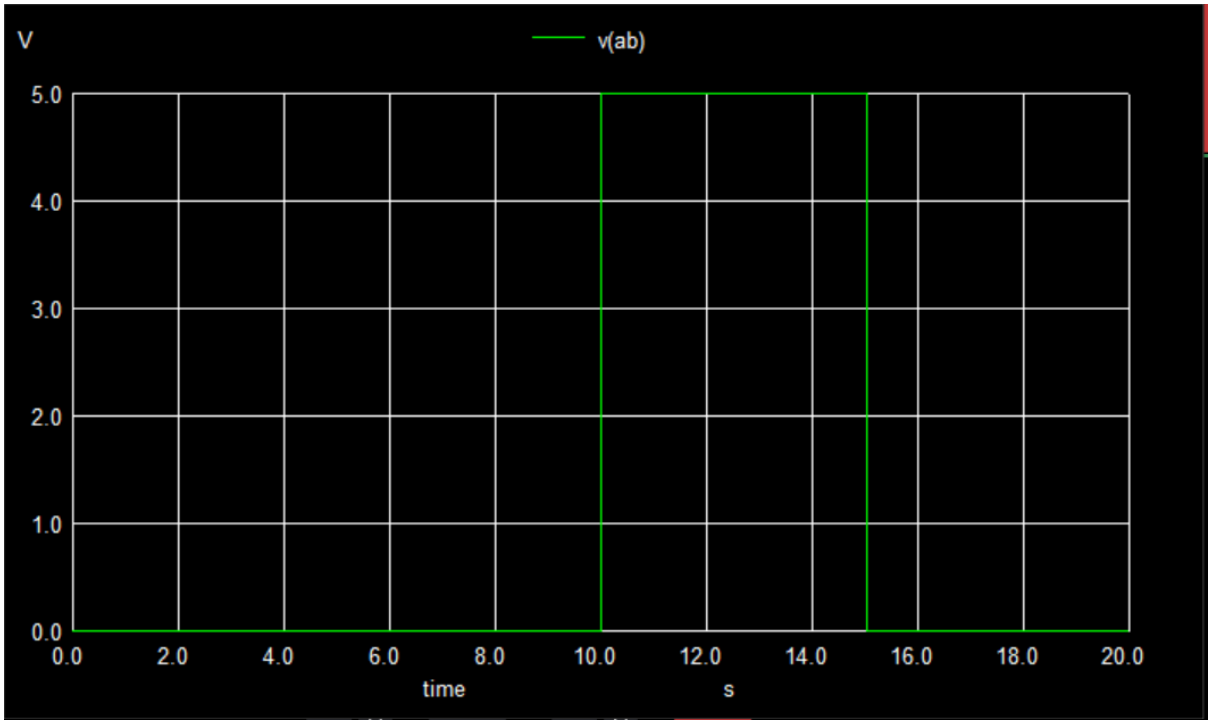
A


V
v(a)
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
0.0 1.0 2.0 3.0 4.0 5.0 6.0 7.0 8.0 9.0 10.0 11.0 12.0 13.0 14.0 15.0 16.0
step
s

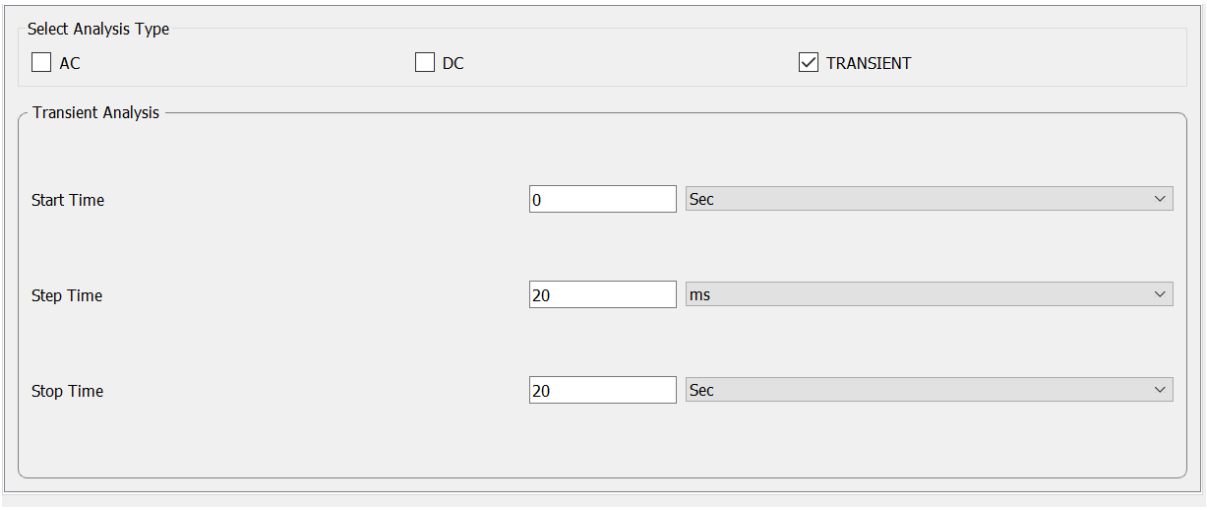
B


V
v(b)
1.0
0.8
0.6
0.4
0.2
0.0
0.0 2.0 4.0 6.0 8.0 10.0 12.0
step
s

A.B



Transient Analysis:



Conclusion:

Thus, the circuit has been designed and verified.

References:

https://www.iitr.ac.in/departments/PH/uploads/Teaching%20Laboratory/Electronics/5.Interconversion%20of%20Universal%20Gates%20and%20De%20Morgans%20Theorem.pdf

https://en.wikipedia.org/wiki/NOR_logic