Circuit Simulation Project

https://esim.fossee.in/circuit-simulation-project

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Project guide: Dr. Maheswari. R

Title of the circuit: 4 Bit Asynchronous UP Counter Using D Flip Flops

Theory/Description:

A 4 bit asynchronous UP counter with D flip flop is shown in above diagram. It is capable of counting numbers from 0 to 15. The clock inputs of all flip flops are cascaded and the D input (DATA input) of each flip flop is connected to a state output of the flip flop.

That means the flip flops will toggle at each active edge or positive edge of the clock signal. The clock input is connected to first flip flop. The other flip flops in counter receive the clock signal input from Q' output of previous flip flop. The output of the first flip flop will change, when the positive edge on clock signal occurs.

In the asynchronous 4- bit up counter, the flip flops are connected in toggle mode, so when the when the clock input is connected to first flip flop FF0, then its output after one clock pulse will become 20.

The rising edge of the Q output of each flip flop triggers the clock input of its next flip flop. It triggers the next clock frequency to half of its applied input. The Q outputs of every individual flip flop (Q0, Q1, Q2, Q3) represents the count of the 4 bit UP counter such as 20 (1) to 23 (8).

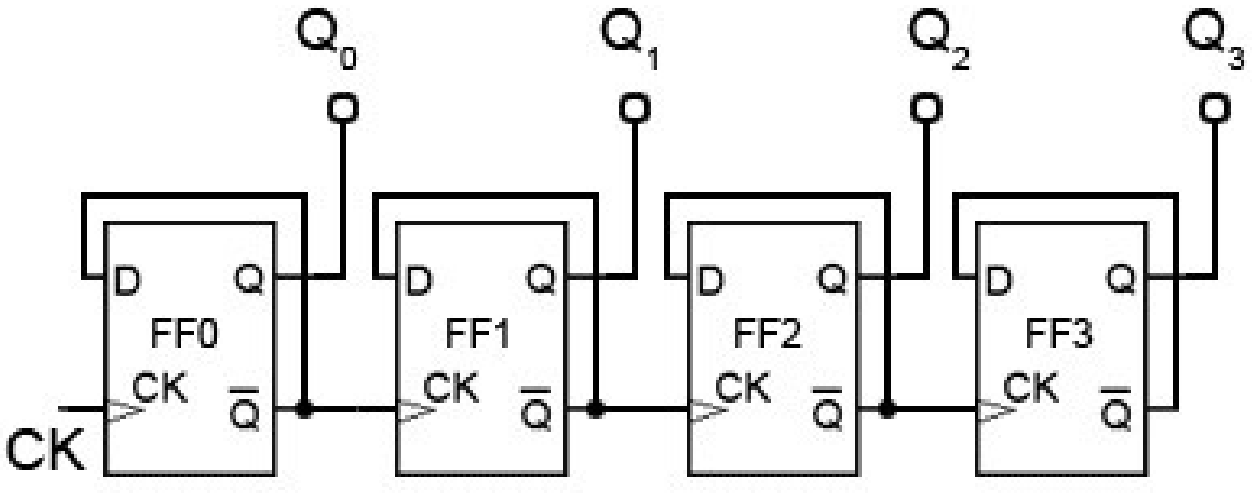
Working of asynchronous up counter is explained below,

Let us assume that the 4 Q outputs of the flip flops are initially 0000. When the rising edge of the clock pulse is applied to the FF0, then the output Q0 will change to logic 1 and the next clock pulse will change the Q0 output to logic 0. This means the output state of the clock pulse toggles (changes from 0 to1) for one cycle.

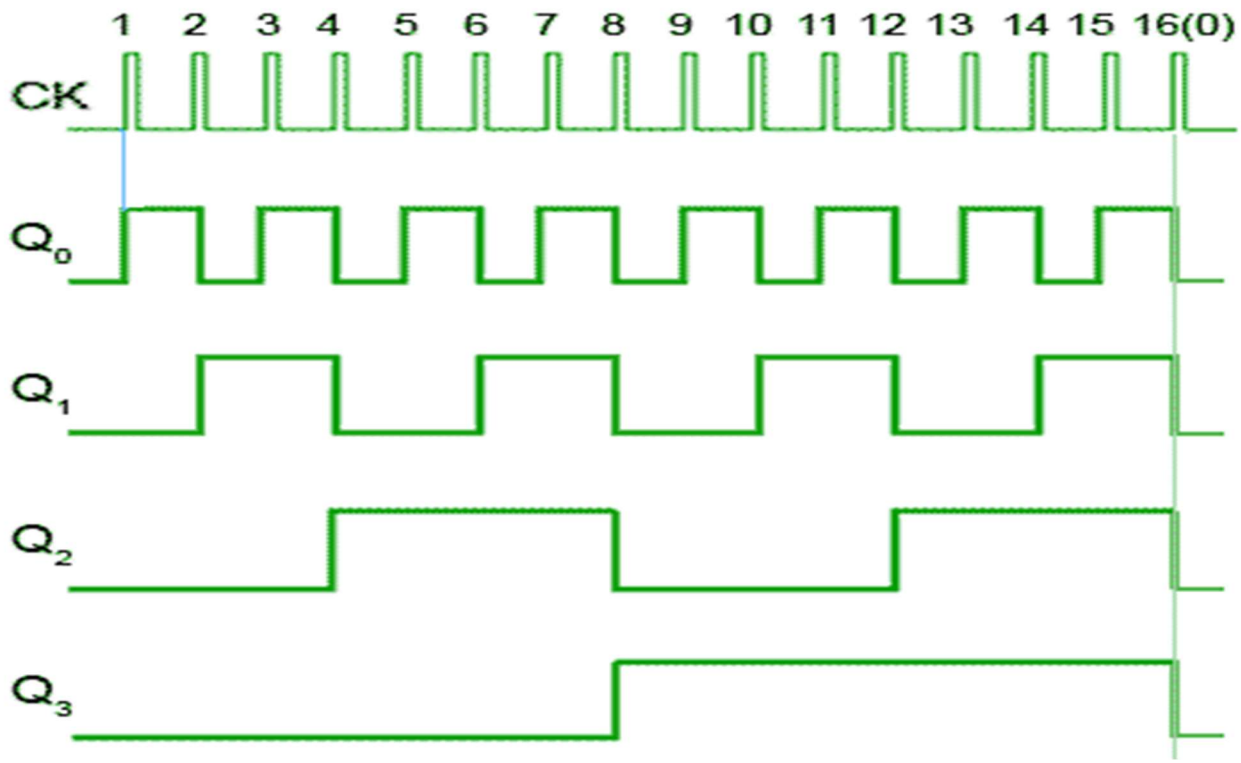
As the Q' of FF0 is connected to the clock input of FF1, then the clock input of second flip flop will become 1. This makes the output of FF1 to be high (i.e. Q1 = 1), which indicates the value 20. In this way the next clock pulse will make the Q0 to become high again.

So now both Q0 and Q1 are high, this results in making the 4 bit output 11002. Now if we apply the fourth clock pulse, it will make the Q0 and Q1 to low state and toggles the FF2. So the output Q2 will become 0010¬2. As this circuit is 4 bit up counter, the output is sequence of binary values from 0, 1, 2, 3....15 i.e. 00002 to 11112 (0 to 1510).

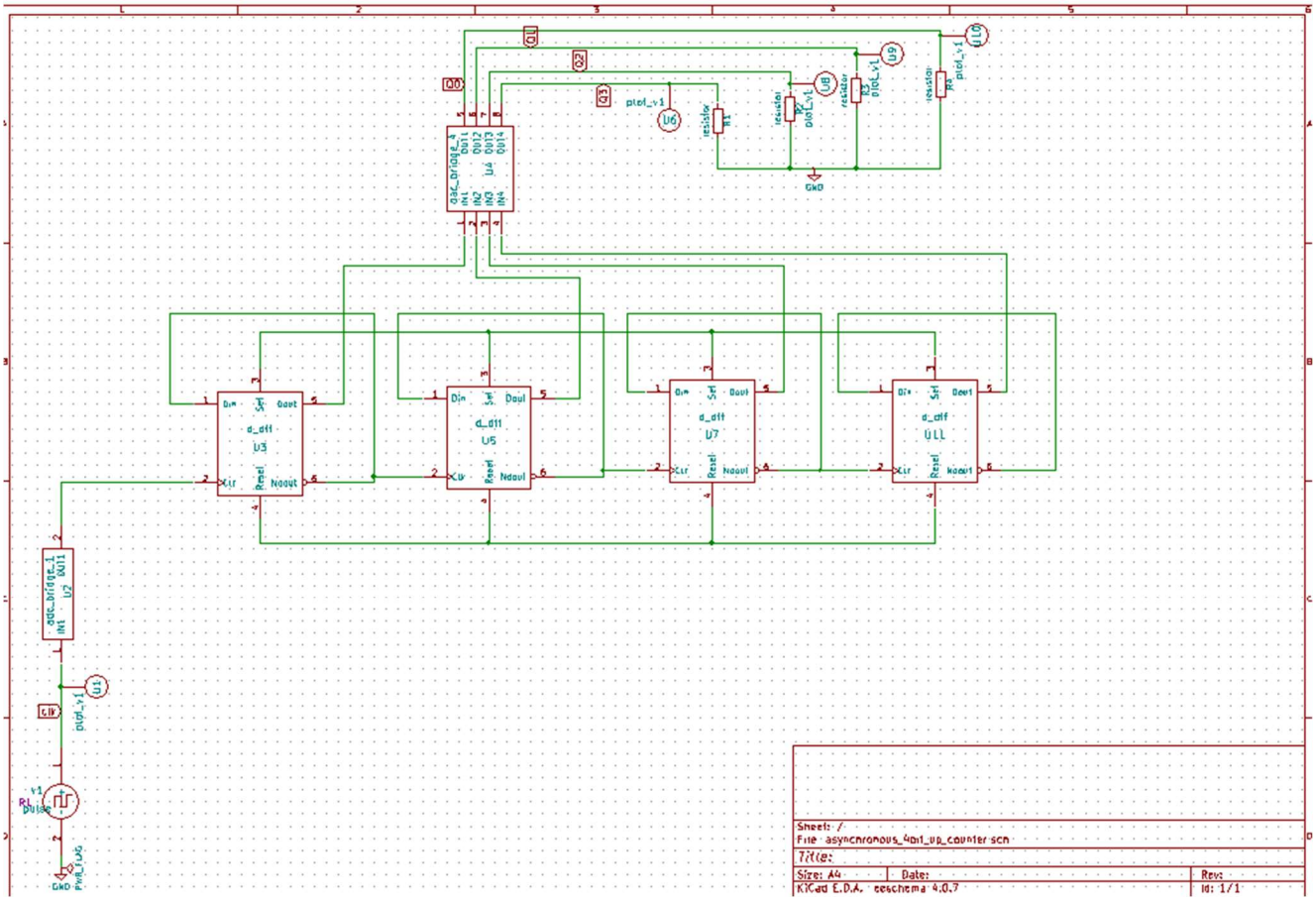
Circuit Diagram:



OUTPUT:

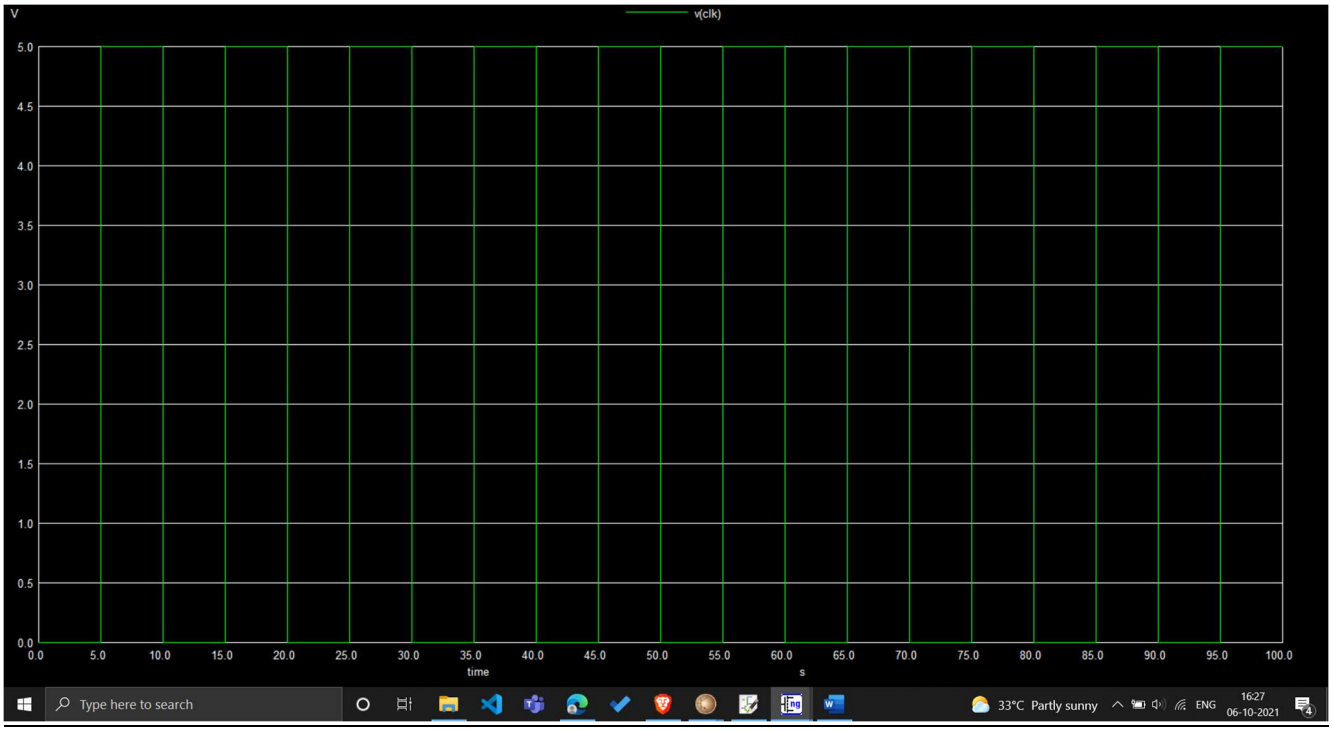


ESIM Circuit Design:

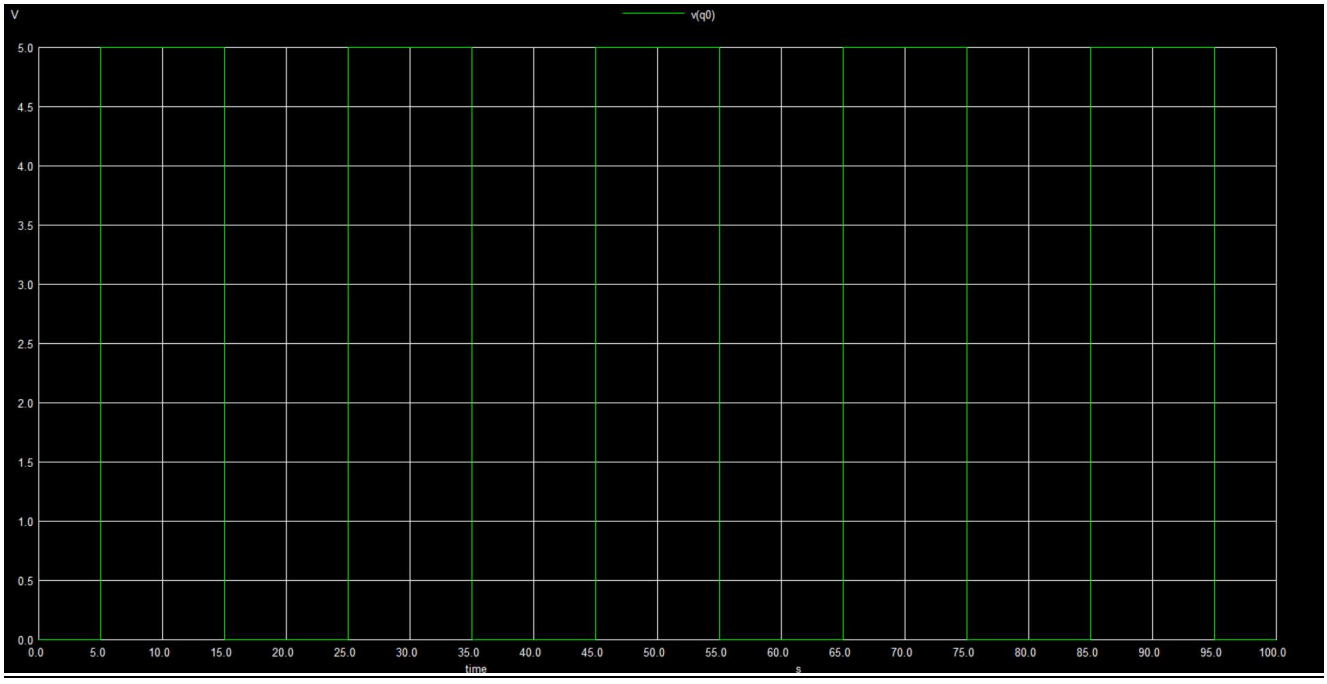


OUTPUT(NG SP[ICE)

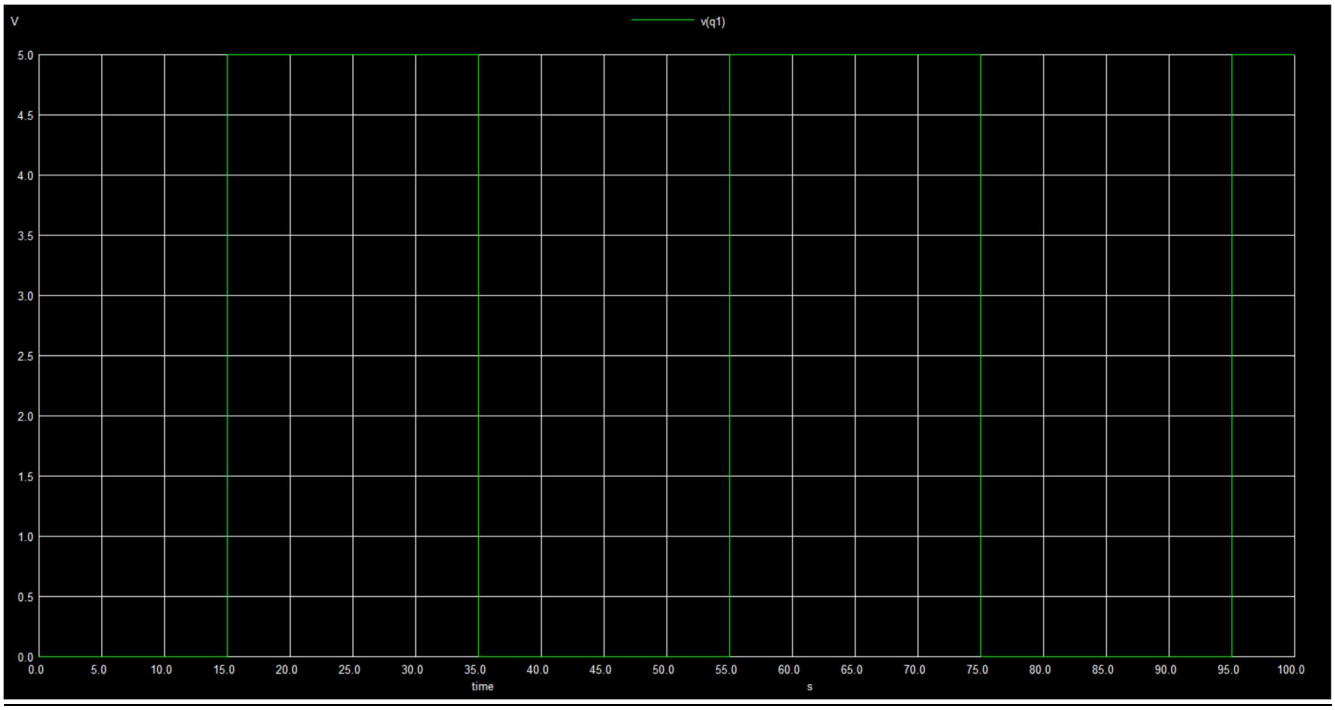
CLK:



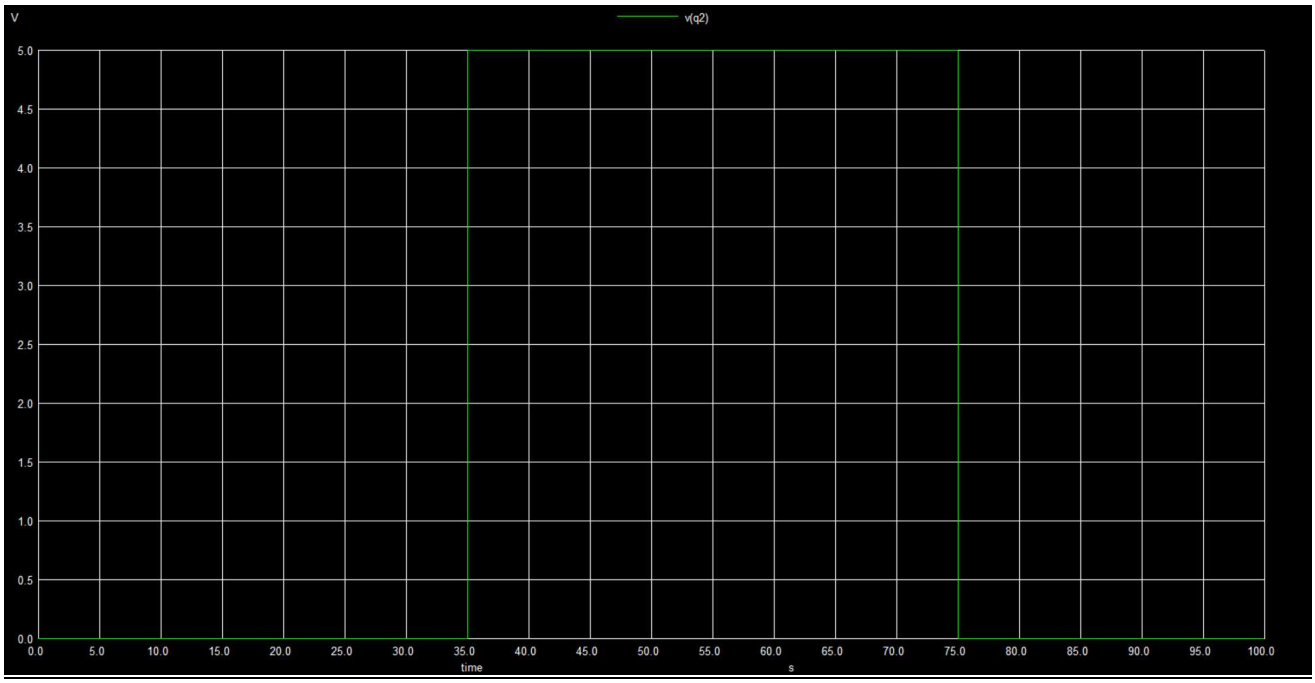
Q0:



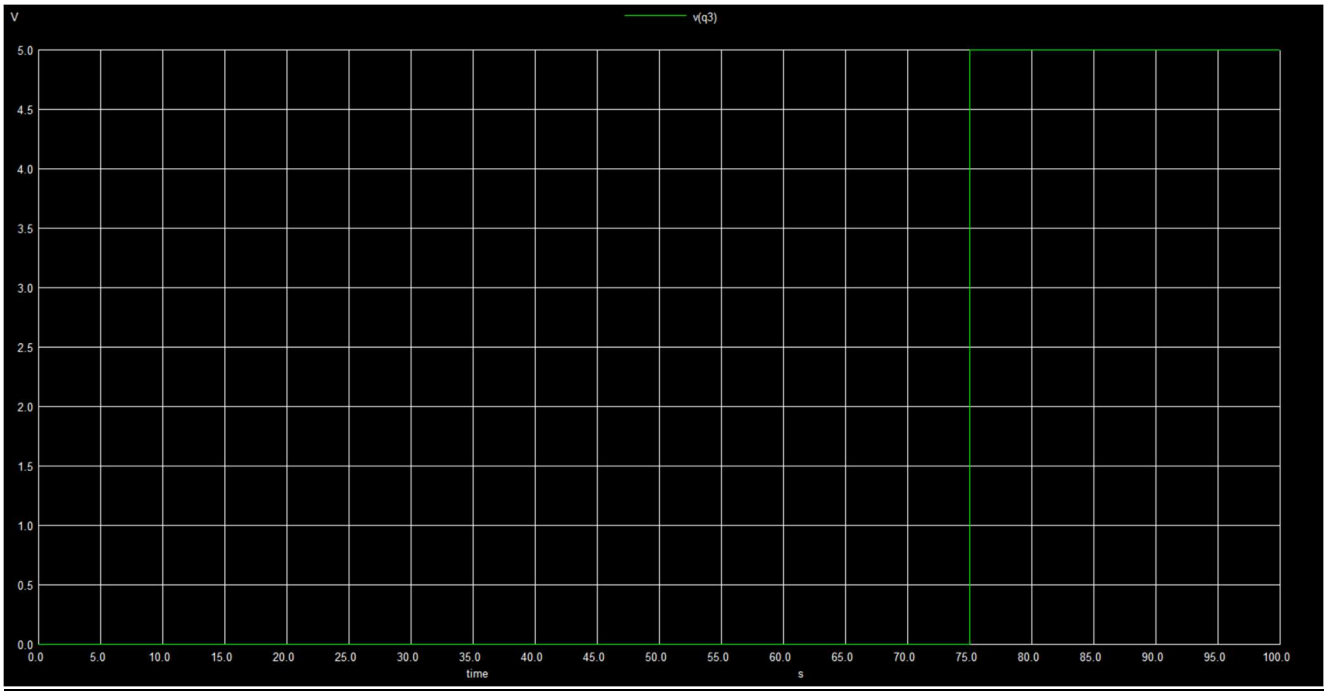
Q1:


V
v(q1)
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0.0 5.0 10.0 15.0 20.0 25.0 30.0 35.0 40.0 45.0 50.0 55.0 60.0 65.0 70.0 75.0 80.0 85.0 90.0 95.0 100.0
time
s

Q2:

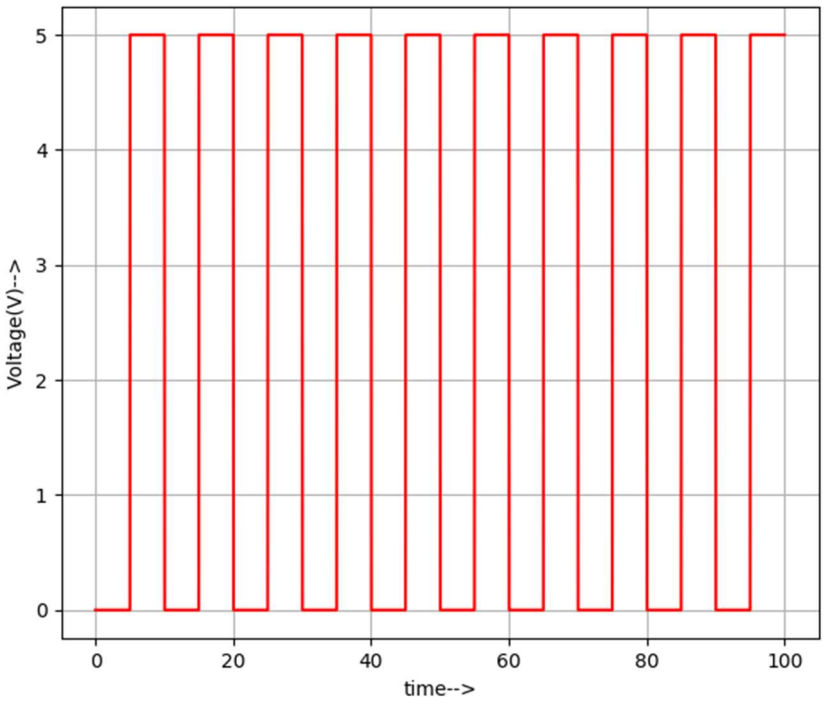

V
v(q2)
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0.0 5.0 10.0 15.0 20.0 25.0 30.0 35.0 40.0 45.0 50.0 55.0 60.0 65.0 70.0 75.0 80.0 85.0 90.0 95.0 100.0
time
s

Q3:

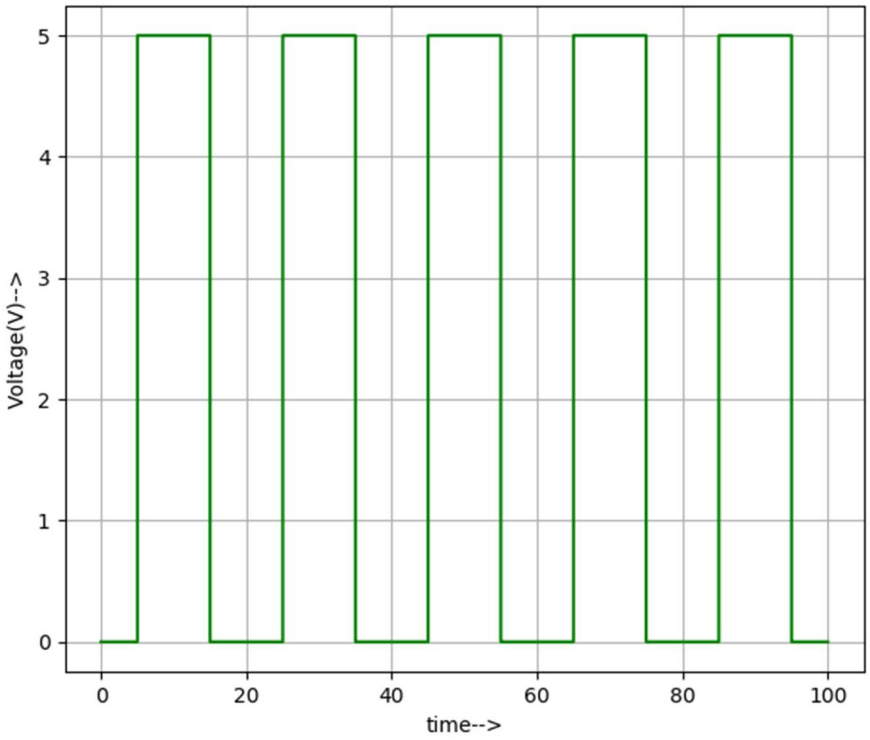


PYTHON;

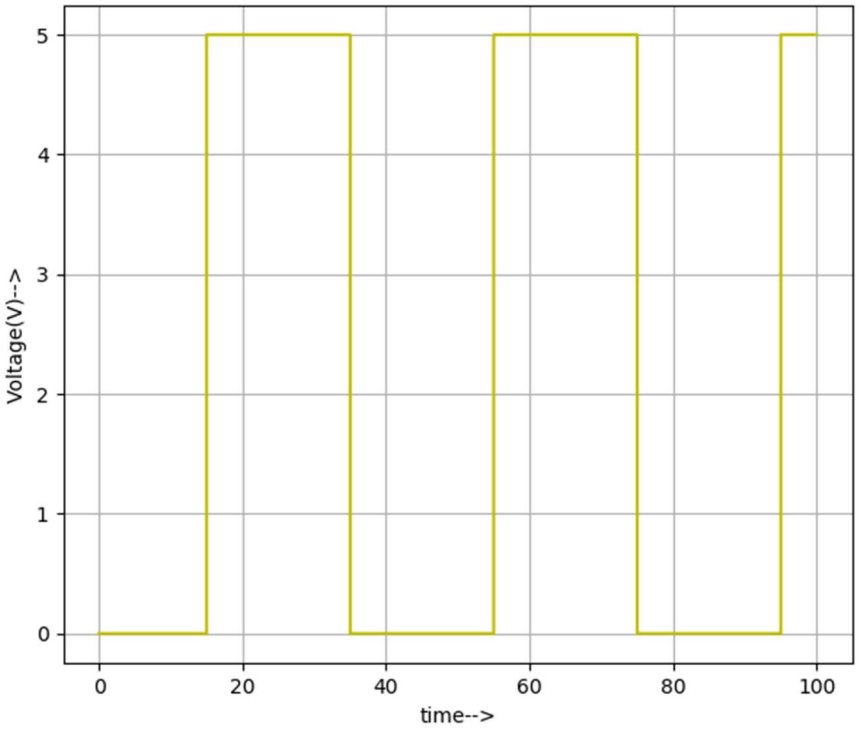
CLK:



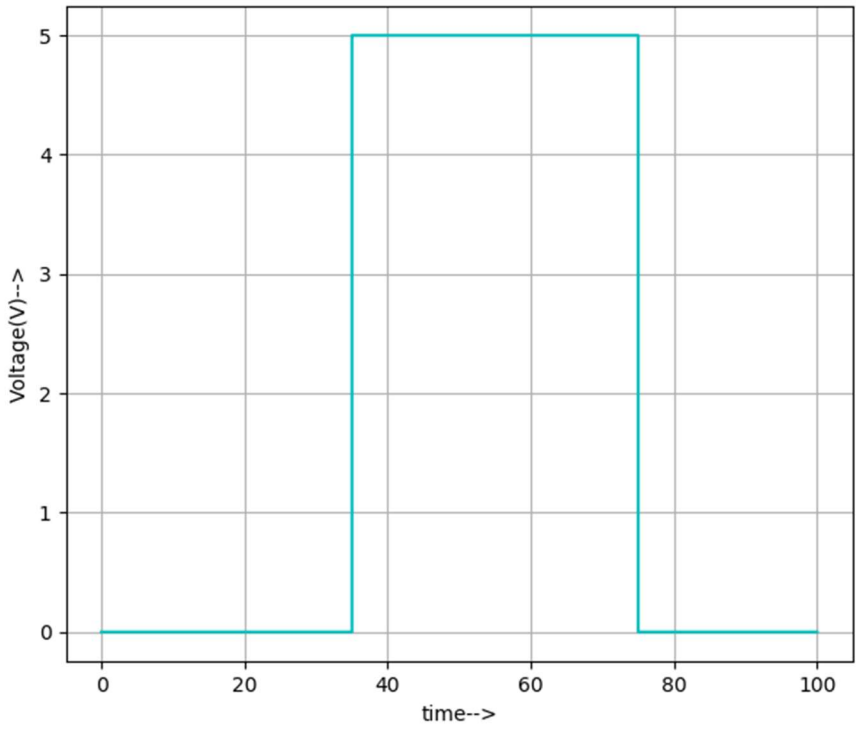
Q0:


Voltage(V)-->
time-->
0
1
2
3
4
5
0
20
40
60
80
100

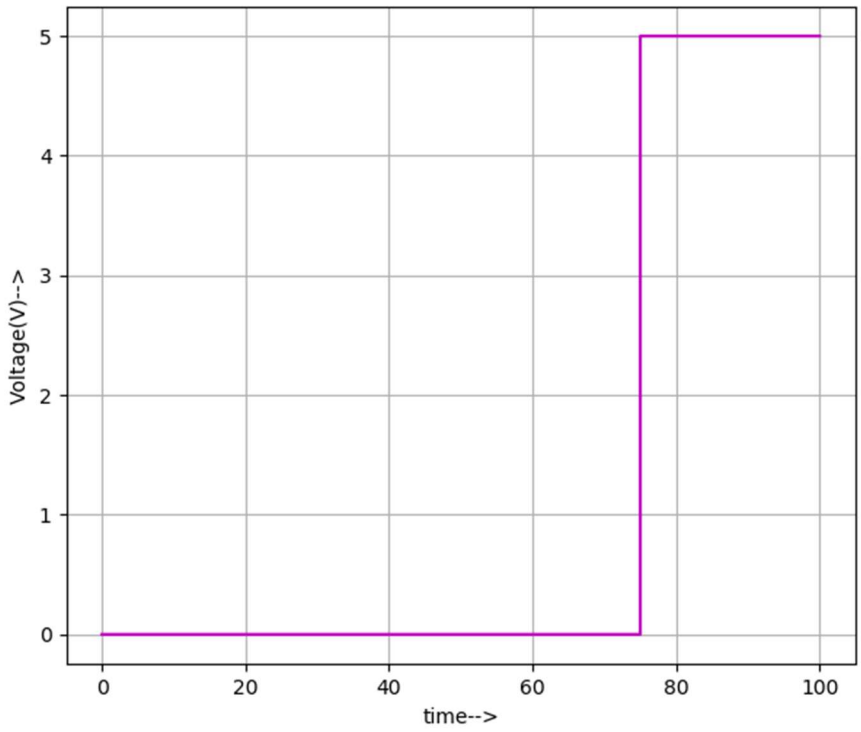
Q1:


Voltage(V)-->
time-->
0
1
2
3
4
5
0
20
40
60
80
100

Q2:


Voltage(V)-->
time-->
0
1
2
3
4
5
0
20
40
60
80
100

Q3:


Voltage(V)-->
time-->
0
1
2
3
4
5
0
20
40
60
80
100

REFERENCES:

https://www.electronicshub.org/asynchronous-counter/#:~:text=A%204%20bit%20asynchronous%20UP,output%20of%20the%20flip%20flop.