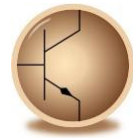




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Circuit Simulation

Project

<https://esim.fossee.in/circuit-simulation-project>

Name of the participant :- Krishna Kumar

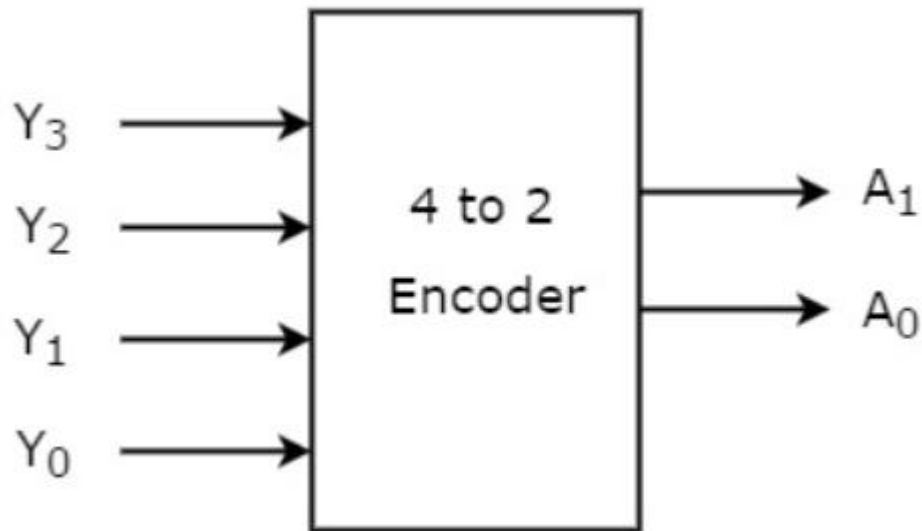
Project Guide :- Dr. Maheswari.R

Institute :- Vellore Institute of Technology, Chennai

Topic :- 4 TO 2 Encoder

Theory :- An **Encoder** is a combinational circuit that performs the reverse operation of Decoder. It has maximum of 2^n input lines and 'n' output lines. It will produce a binary code equivalent to the input, which is active High. Therefore, the encoder encodes 2^n input lines with 'n' bits. It is optional to represent the enable signal in encoders.

Let 4 to 2 Encoder has four inputs Y_3 , Y_2 , Y_1 & Y_0 and two outputs A_1 & A_0 . The **block diagram** of 4 to 2 Encoder is shown in the following figure.



At any time, only one of these 4 inputs can be '1' in order to get the respective binary code at the output. The **Truth table** of 4 to 2 encoder is shown below.

Truth Table:-

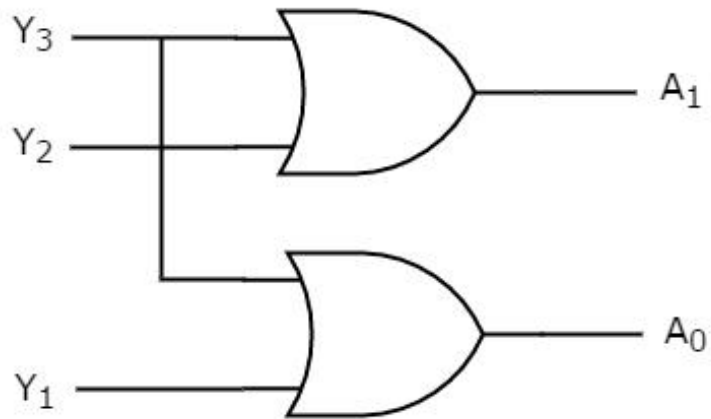
Inputs				Outputs	
Y_3	Y_2	Y_1	Y_0	A_1	A_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

From Truth table, we can write the **Boolean functions** for each output as

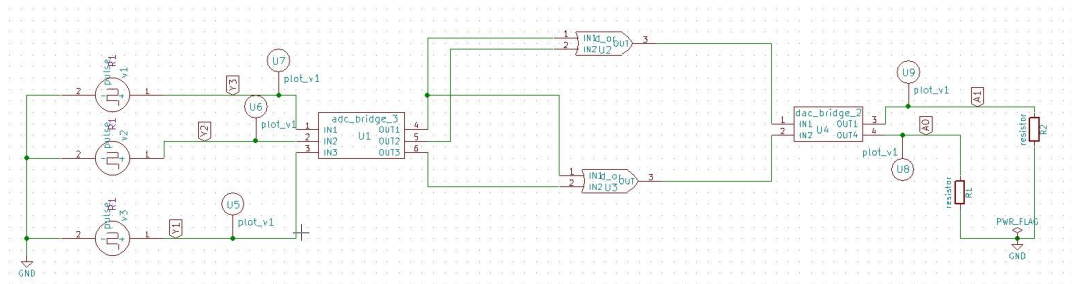
$$A_1 = Y_3 + Y_2$$

$$A_0 = Y_3 + Y_1$$

Circuit Diagram :-

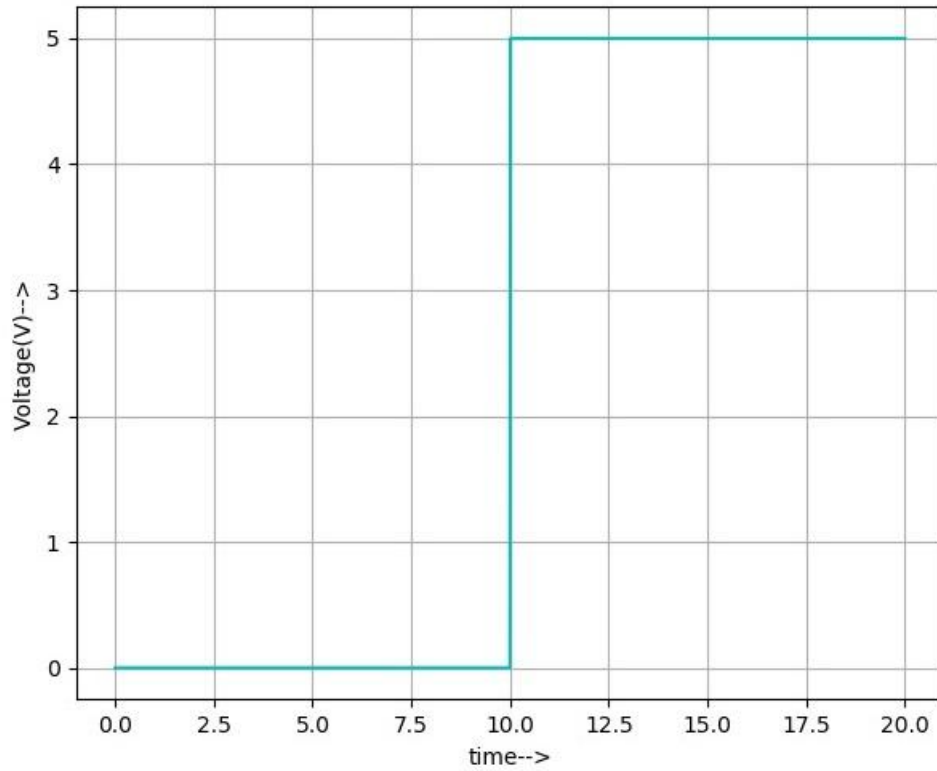


Schematic Diagram (ESim Implementation)

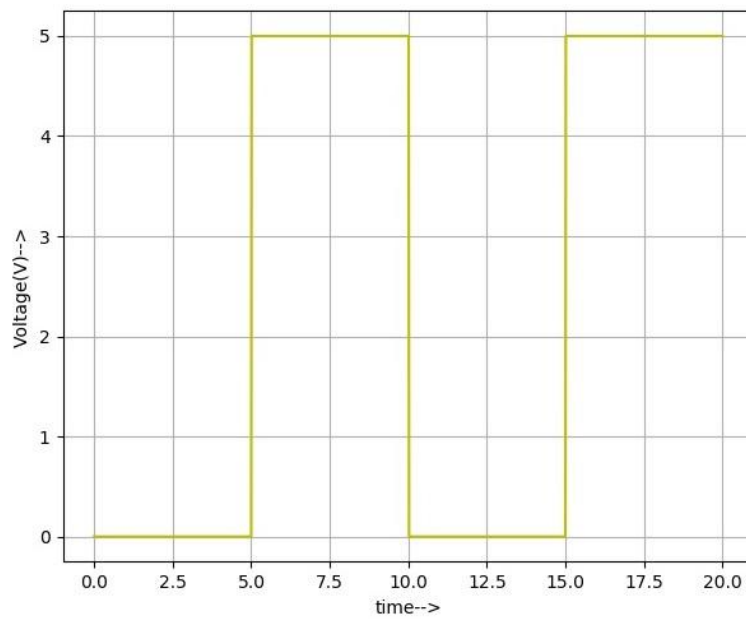


Simulation Plots :-

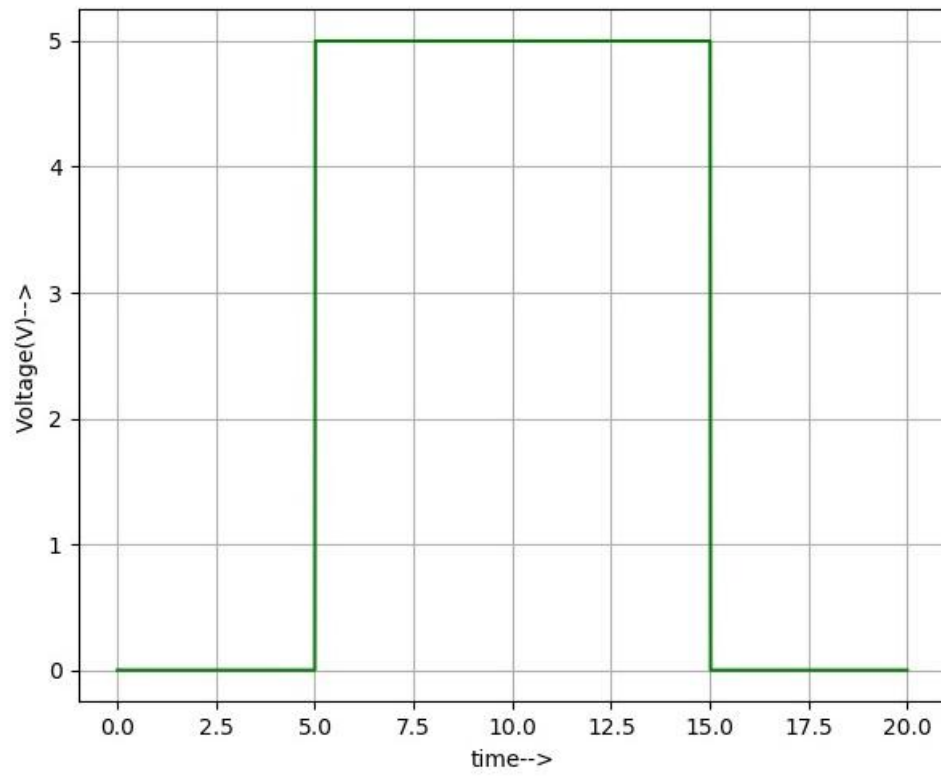
1) Y3



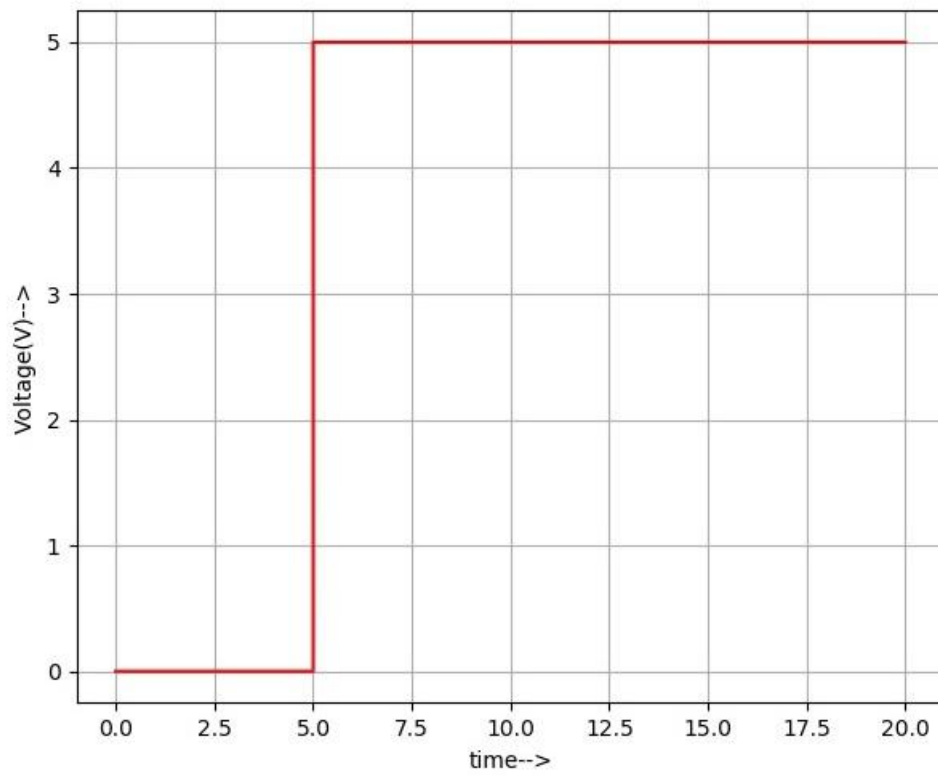
2) Y2



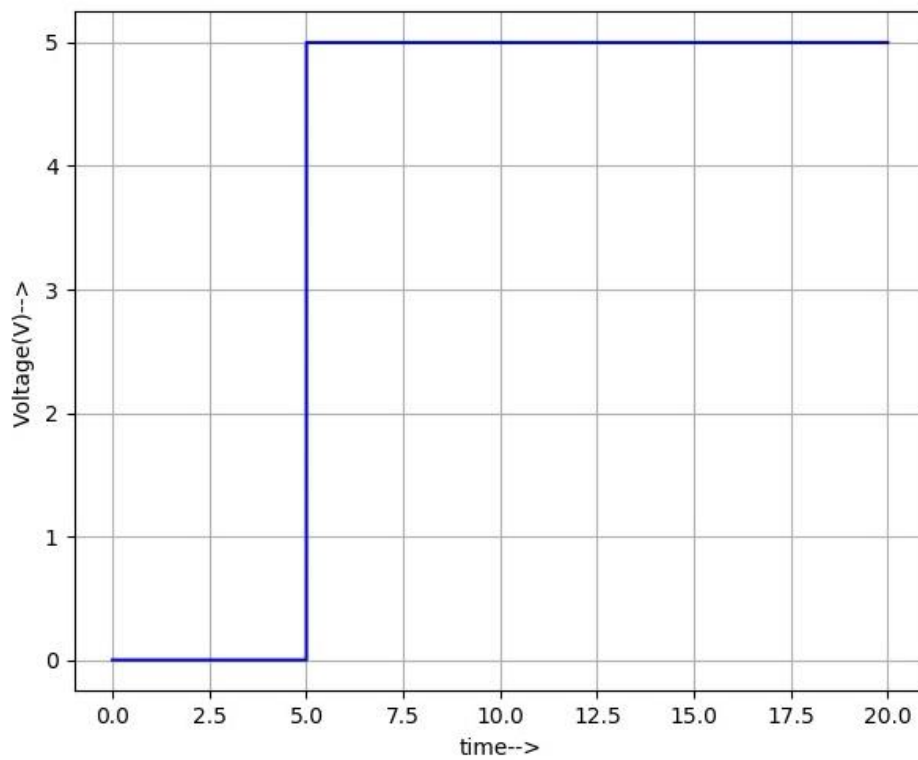
3) Y1



4) A0



5) A1



Conclusion: Using the circuit simulated, we have studied the logic and output of 4 to 2 Encoder circuit. The results simulated follow the truth table, thus validating the correctness of the circuit simulated.

References :-

https://www.tutorialspoint.com/digital_circuits/digital_circuits_encoders.htm