CIRCUIT SIMULATION PROJECT

https://esim.fossee.in/circuit-simulation-project

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Project Guide: Dr. Maheswari. R

Title of the circuit:

2 - BIT MAGNITUDE COMPARATOR

THEORY/DESCRIPTION:

A magnitude digital Comparator is a combinational circuit that compares two digital or binary numbers to find out whether one binary number is equal, less than or greater than the other binary number.

A comparator used to compare two binary numbers each of two bits is called a 2-bit Magnitude comparator. It consists of four inputs and

three outputs to generate less than, equal to and greater than between two binary numbers.

The truth table for a 2-bit comparator is given below:

INPUT				OUTPUT		
A1	A0	B1	B0	A<B	A=B	A>B
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

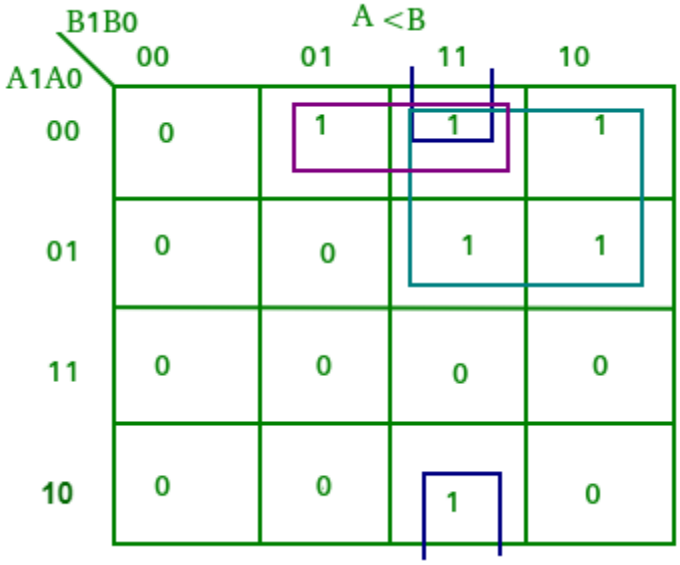
From the above truth table K-map for each output can be drawn as follows:

A>B

A1A0 \ B1B0	00	01	11	10
00	0	0	0	0
01	1	0	0	0
11	1	1	0	1
10	1	1	0	0

A =B

A1A0 \ B1B0	00	01	11	10
00	1	0	0	0
01	0	1	0	0
11	0	0	1	0
10	0	0	0	1



From the above K-maps logical expressions for each output can be expressed as follows:

A>B: A1B1’ + A0B1’B0’ + A1A0B0’

A=B: A1’A0’B1’B0’ + A1’A0B1’B0 + A1A0B1B0 + A1A0’B1B0’

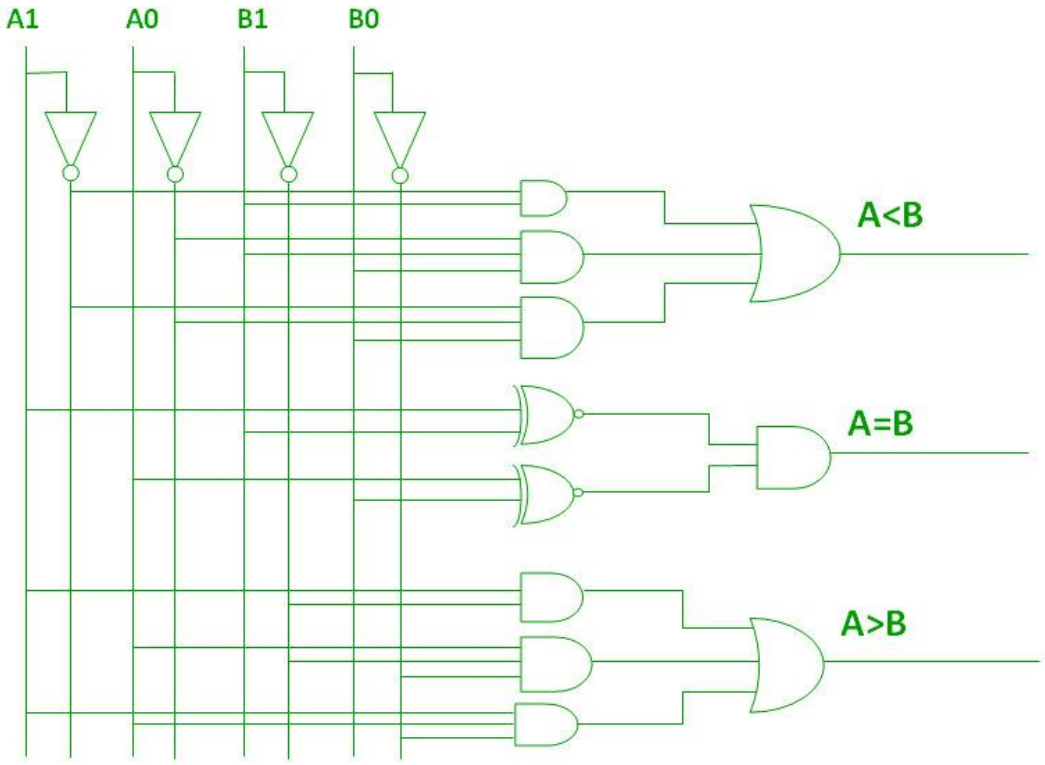
: A1’B1’ (A0’B0’ + A0B0) + A1B1 (A0B0 + A0’B0’)

: (A0B0 + A0’B0’) (A1B1 + A1’B1’)

: (A0 Ex-nor B0) (A1 Ex-nor B1)

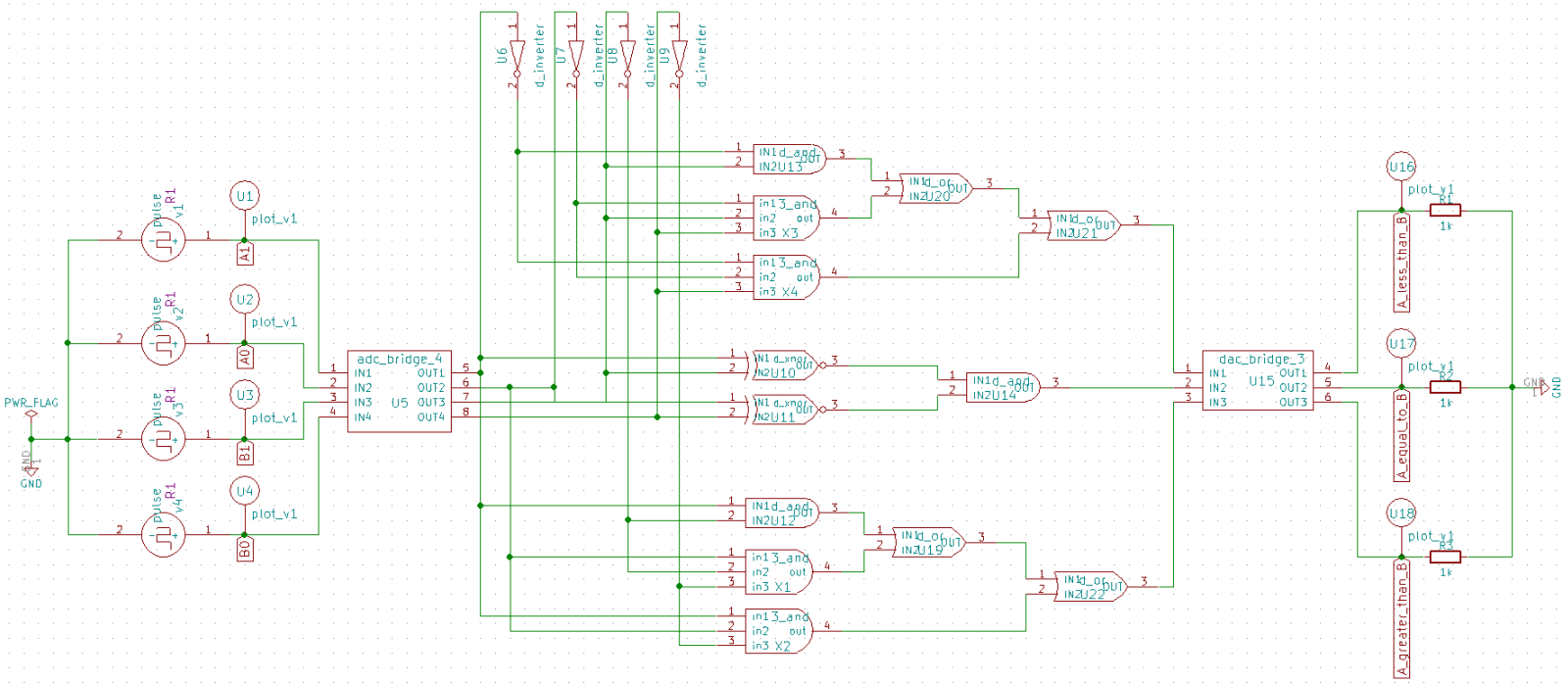
A<B: A1’B1 + A0’B1B0 + A1’A0’B0

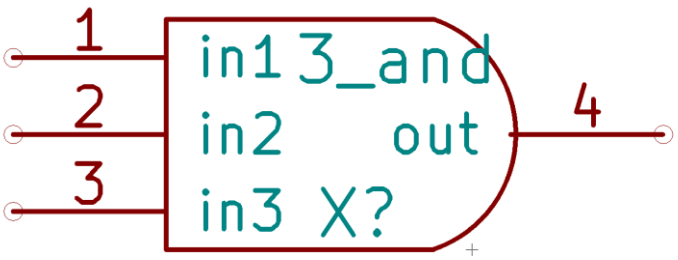
By using these Boolean expressions, we can implement a logic circuit for this comparator as given below:



ESIM CIRCUIT DIAGRAM FOR 2 - BIT MAGNITUDE

COMPARATOR :



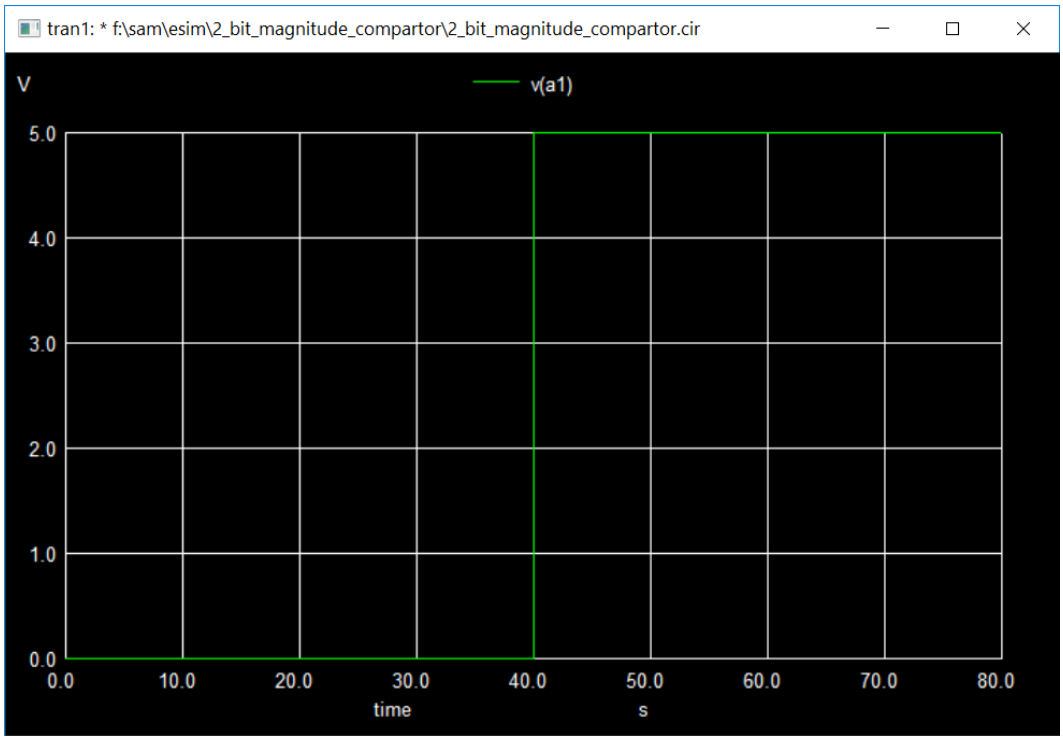


Subcircuit Symbol for 3-Input AND Gate (already exists in eSim_Subckt)

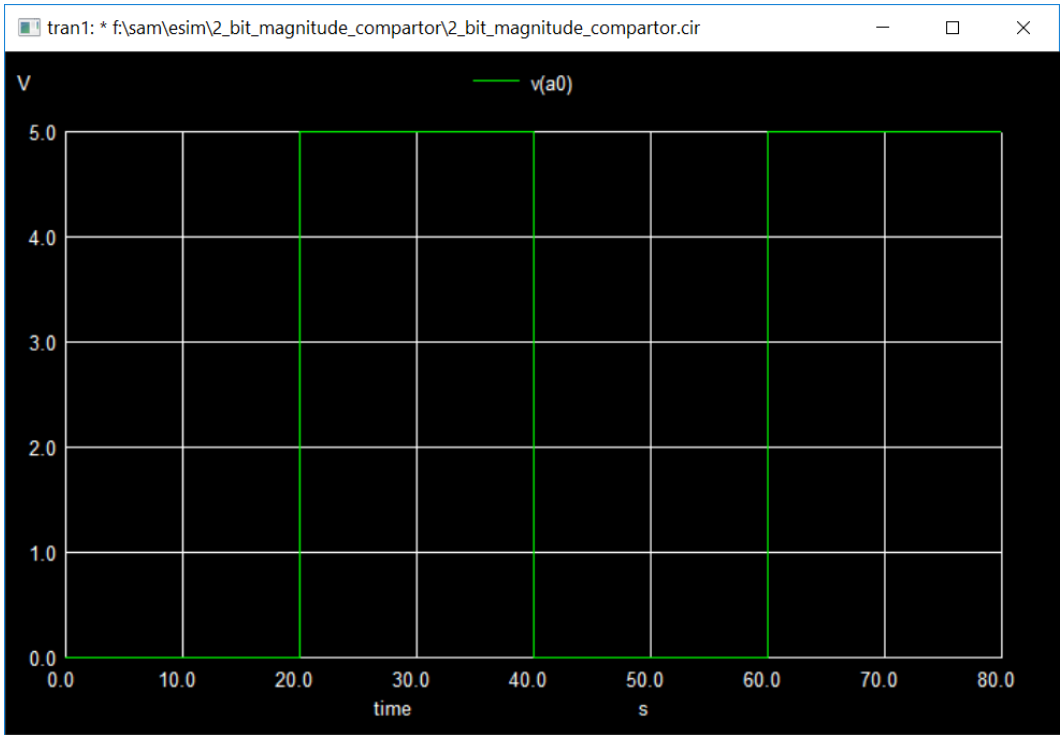
RESULT/OUTPUT:

- **NGSPICE PLOTS:**

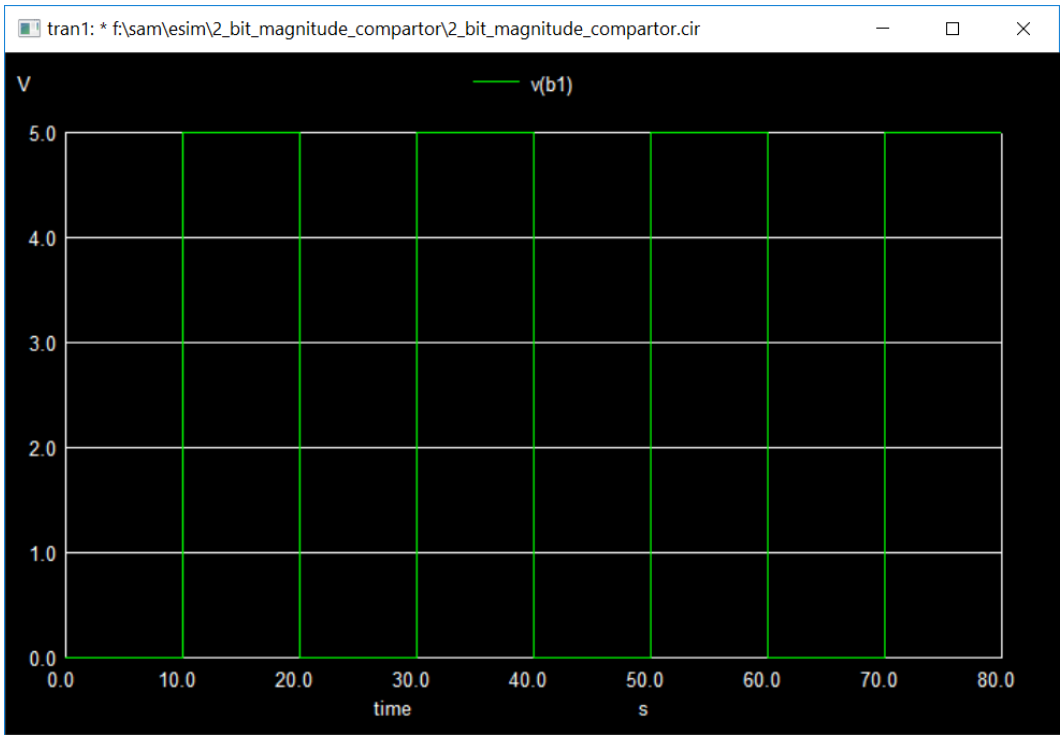
  INPUTS:



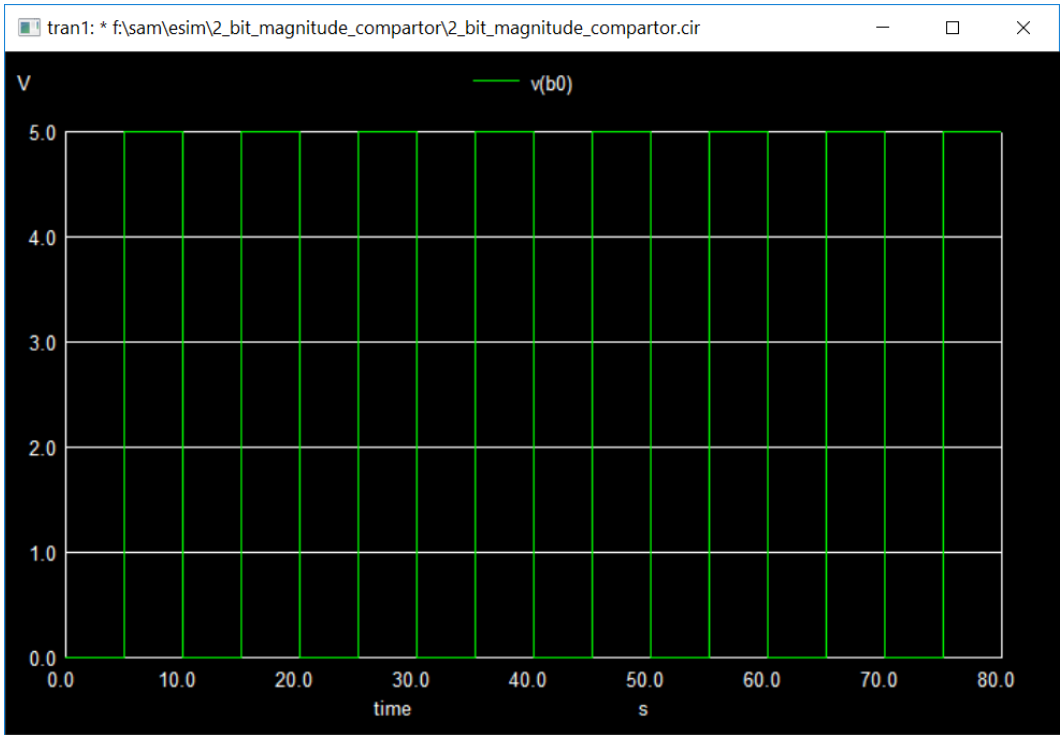
A1


tran1: * f:\sam\esim\2_bit_magnitude_compartor\2_bit_magnitude_compartor.cir
V
v(a0)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
time
s

A0

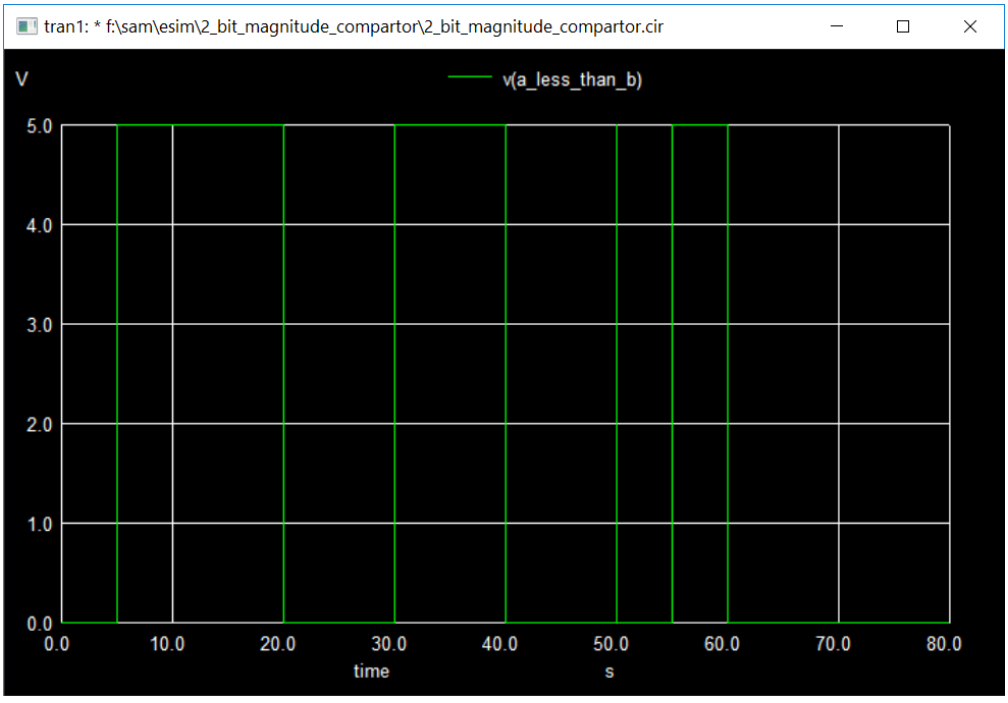

tran1: * f:\sam\esim\2_bit_magnitude_compartor\2_bit_magnitude_compartor.cir
V
v(b1)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
time
s

B1

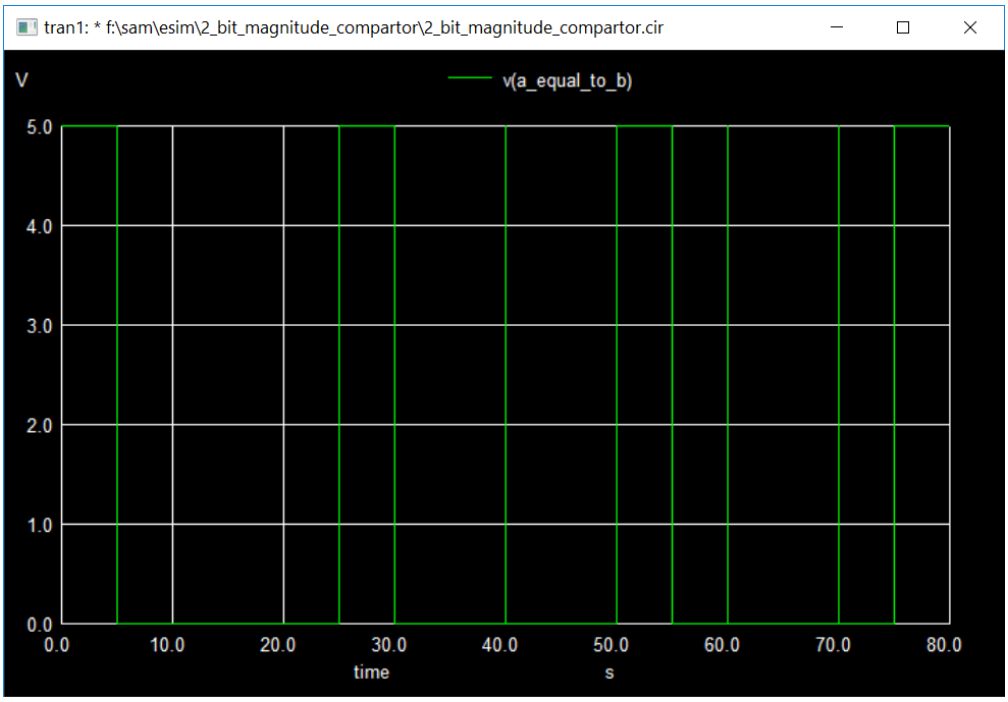


B0

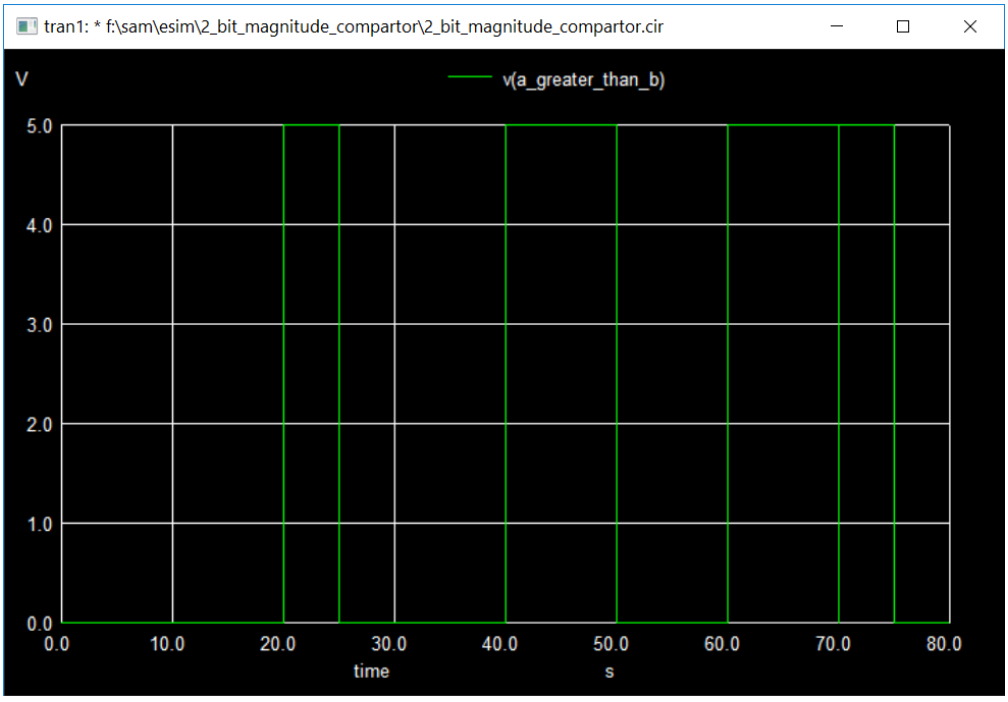
OUTPUTS:



A < B


tran1: * f:\sam\esim\2_bit_magnitude_compartor\2_bit_magnitude_compartor.cir
V
v(a_equal_to_b)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
time
s

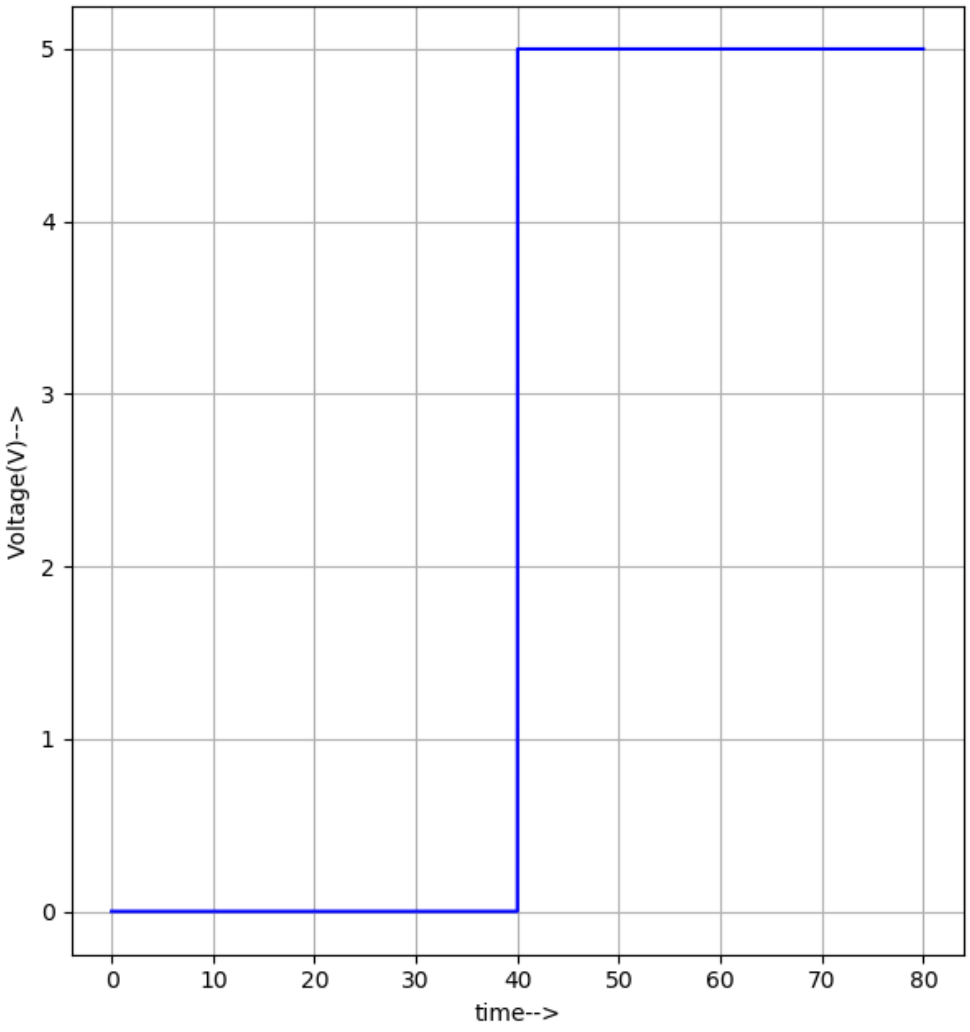
A = B


tran1: * f:\sam\esim\2_bit_magnitude_compartor\2_bit_magnitude_compartor.cir
V
v(a_greater_than_b)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
time
s

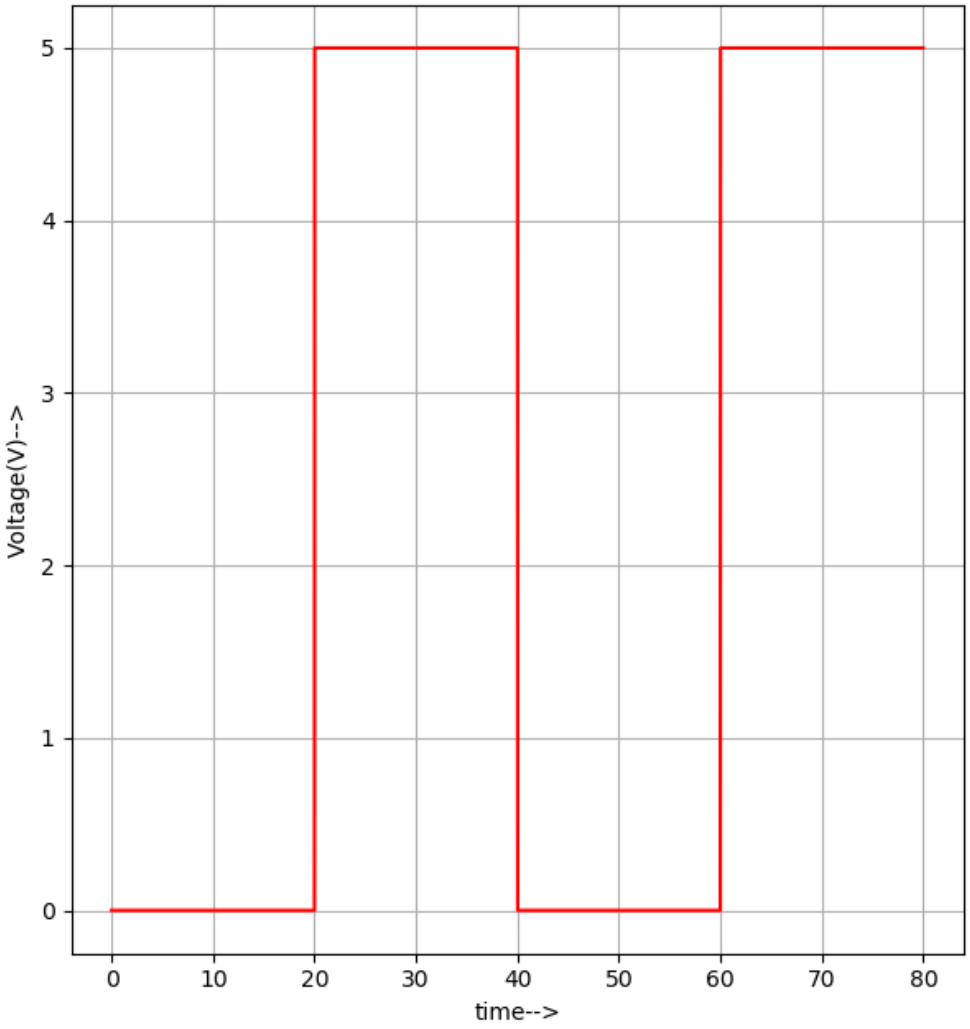
A > B

- **PYTHON PLOTS:**

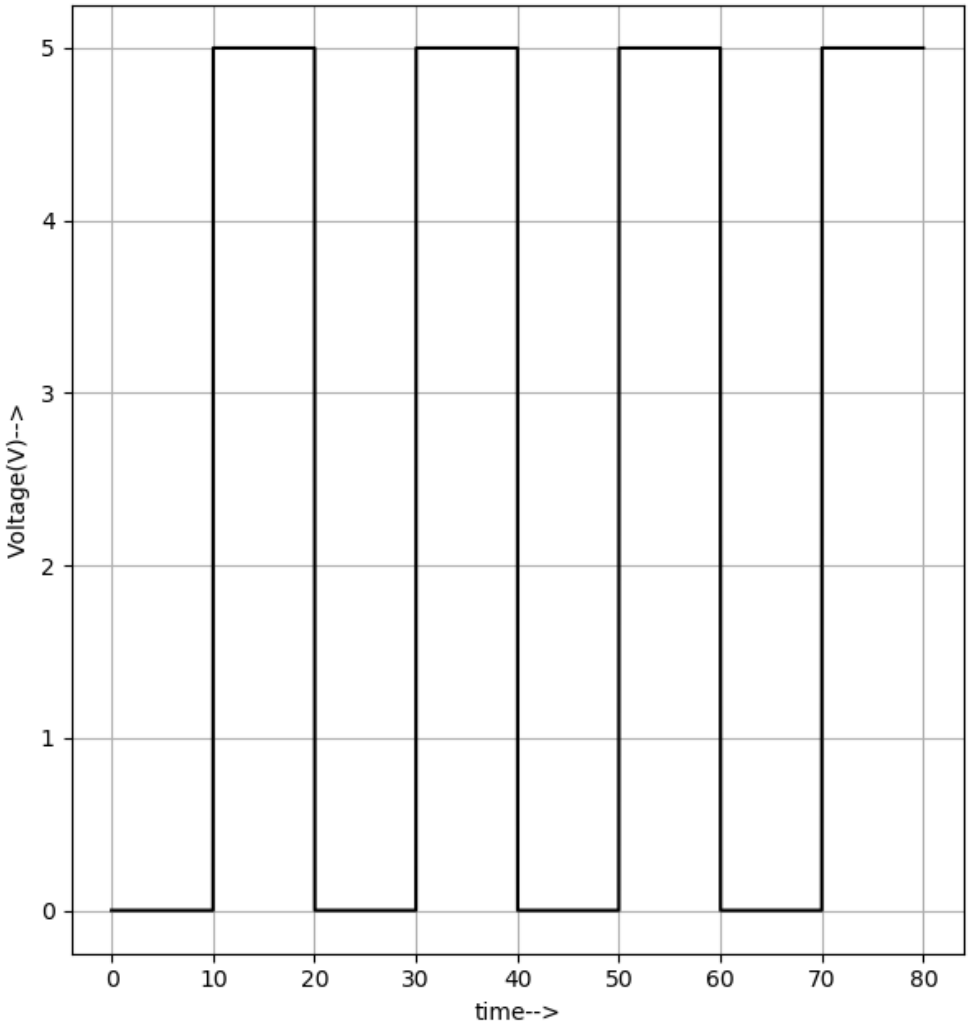
  INPUTS:



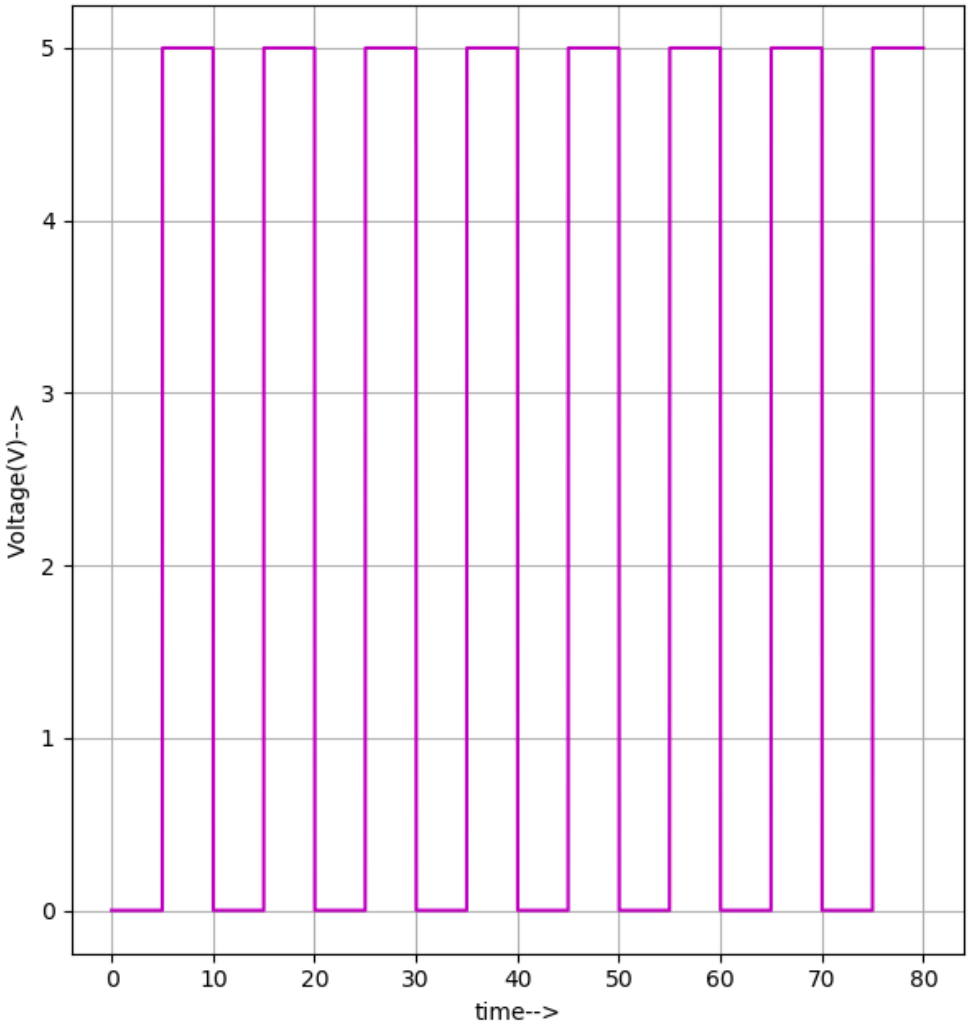
A1



A0

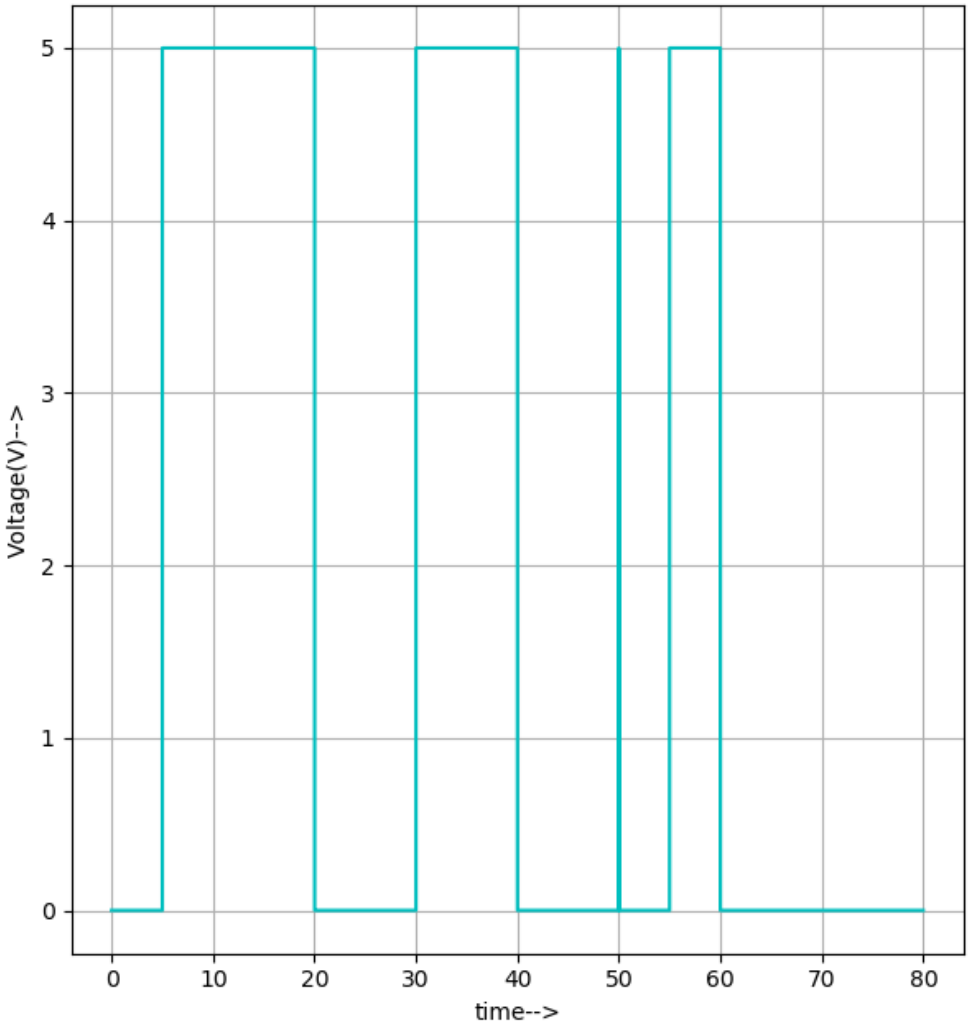


B1

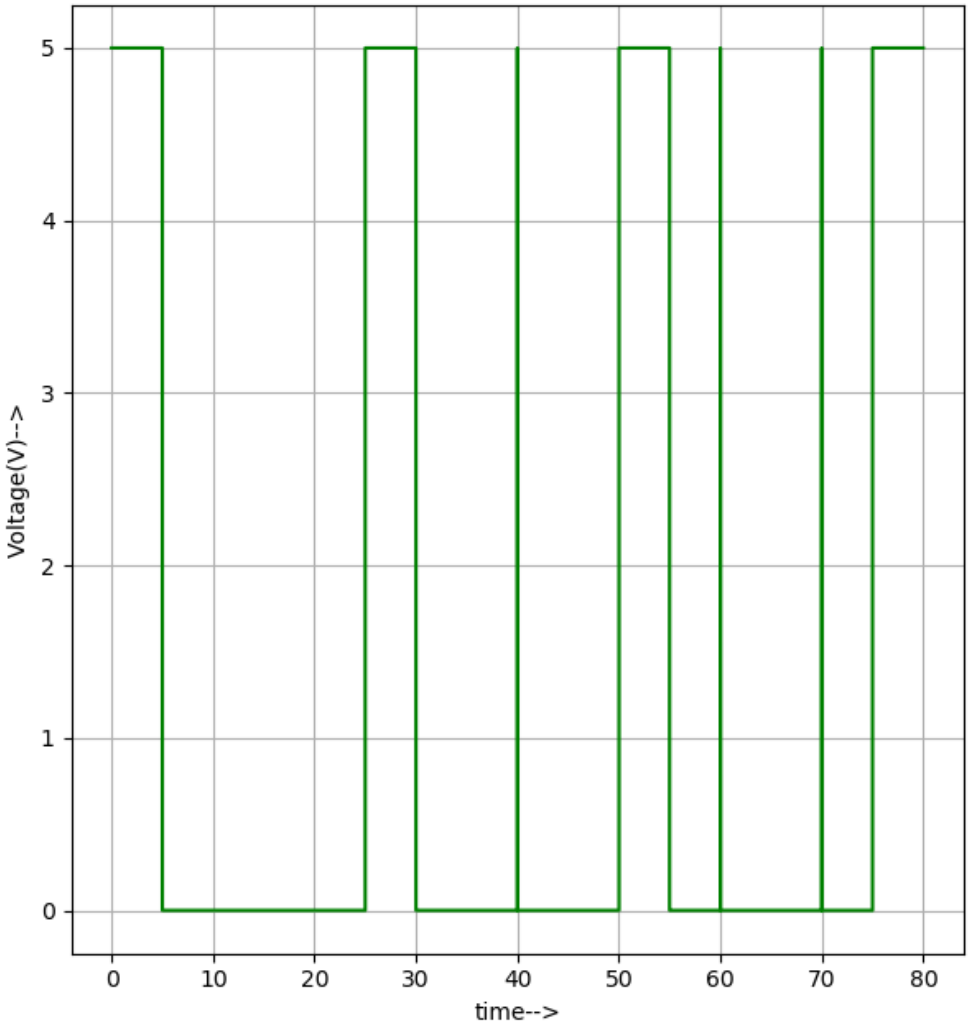


B0

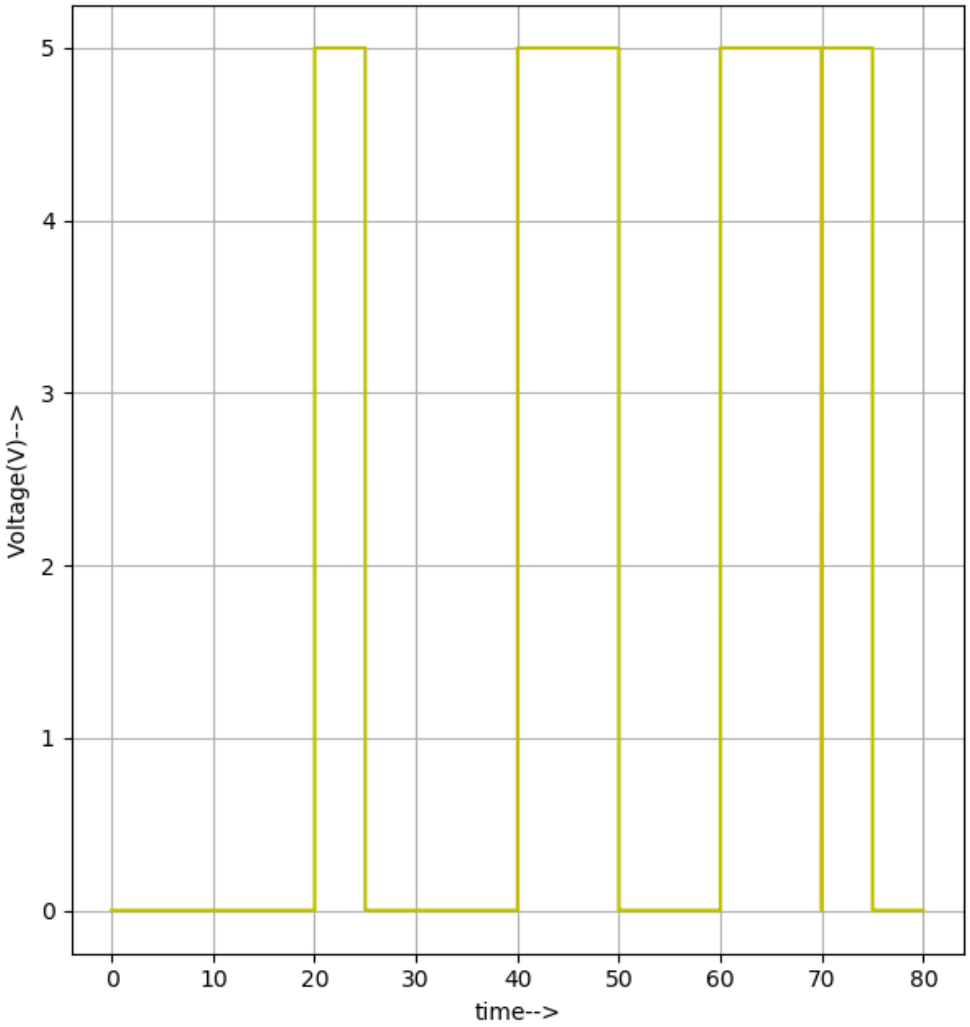
OUTPUTS:



A < B



A = B



A > B

Source/Reference(s):

https://www.geeksforgeeks.org/magnitude-comparator-in-digital-logic/