Circuit Simulation Project

https://esim.fossee.in/circuit-simulation-project

Name of the participant: Arjun Vishanth

Project Guide: Dr. R. Maheswari

Title of the Project: SR flip flop using NAND gates

Theory & Description:

The SR flip flop is a 1-bit memory bistable device having two inputs, i.e. SET and RESET. The SET input ‘S’ sets the device or produces the output 1, and the RESET input ‘R’ resets the device or produces the output 0.

The SR flip flop stands for ‘Set-Reset’ flip flop. The reset input is used to get back the flip flop to its original state from the current state with an output ‘Q’. This output depends on the set and reset conditions, which is either at the logic level “0” or “1”.

The NAND gate SR flip flop is a basic flip flop which provides feedback from both of its outputs back to its opposing input. This circuit is used to store the single data bit in the memory circuit. So, the SR flip flop has a total of three inputs, i.e., 'S' and 'R', and current output 'Q'. This output 'Q' is related to the current history or state. The term "flip-flop" relates to the actual operation of the device, as it can be "flipped" to a logic set state or "flopped" back to the opposing logic reset state.

The Set state:

In the below diagram, when the input R is set to false or 0 and the input S is set to true or 1, the NAND gate U5 has an input 0, which will produce the output Q' 1. The value of Q' is faded to the NAND gate U4 as input 'A', and now both the inputs of the NAND gate U4 are 1(S=A=1), which will produce the output 'Q' 0.

Now, if the input R is changed to 1 with 'S' remaining 1, the inputs of NAND gate U5 is R=1 and B=0. Here, one of the inputs is also 0, so the output of Q' is 1. So, the flip flop circuit is set or latched with Q=0 and Q'=1.

Reset state:

The output Q' is 0, and output Q is 1 in the second stable state. It is given by R =1 and S = 0. One of the inputs of NAND gate U4 is 0, and its output Q is 1. Output Q is faded to NAND gate U5 as input B. So, both the inputs to NAND gate U5 are set to 1, therefore, Q' = 0.

Now, if the input S is changed to 0 with 'R' remaining 1, the output Q' will be 0 and there is no change in state. So, the reset state of the flip flop circuit has been latched, and the set/reset actions are defined in the following truth table:

Truth table:

State	S	R	Q	Q’	Description
Set	1	0	0	1	Set Q’ >> 1
	1	1	0	1	No change
Reset	0	1	1	0	Reset Q’ >> 0
	1	1	1	0	No change
Invalid	0	0	1	1	Invalid condition

Circuit Diagram:

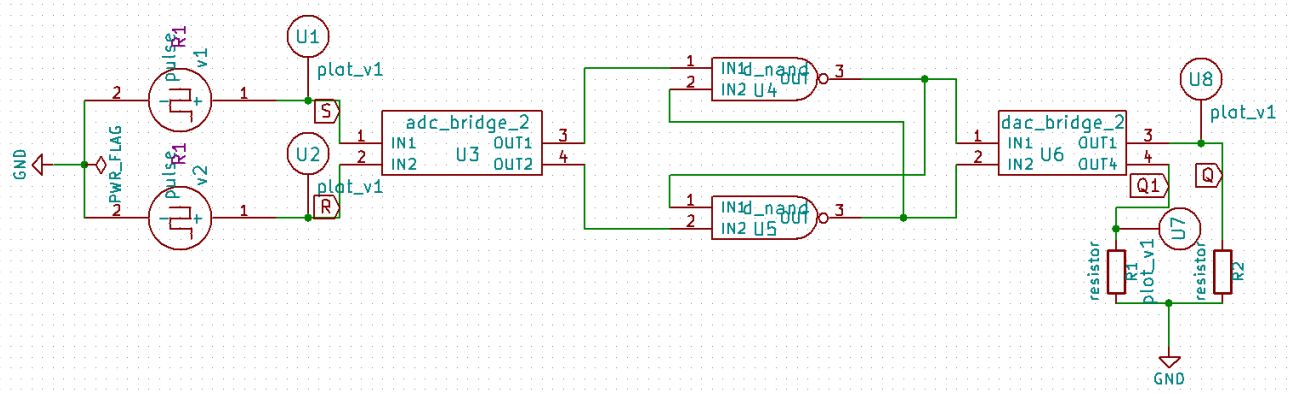

Fig. 1: NAND gates implementation of an SR flip flop

Fig. 1 represents the schematic for the circuit. The pulse sources feed the inputs from 0000 to 1111. The ADC bridge is used to convert the analog voltage source inputs into digital bits to be used with the digital gates. The DAC bridge is

used to convert the digital signals back to analog so that they can be plotted and viewed as output.

Results (Input, Output waveforms):

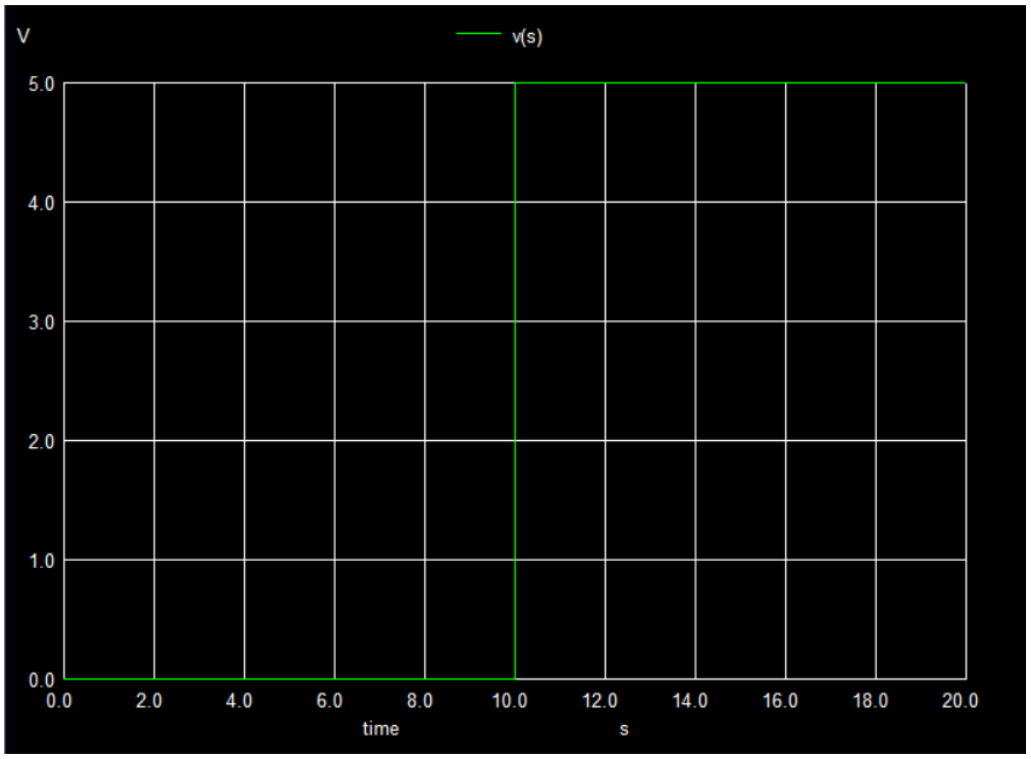

Fig. 2a: Analog signal for S (Set state)

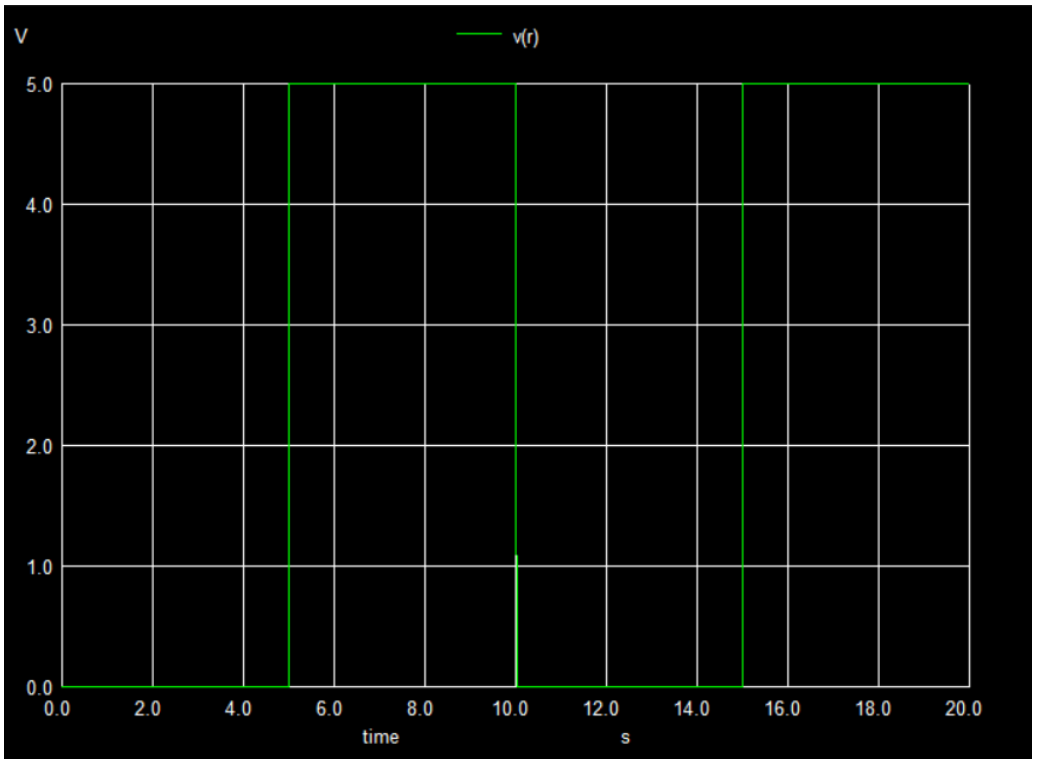

Fig. 2b: Analog signal for R (Reset state)

Figures 2a and 2b show the analog signals for the input bits (S and R).

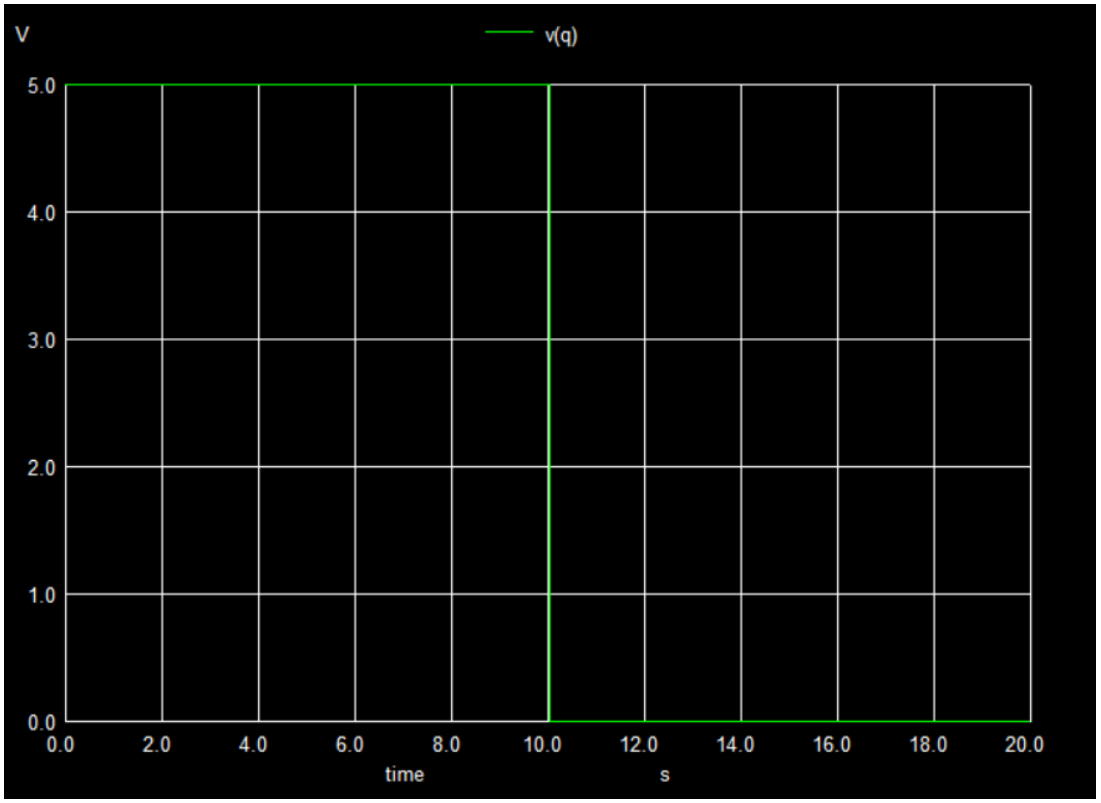

Fig. 3a: Analog signal for Q

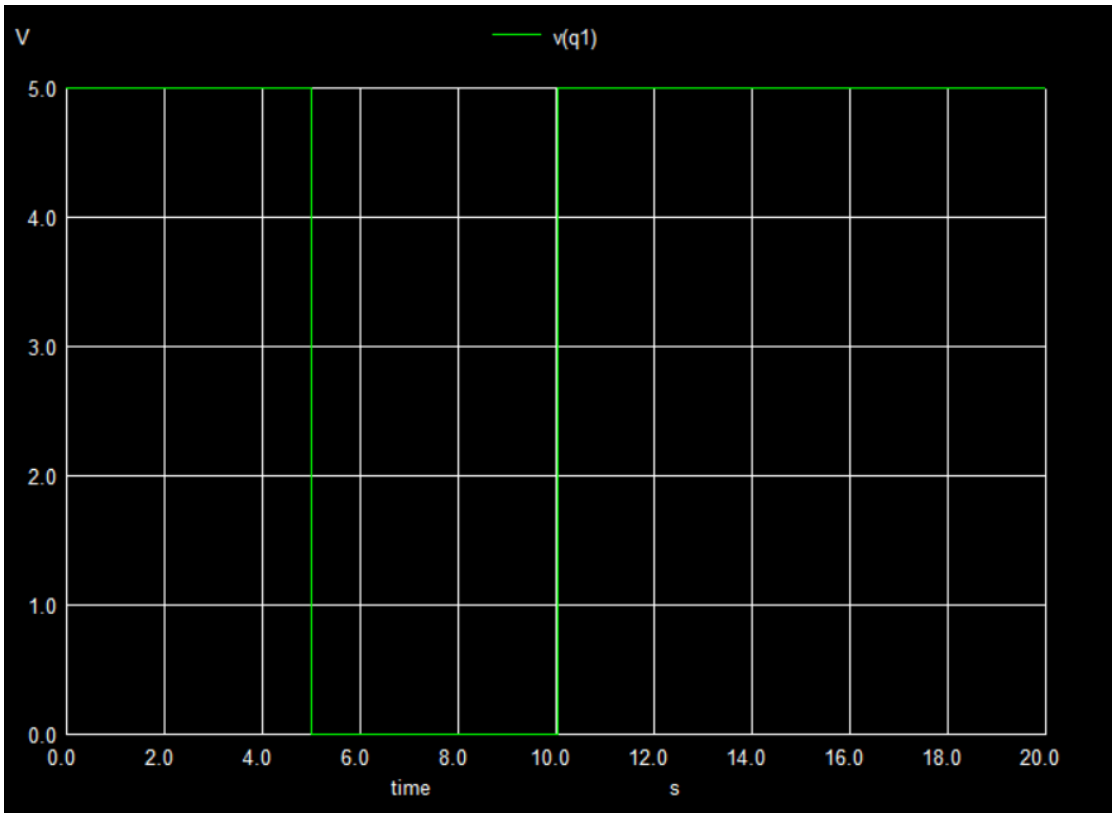

Fig. 3b: Analog signal for Q'

Figures 3a and 3b show the output analog signals for the output bits (Q and Q').

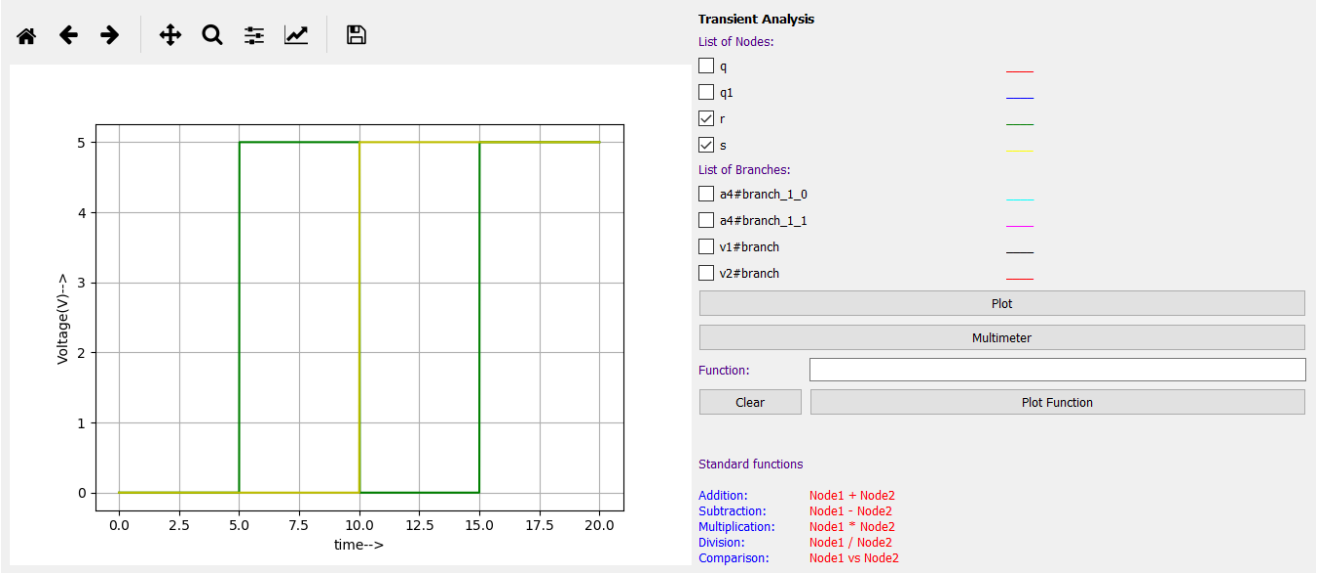

Fig. 4a: Python plots for S and R

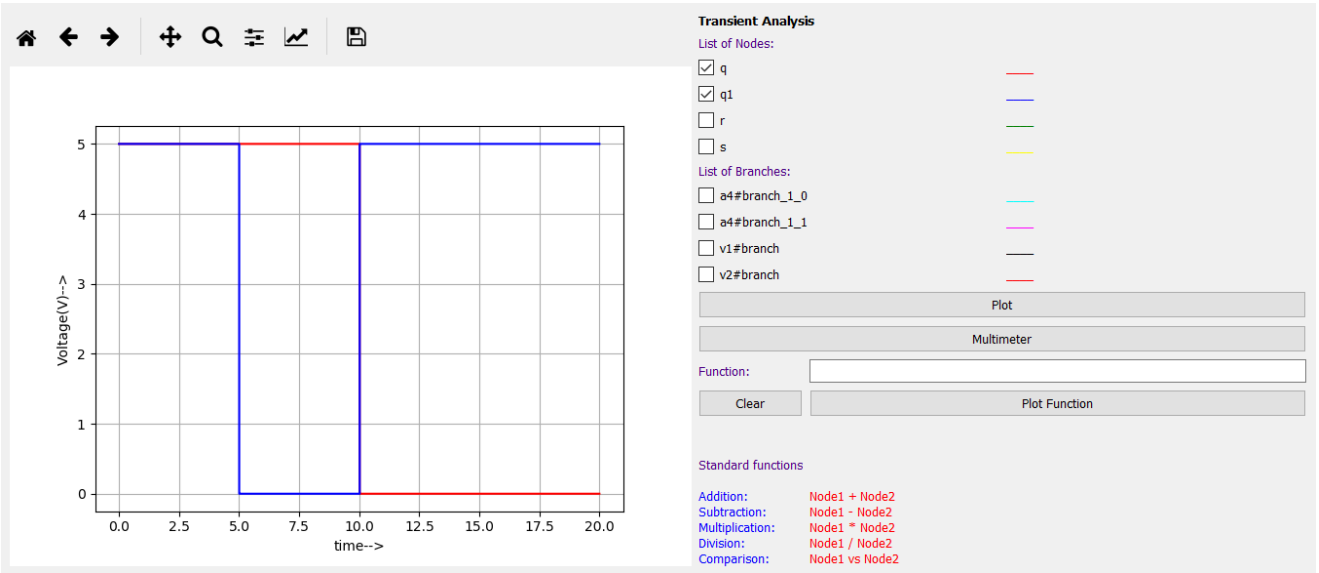

Fig. 4b: Python plots for Q and Q'

Figures 4a and 4b show the python plots for the same signals for better visualisation.

Simulation parameters for reference:

Fig. 5a

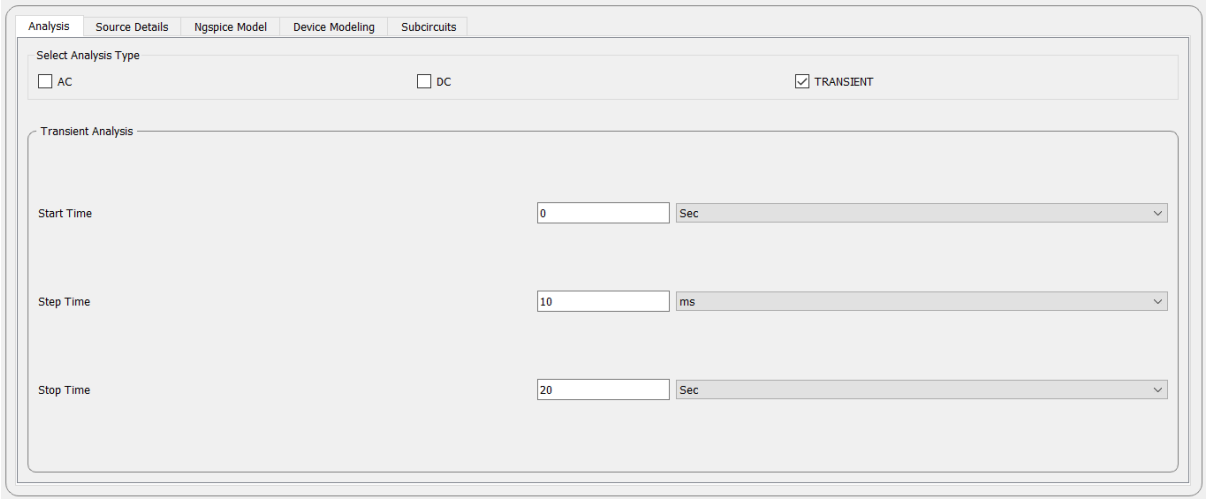

Fig. 5b

Source / Reference:

https://www.javatpoint.com/sr-flip-flop-in-digital-electronics