Title of the Experiment:

Construction and working of a Full Adder using 3x8 decoder.

Theory:

A full adder circuit takes three inputs and gives two outputs. It provides the sum and carry and is implemented using a 3x8 decoder in our circuit.

We give our 3 pulse inputs to the 3x8 decoder. We came to the conclusion that

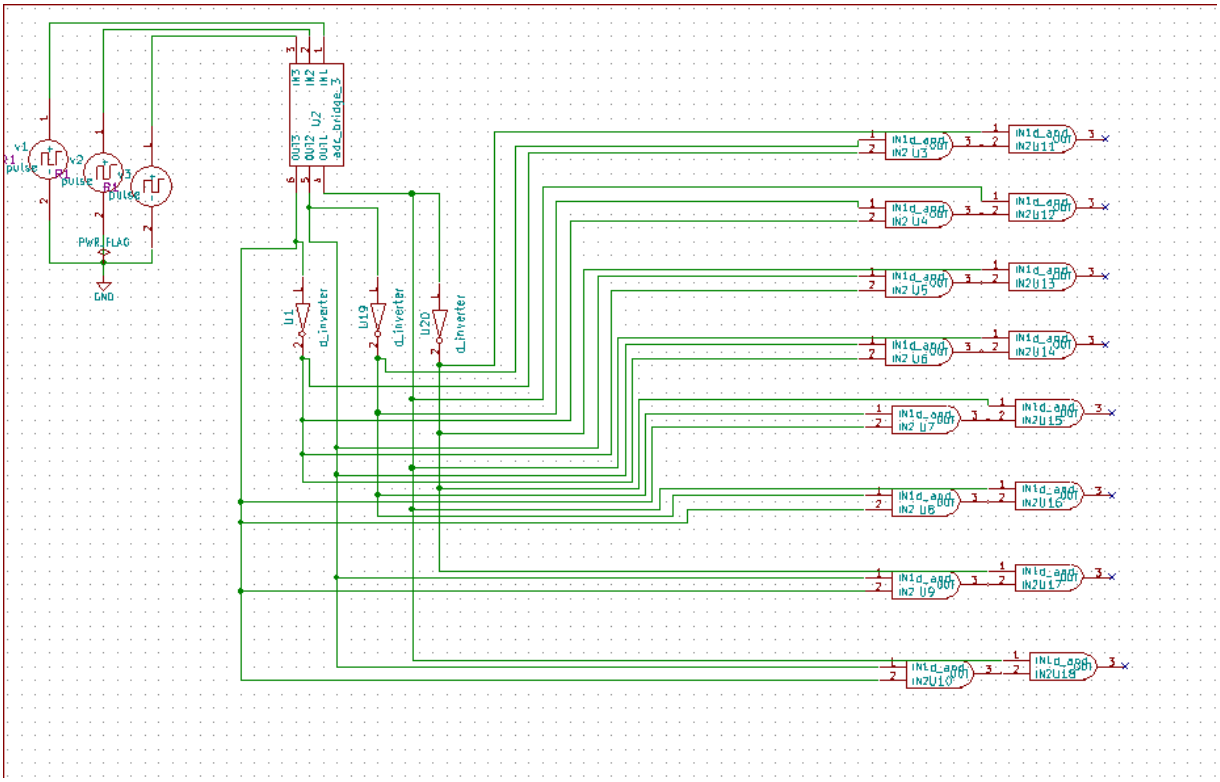
Sum=Σm(1,2,4,7)

Carry=Σm(3,5,6,7)

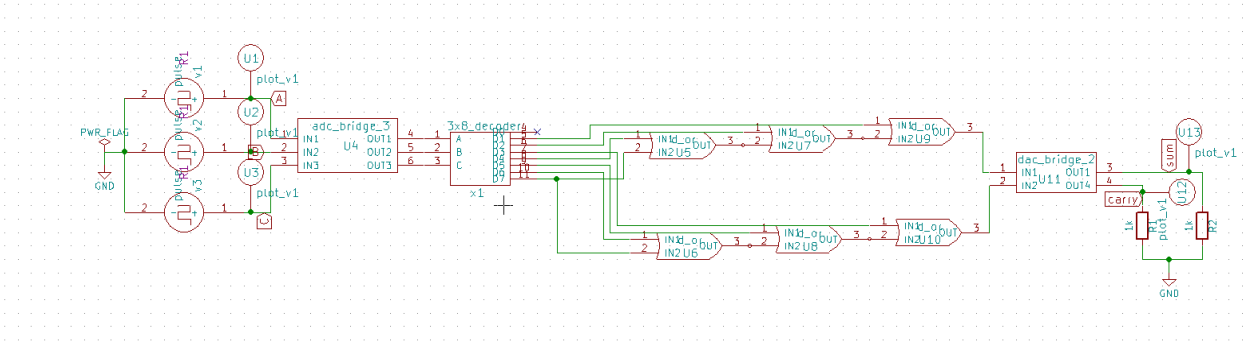
Our final sum will be the OR operation of 2^{nd},3^{rd},5^{th} and 8^{th} output of our decoder and final carry will be the OR operation of 4^{th},6^{th},7^{th} and 8^{th} output of the decoder.

Schematic Diagram:

3x8 decoder schematic:



Full adder using 3x8 decoder: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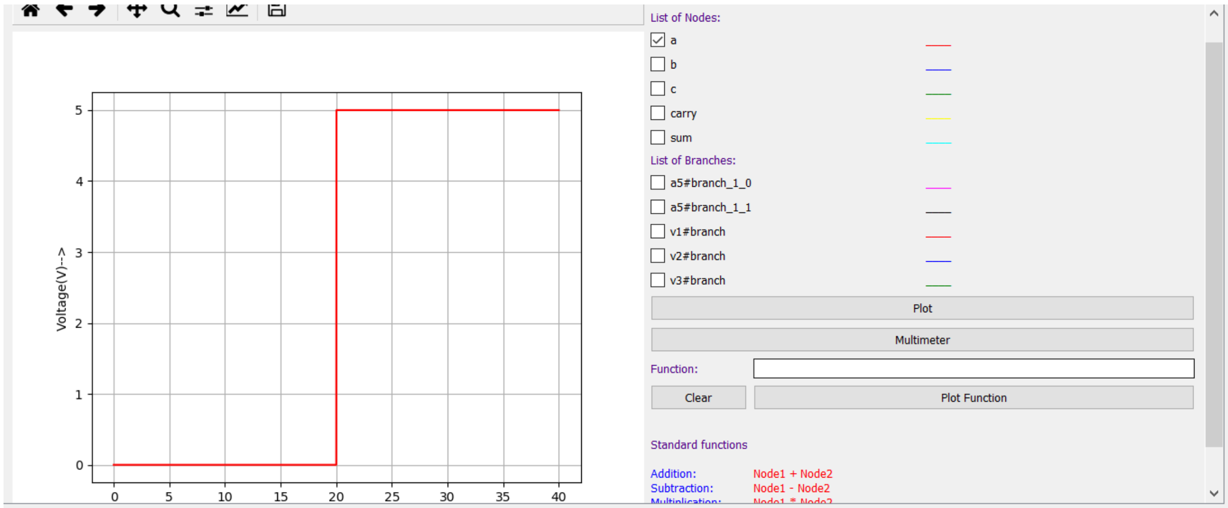
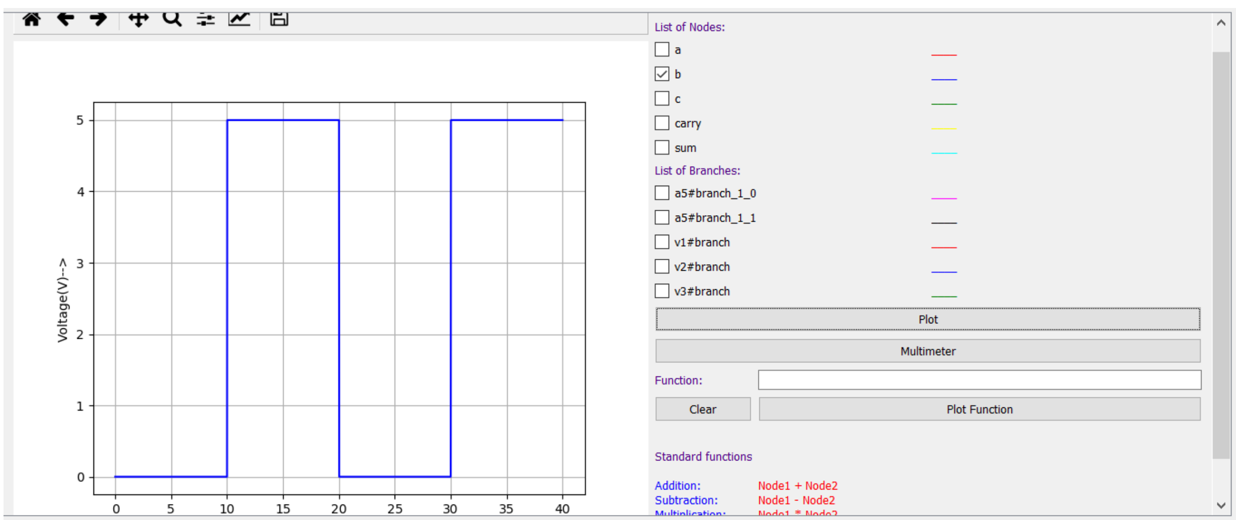
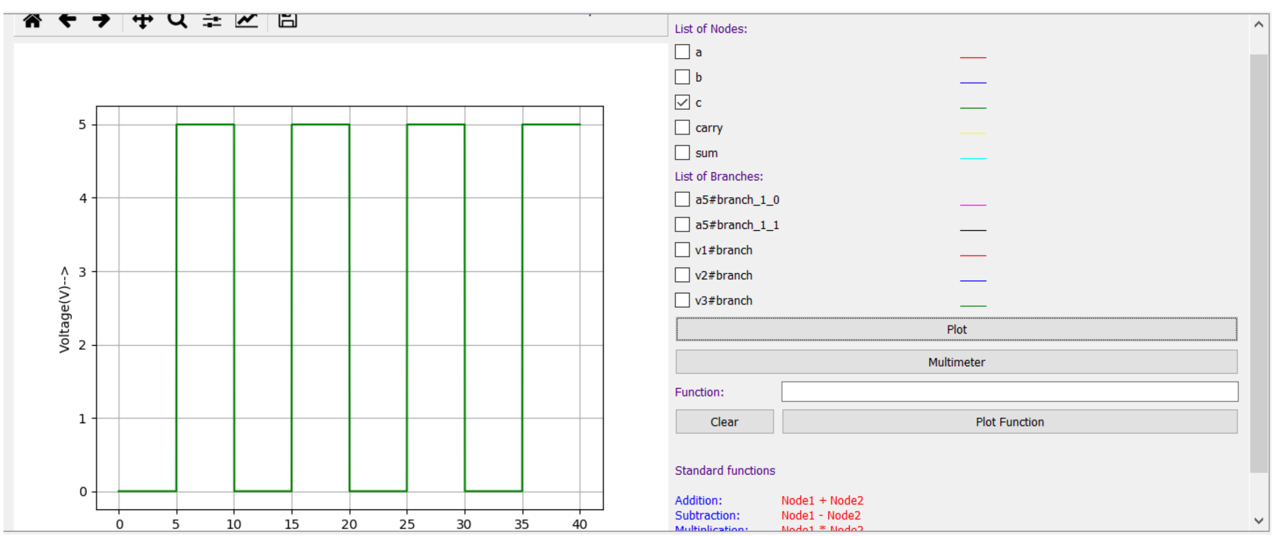
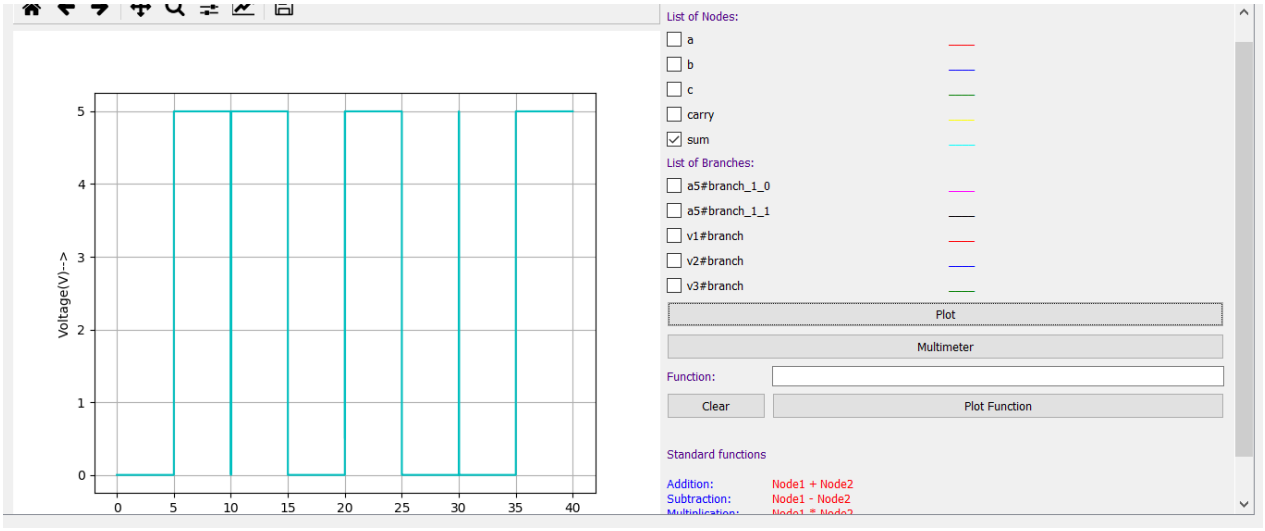
GND
pulse
v1
v2
v3
U1
U2
U3
plot_v1
A
B
C
adc_bridge_3
U4
IN1
IN2
IN3
OUT1
OUT2
OUT3
3x8_decoder
x1
IN1d_or
IN2
U5
U6
U7
U8
U9
U10
OUT
dac_bridge_2
U11
carry
U12
sum
U13
R1
R2
1k

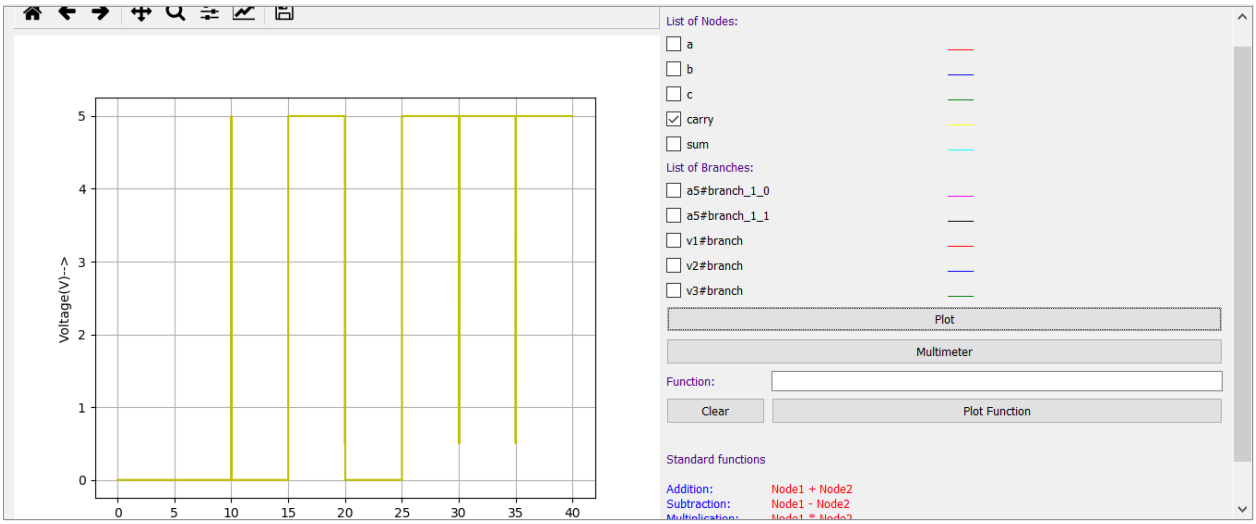
Python plots:











References:

https://www.deldsim.com/study/material/51/full-adder-function-using-38-decoder/