Circuit Simulation Project

https://esim.fossee.in/circuit-simulation-project

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Project Guide: Dr R. Maheshwari
Title of the circuit: Mod-7 Twisted Ring Counter Using J-K Flip Flop

Theory:

A twisted ring counter, also known as Johnson counter or walking ring counter, is a shift register in which the complement of the output of the last register is given as the input of the first register and circulates a stream of ones followed by zeros around the ring.

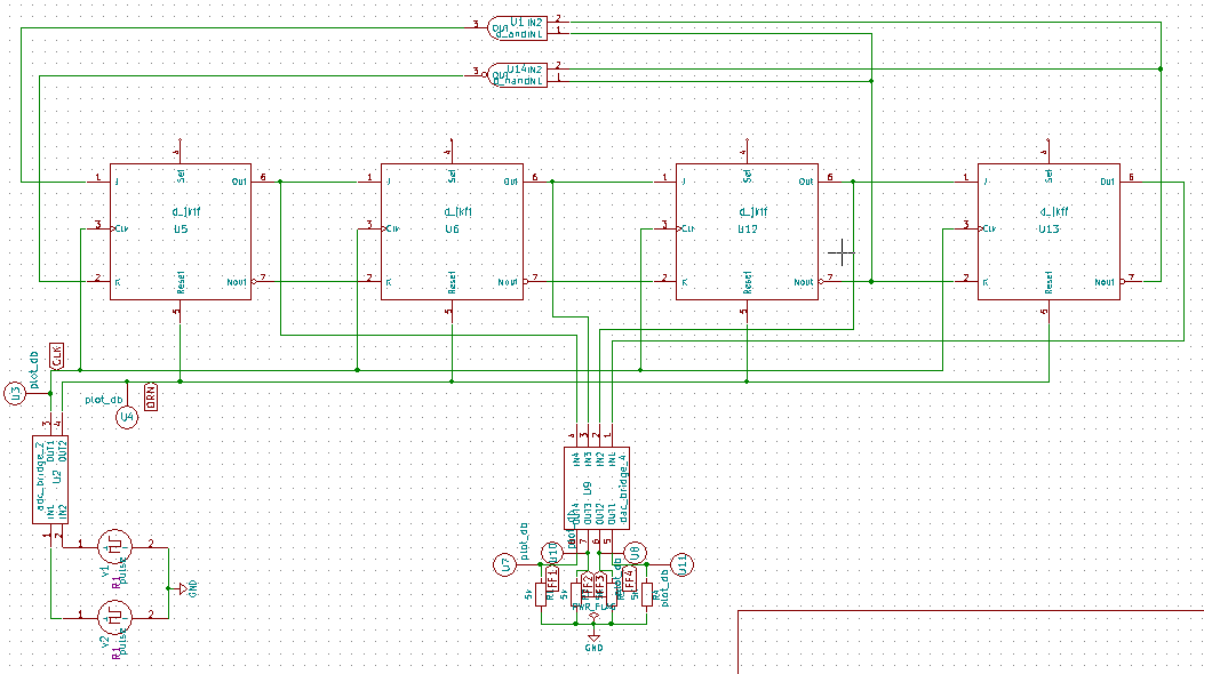
For example after every clock cycle the parallel output of the counter is as follows:

0000, 1000, 1100, 1110, 0111, 0011, 0001, 0000

As there are only 7 distinct states hence it's a Mod -7 counter.

In this project I have implemented Mod-7 Twisted Ring Counter using 4 J-K flip flops. So to make the J-K flip flop act like D flip flop we have to give the input to J and complement of the input to K. By using this principal I constructed this Mod-7 Twisted Ring Counter.

Circuit Diagram:



Results:

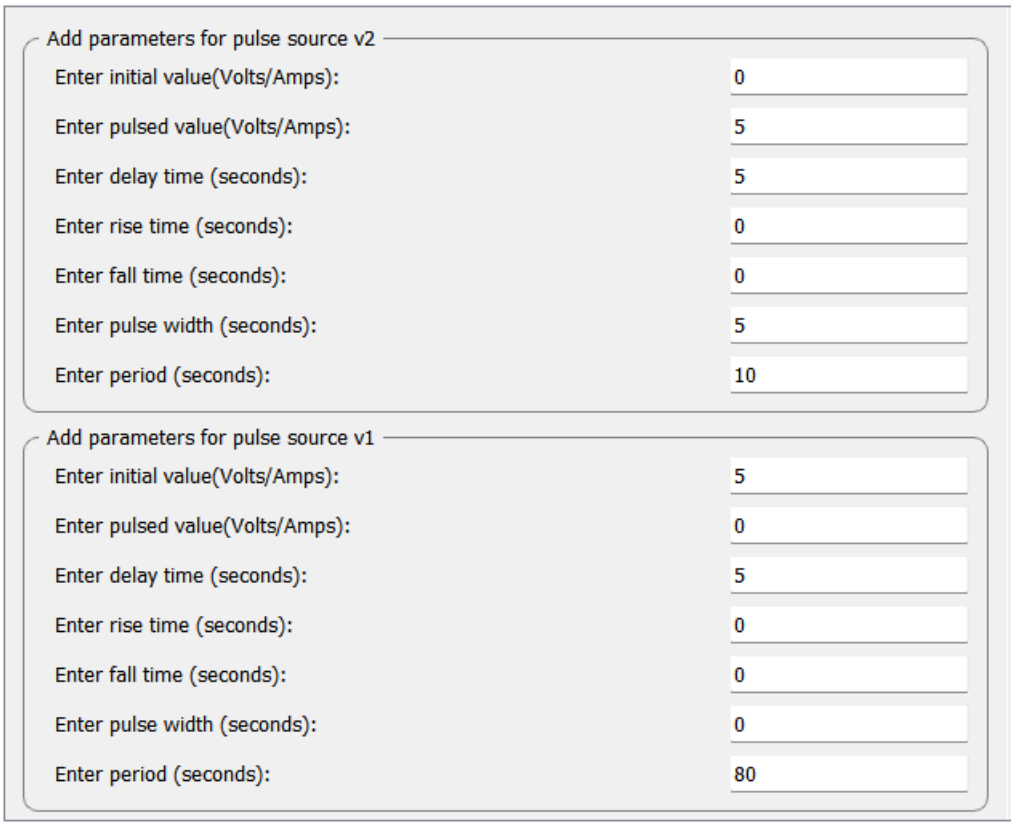
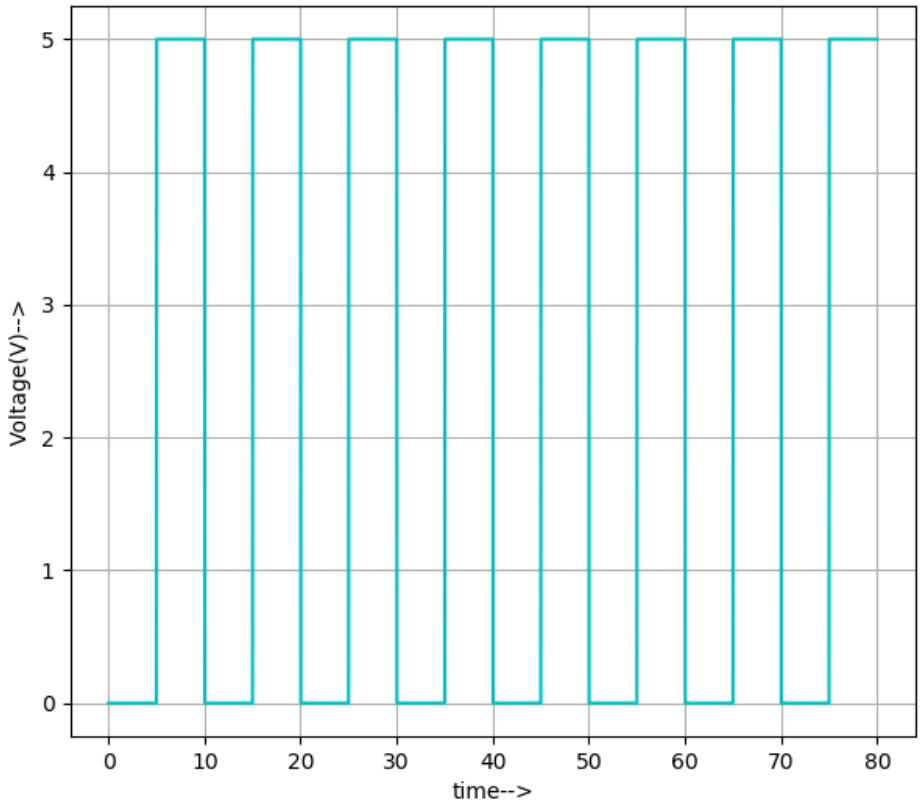
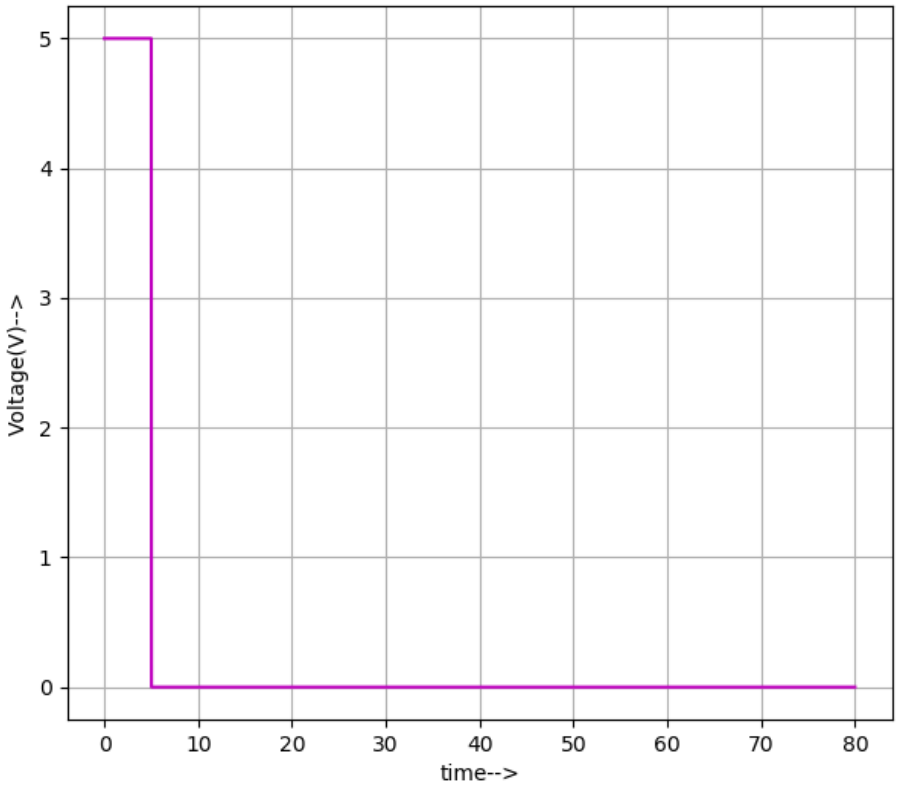


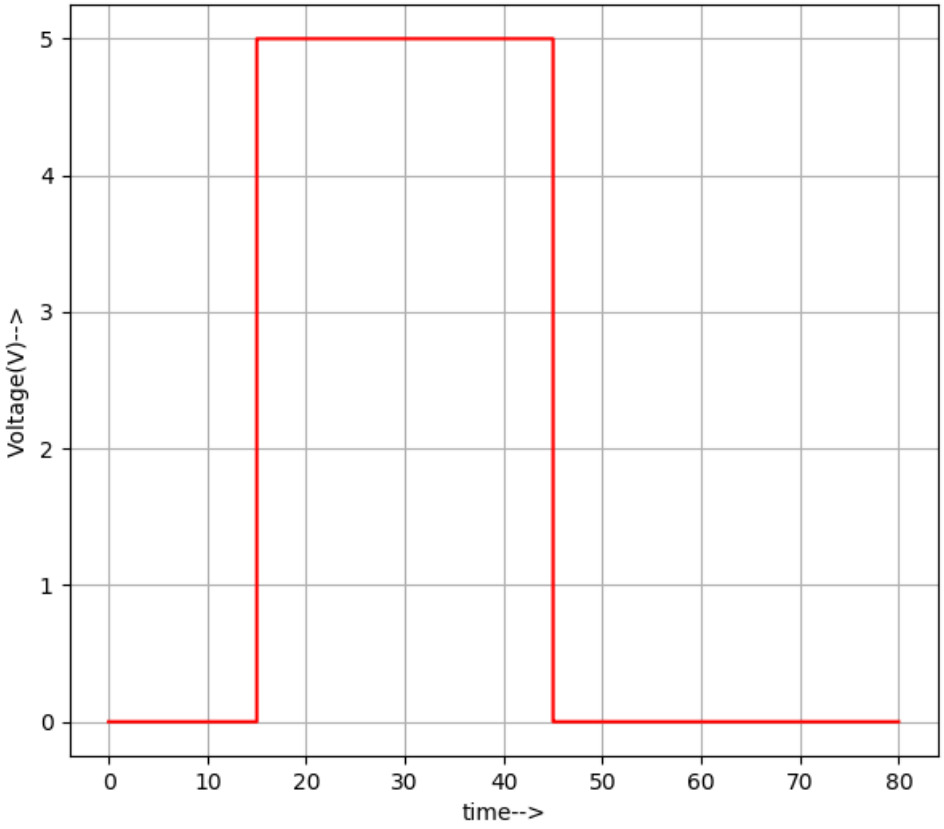
Fig 1: Source Details



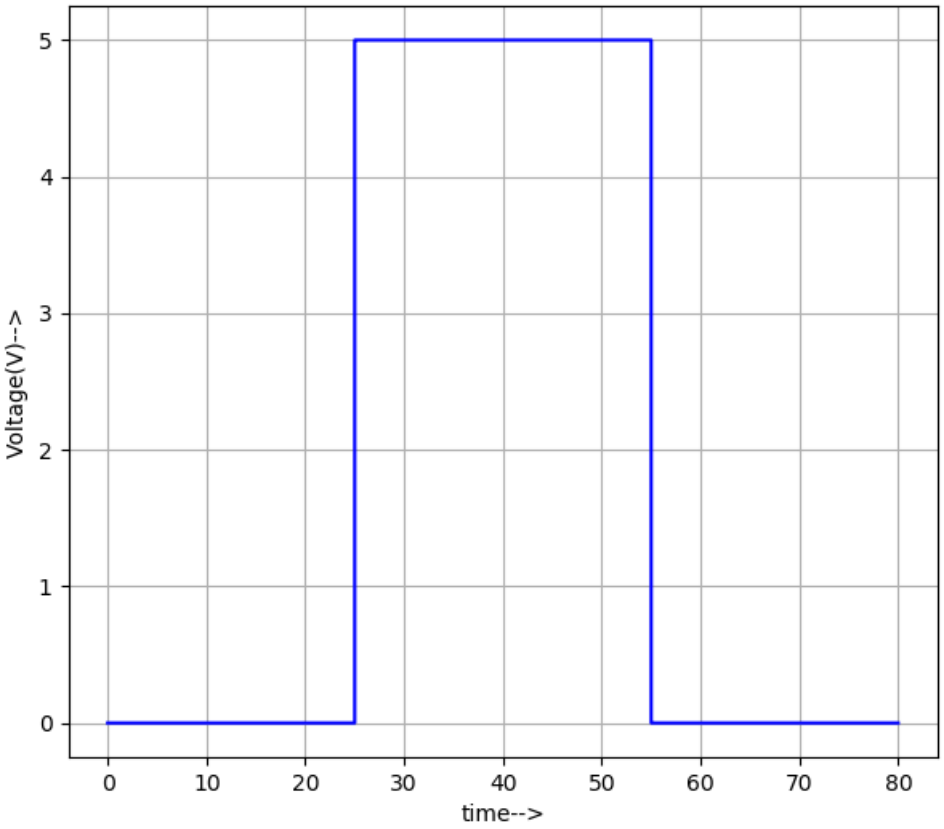
Plot 1: Clock Signal



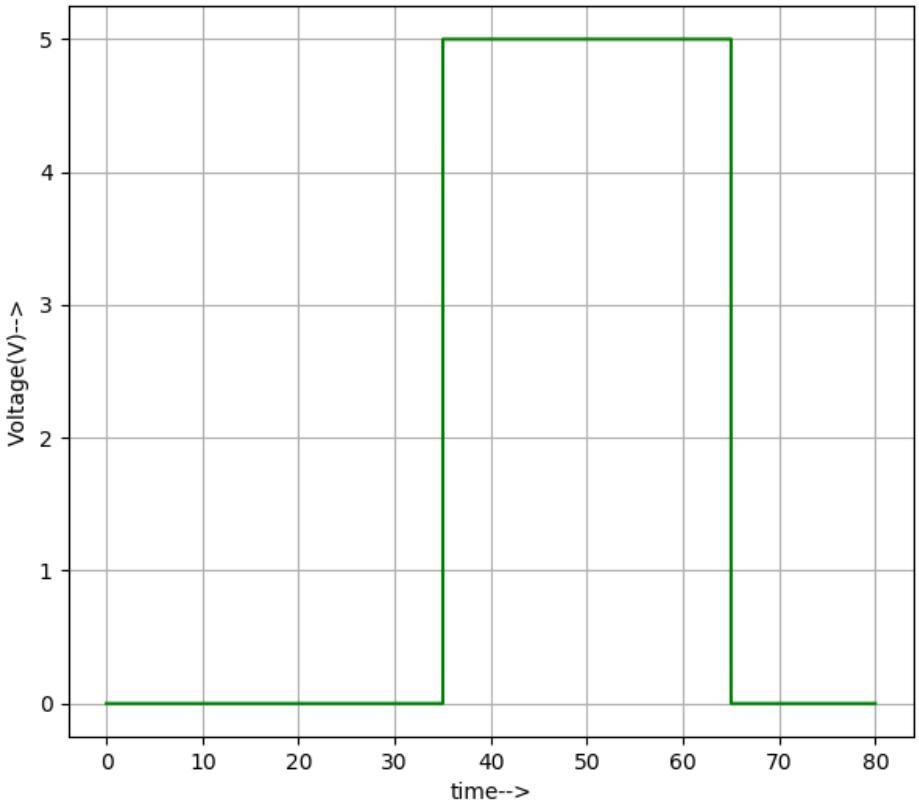
Plot 2: Orientation Signal



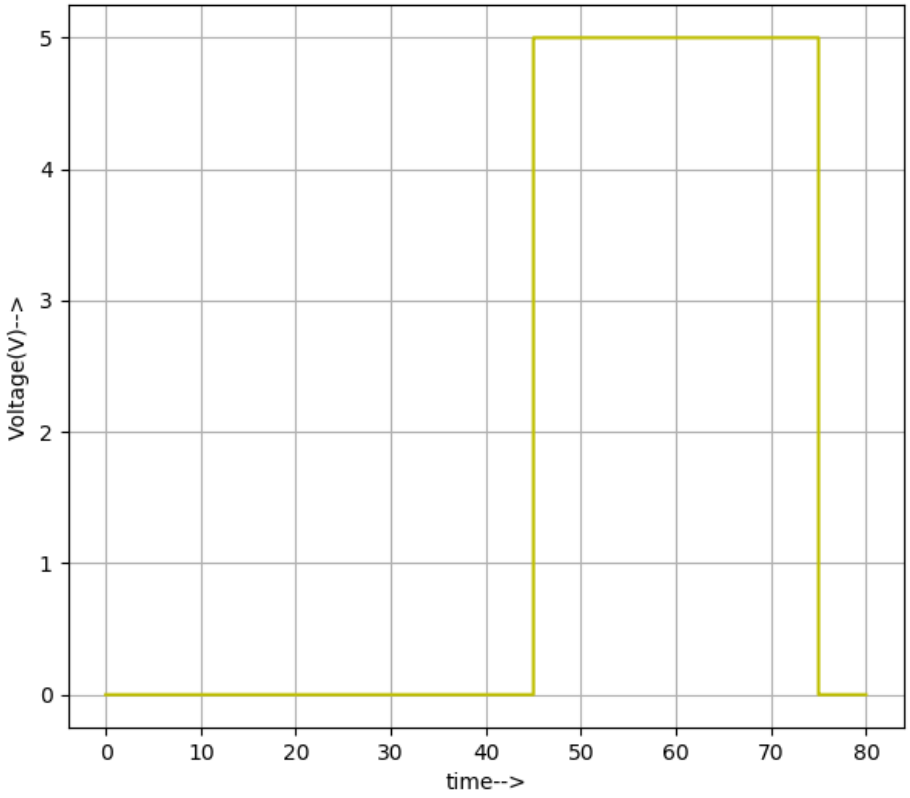
Plot 3: Output of Flip Flop 1



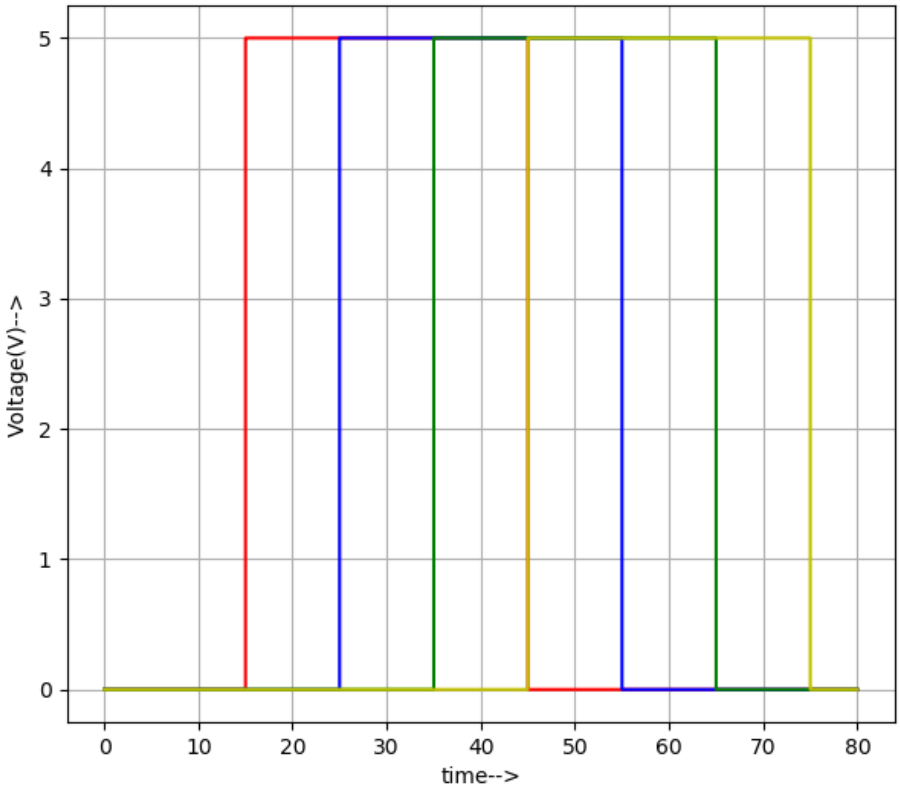
Plot 4: Output of Flip Flop 2



Plot 5: Output of Flip Flop 3



Plot 6: Output of Flip Flop 4



Plot 7: Output of All the Flip Flops

Hence the pattern formed here is 0000, 1000, 1100, 1110, 0111, 0011, 0001, and 0000.

Source/Reference(s):

https://www.geeksforgeeks.org/n-bit-johnson-counter-in-digital-logic/

https://www.electronics-tutorials.ws/sequential/seq_6.html