Circuit Simulation Project

https://esim.fossee.in/circuit-simulation-project

Name of the participant: Vishakha Agarwal

Project Guide: Dr. Maheswari R

Institute: Vellore Institute of Technology, Chennai

Title of experiment:

4-Bit Even Odd Parity Generator

Theory:

A Parity Generator is a combinational logic circuit that generates the parity bit in the transmitter. Parity is used to detect errors in transmitted data caused by noise or other disturbances.

Parity Generator is a combinational circuit that accepts n-1 bit data and generates the additional bit that is to be transmitted with the bit stream. This additional or extra bit is called as a Parity Bit.

In even parity bit scheme, the parity bit is '0' if there are even number of 1s in the data stream and the parity bit is '1' if there are odd number of 1s in the data stream.

In odd parity bit scheme, the parity bit is '1' if there are even number of 1s in the data stream and the parity bit is '0' if there are odd number of 1s in the data stream.

Truth table of 2's complement of 4-bit number:

A0	A1	A2	A3	Even	Odd
0	0	0	0	0	1
0	0	0	1	1	0
0	0	1	0	1	0
0	0	1	1	0	1
0	1	0	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	1	0
1	0	0	0	1	0
1	0	0	1	0	1
1	0	1	0	0	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	1	1	0
1	1	1	0	1	0
1	1	1	1	0	1

Schematic Diagram:

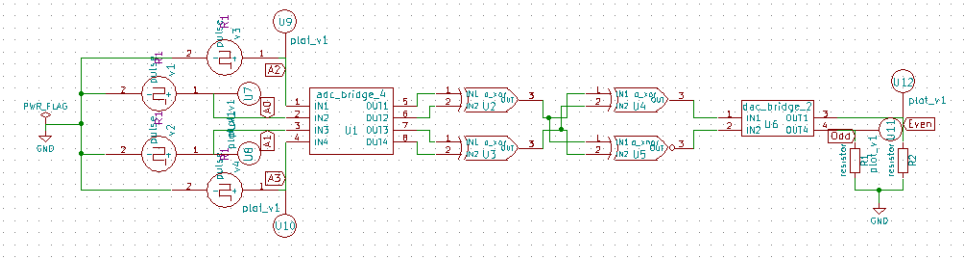

Figure 1: 4-Bit Parity Generator

Simulation Plots:

1. NgSpice Plots:

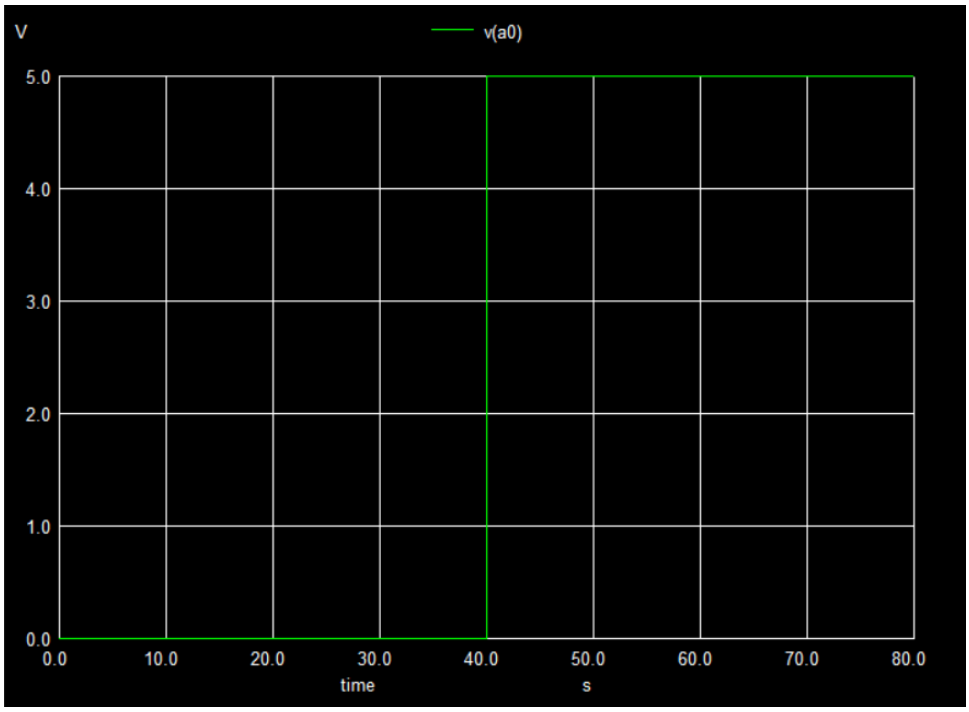

Figure 2.a: Input Plot (A0)

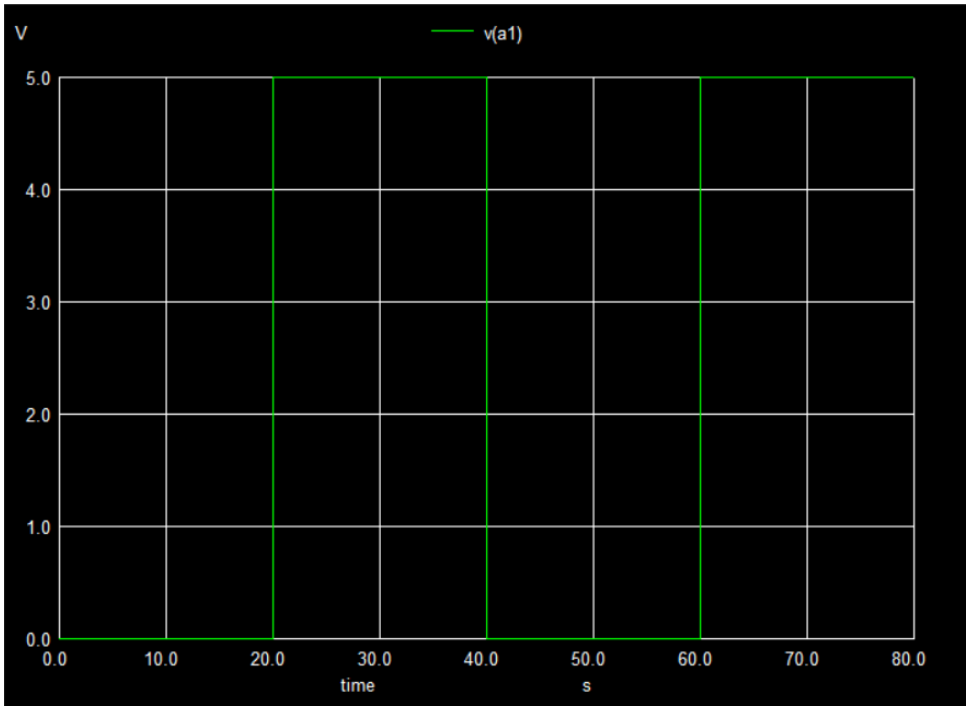

Figure 2.b: Input Plot (A1)

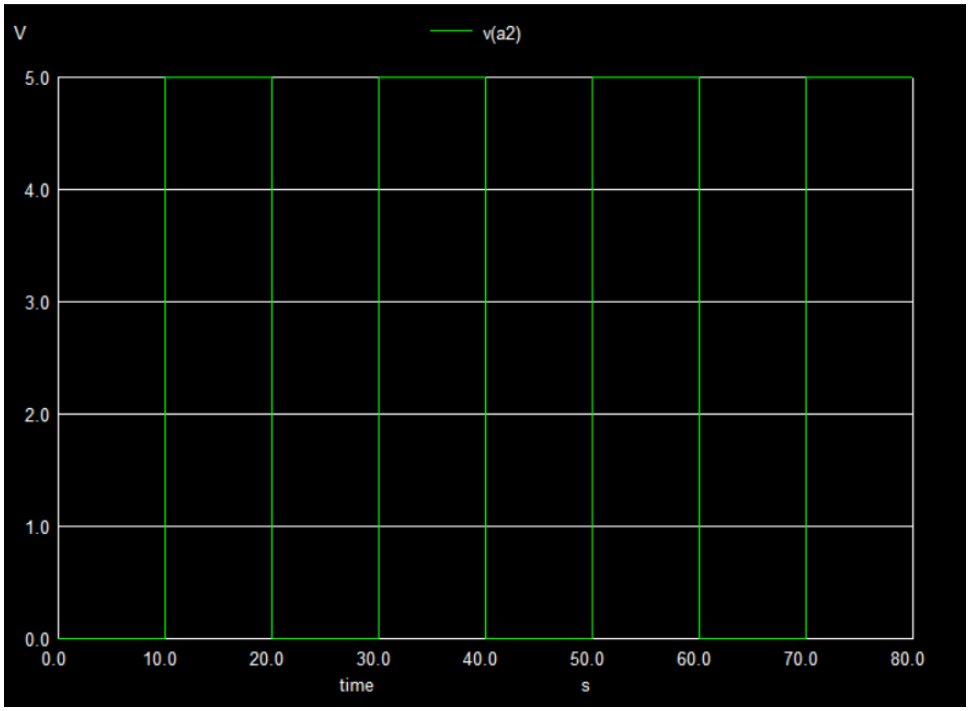

Figure 2.c: Input Plot (A2)

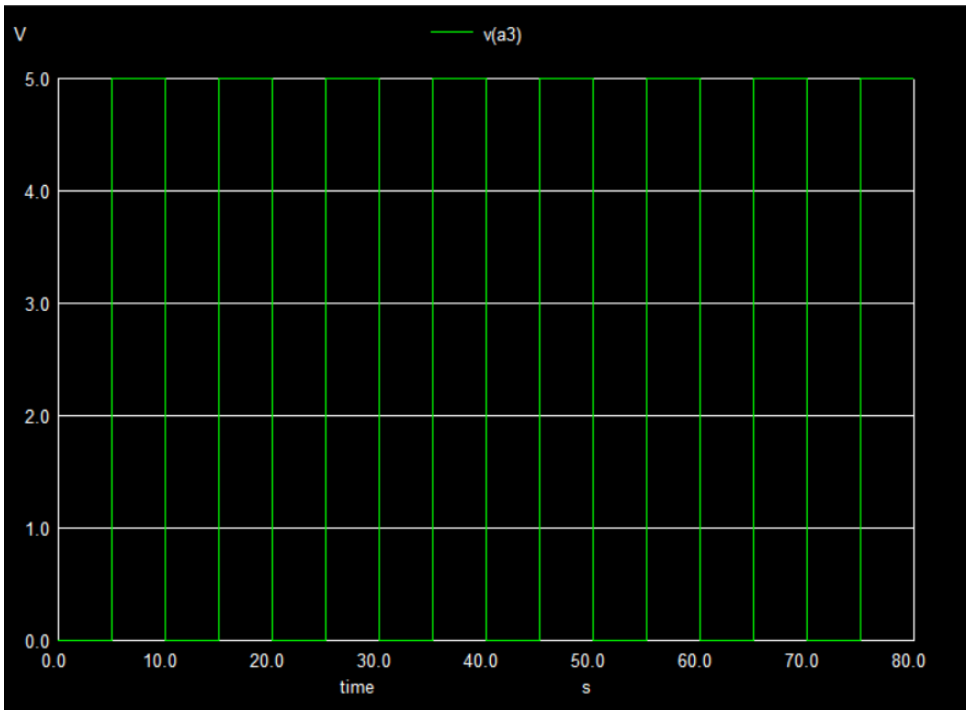

Figure 2.d: Input Plot (A3)

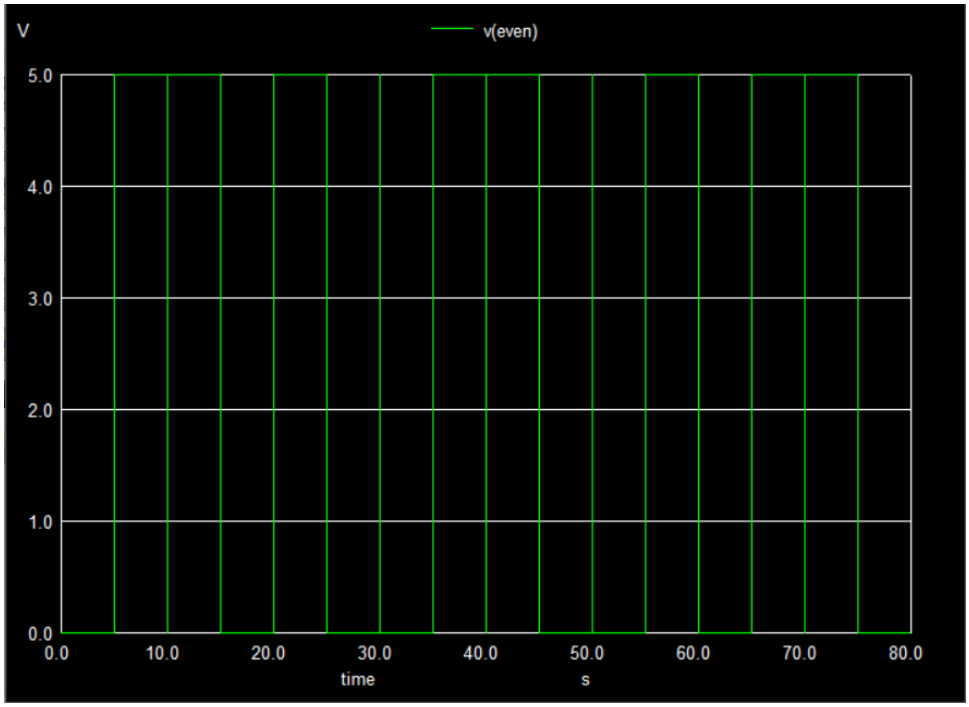

Figure 2.e: Output Plot (Even)

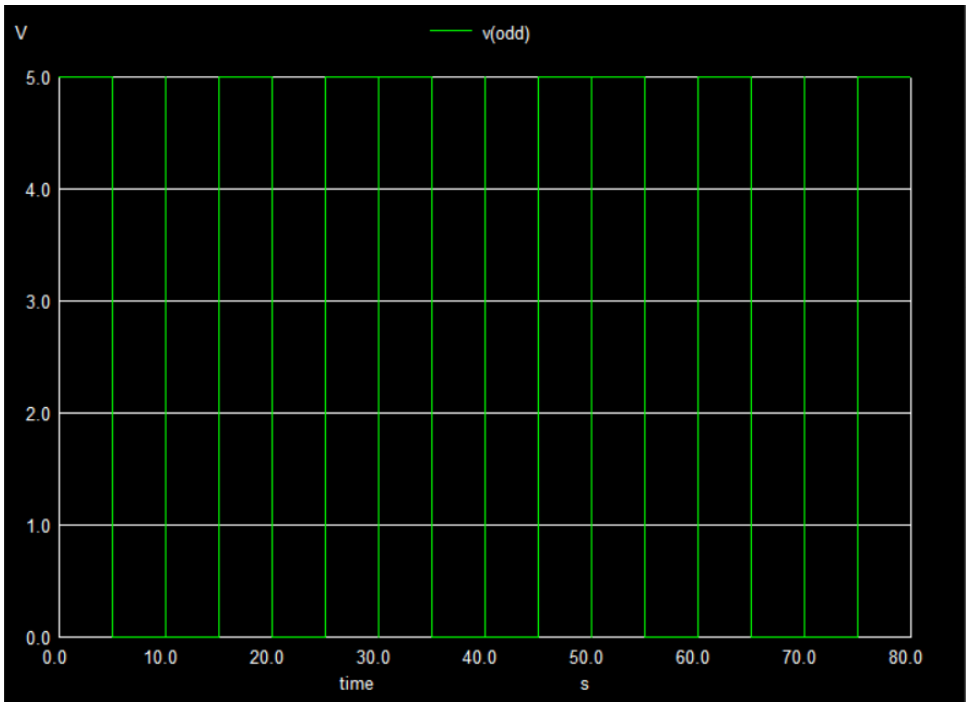

Figure 2.f: Output Plot (Odd)

2. Python Plots:

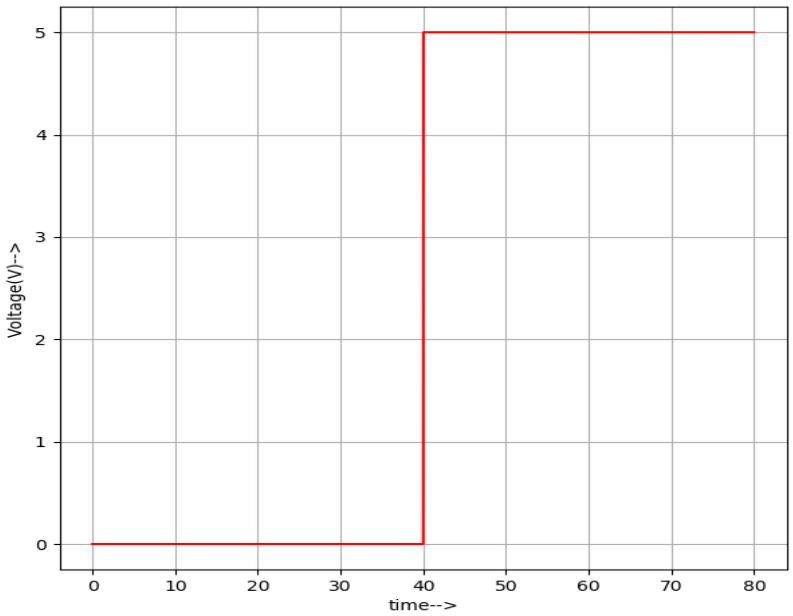

Figure 3.a: Input Plot (A0)

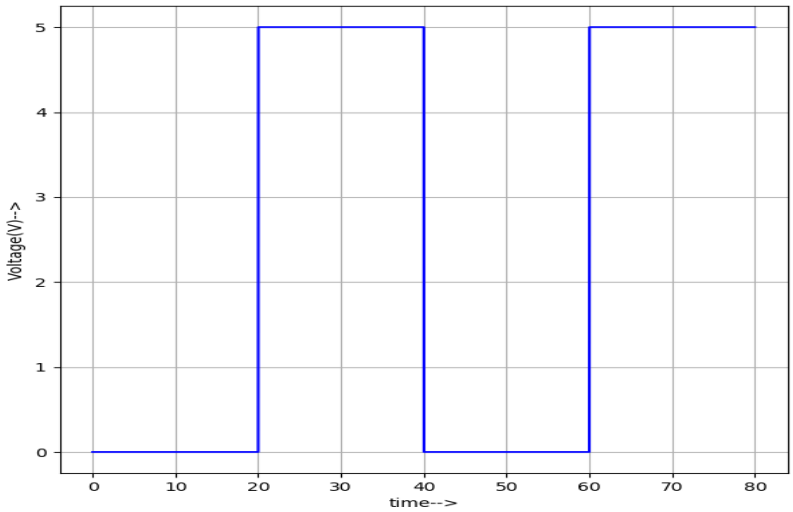

Figure 3.b: Input Plot (A1)

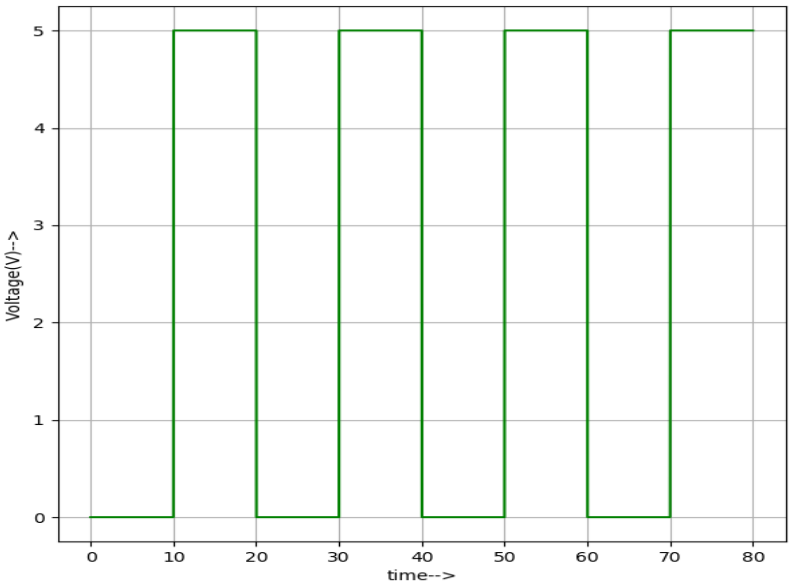

Figure 3.c: Input Plot (A2)

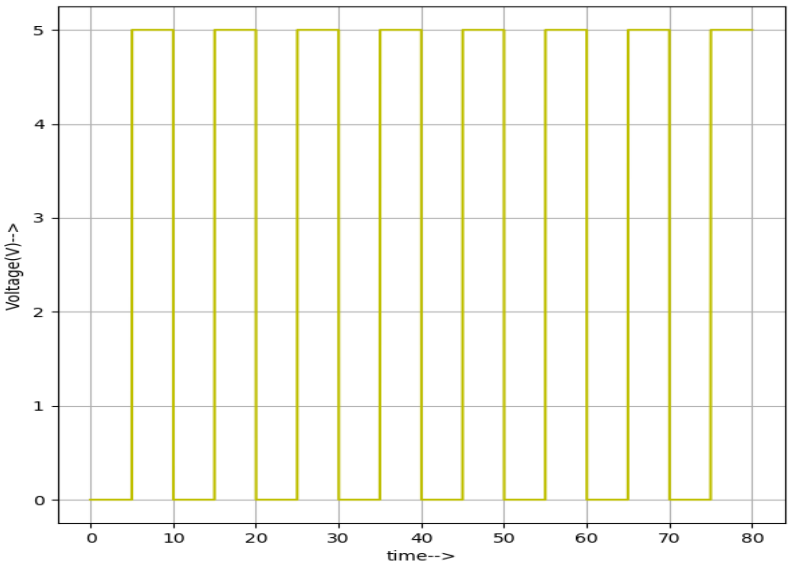

Figure 3.d: Input Plot (A3)

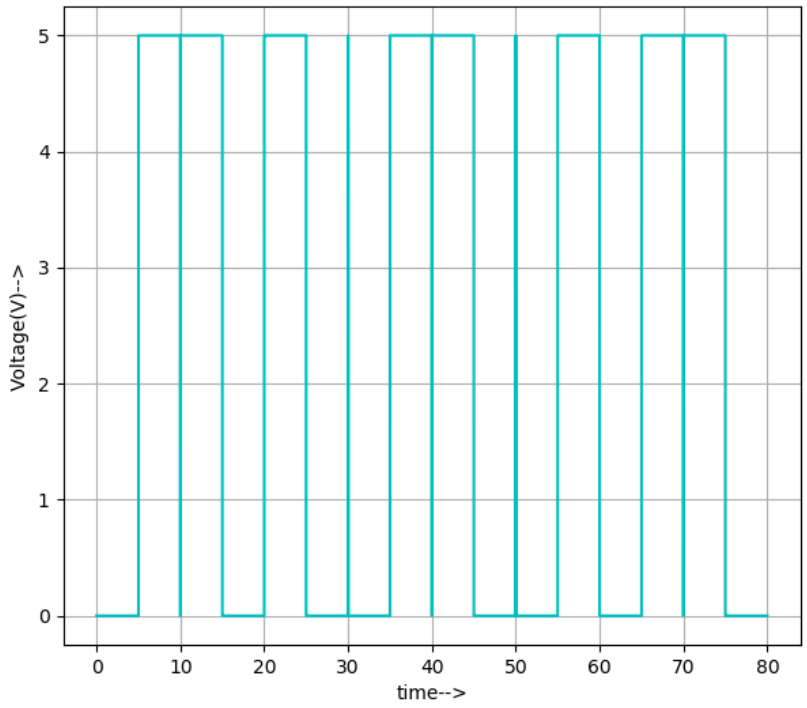

Figure 3.e: Output Plot (Even)

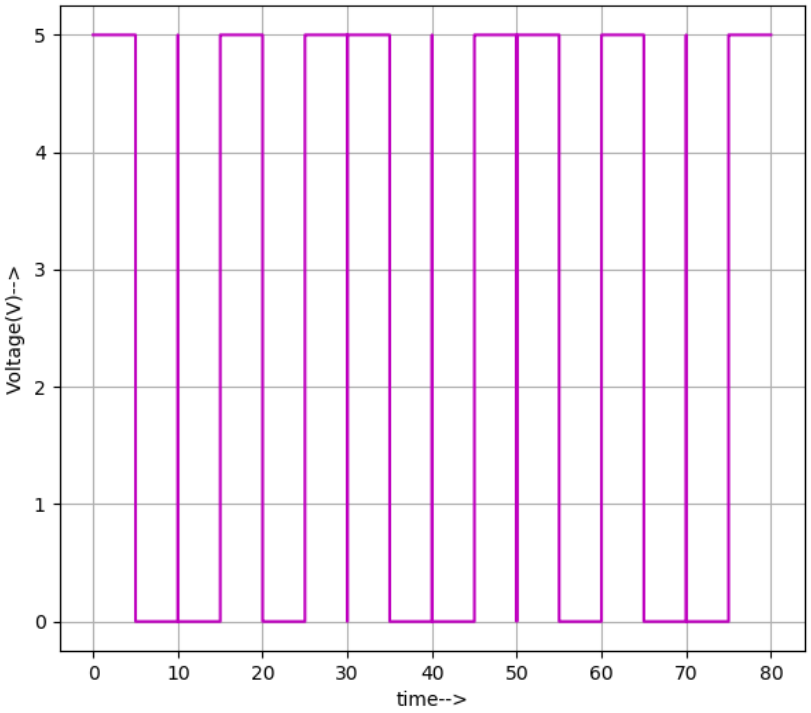

Figure 3.f: Output Plot (Odd)

Conclusion:

Using the circuit simulated, we have studied the logic and output of 4-bit parity generator and it's practical use. The results simulated follow the truth table, thus validating the correctness of the circuit simulated.

References:

https://www.electronicshub.org/parity-generator-and-parity-check/