Circuit Simulation Project

https://esim.fossee.in/circuit-simulation-project

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Project Guide: Dr. Maheswari. R

Title of the project:

Design of a NAND gate based Decoder with Enable

Theory/Description:

A **binary decoder** is a combinational logic circuit that converts binary information from the n coded inputs to a maximum of 2n unique outputs. They are used in a wide variety of applications, including instruction decoding, data multiplexing and data demultiplexing, seven segment displays etc.

Decoders can also be constructed with NAND gates. Since a NAND gate produces the AND operation with an inverted output, it becomes more economical to generate the decoder minterms in their complemented form.

The circuit operates with complemented outputs and a complement enable input. The decoder is enabled when enable, *E* is equal to 0 (i.e., active-low enable).

If A and B are the inputs and E is the enable then the equations of the outputs of a 2 x 4 NAND gate based decoder are:

D0 = A'B'E'

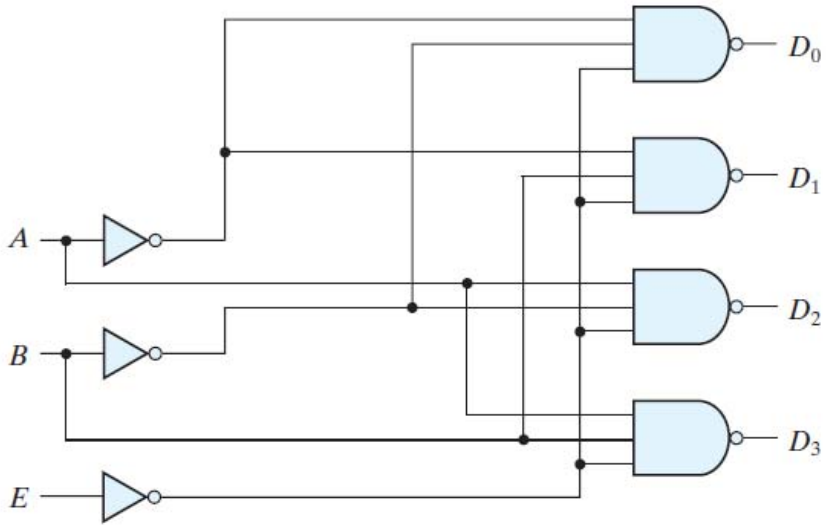
D1 = A'BE'

D2 = AB'E'

D3 = ABE'

where A', B' and E' represents the complement of A, B and E respectively.

Circuit Diagram of a 2 to 4 NAND Gate based decoder with enable:

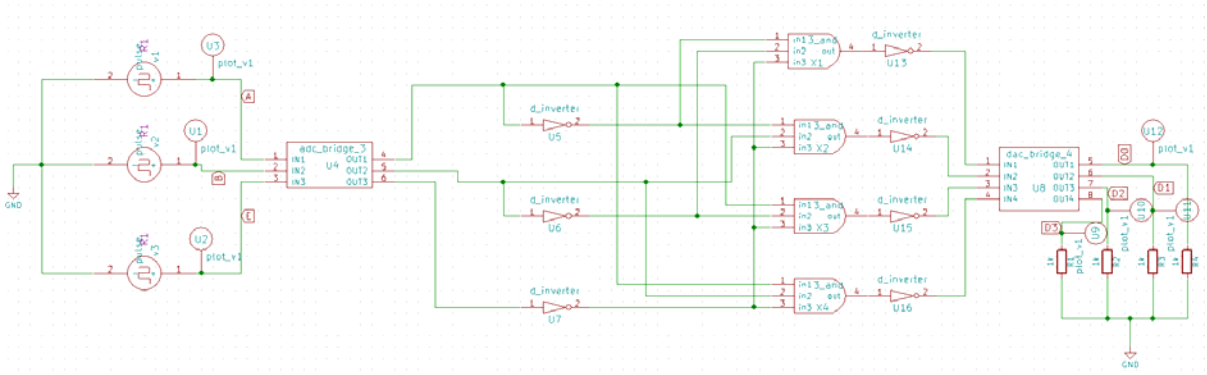


Truth table:

E	A	B	D_0	D_1	D_2	D_3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	1

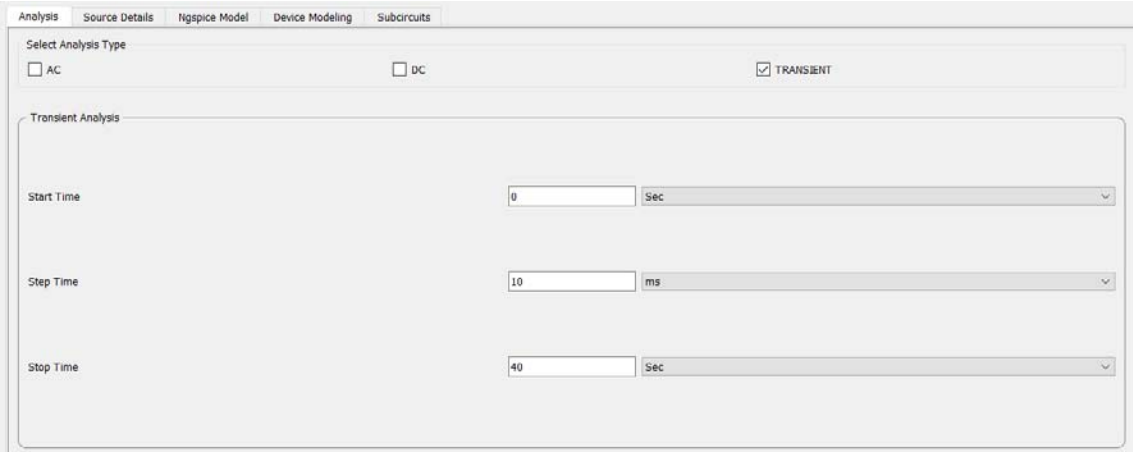
Circuit Diagrams using eSim:

- Circuit Diagram of 2 to 4 NAND gate based Decoder:



Source details:

Analysis:

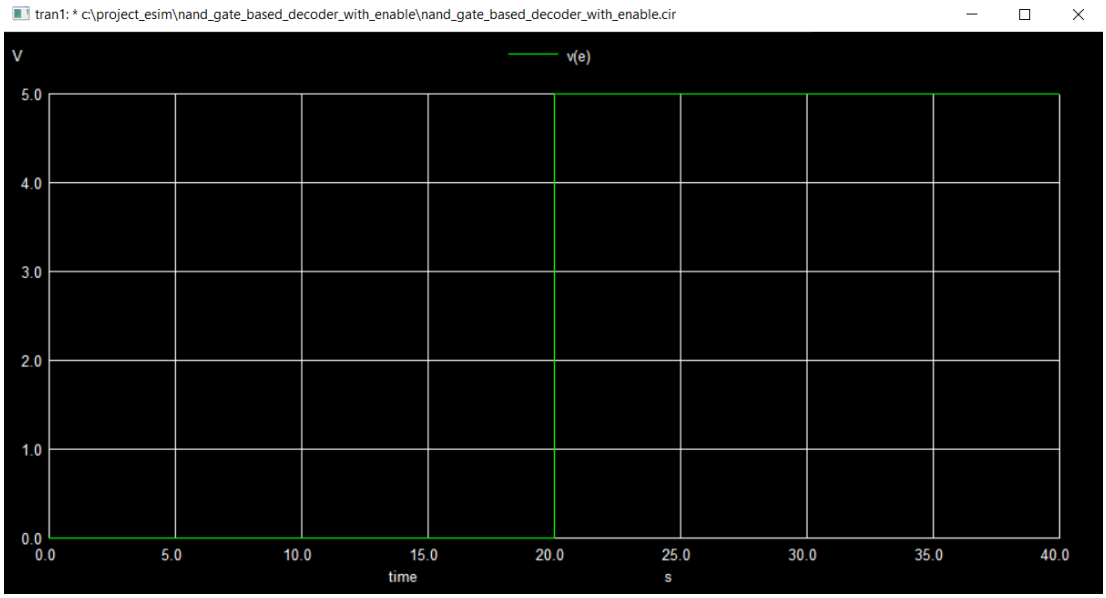

Analysis
Source Details
Ngspice Model
Device Modeling
Subcircuits
Select Analysis Type
AC
DC
TRANSIENT
Transient Analysis
Start Time
0
Sec
Step Time
10
ms
Stop Time
40
Sec

Results

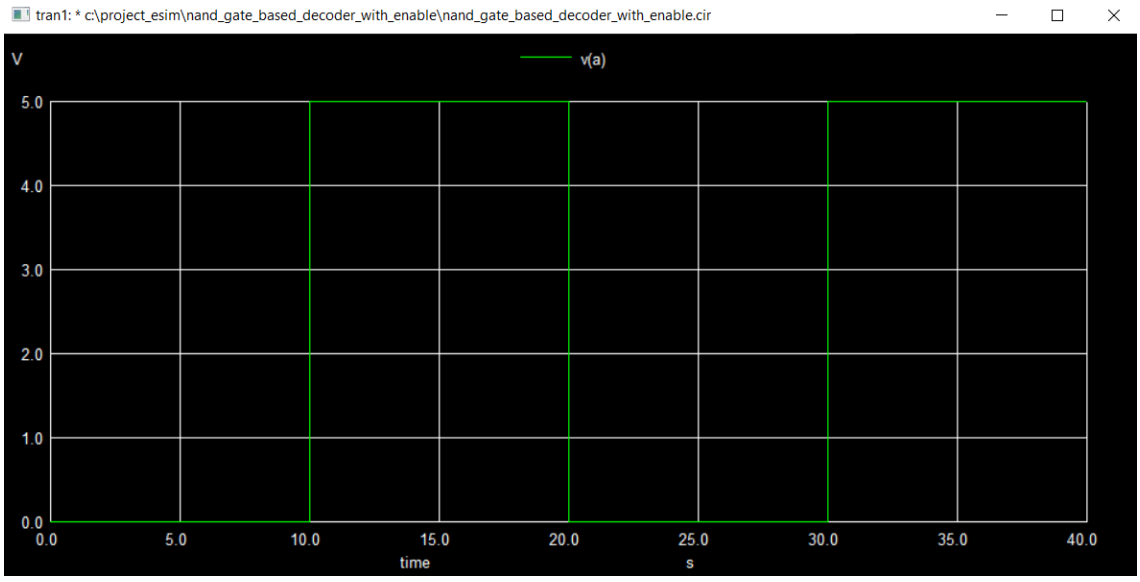
Ngspice plots:

Input waveforms:

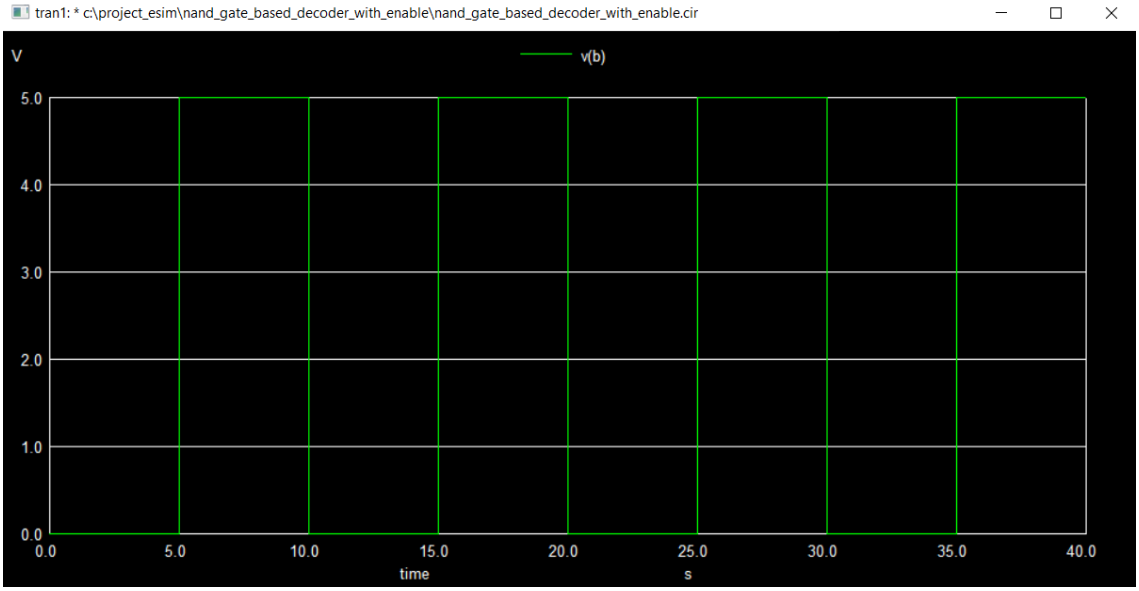
- **E**



- **A**

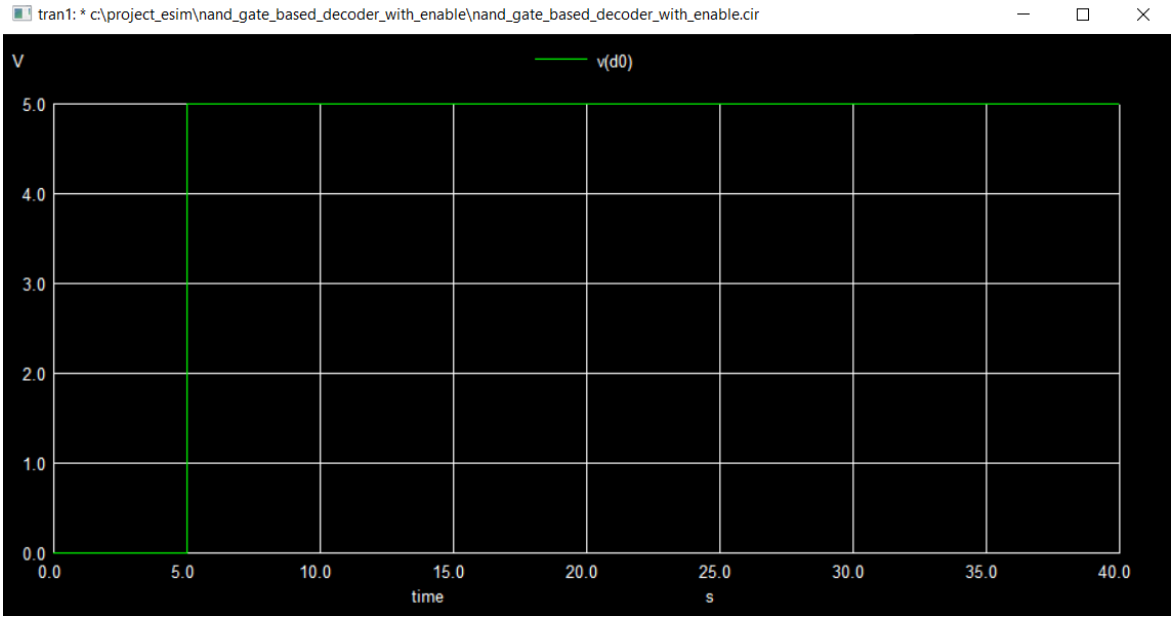


- **B**

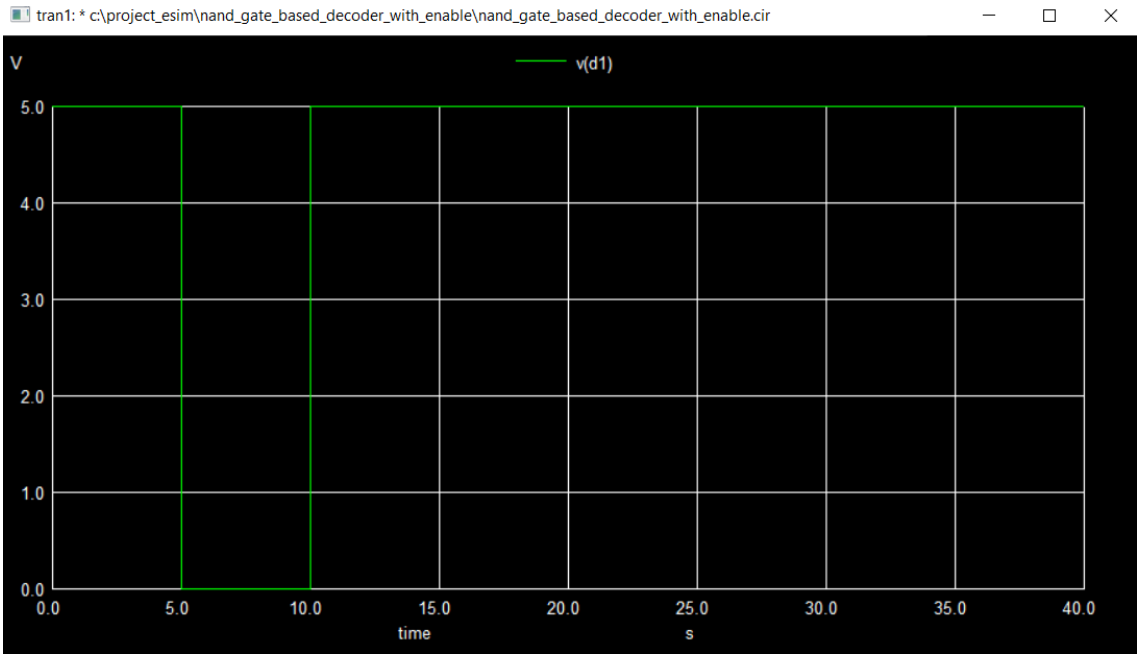


Output Waveforms:

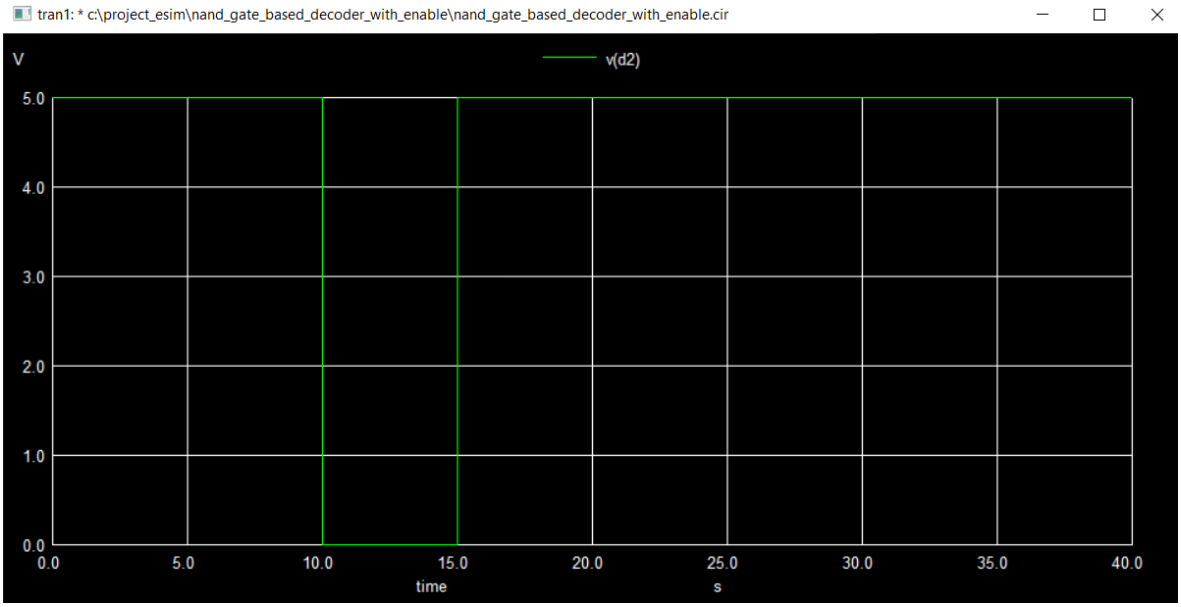
- **D0**



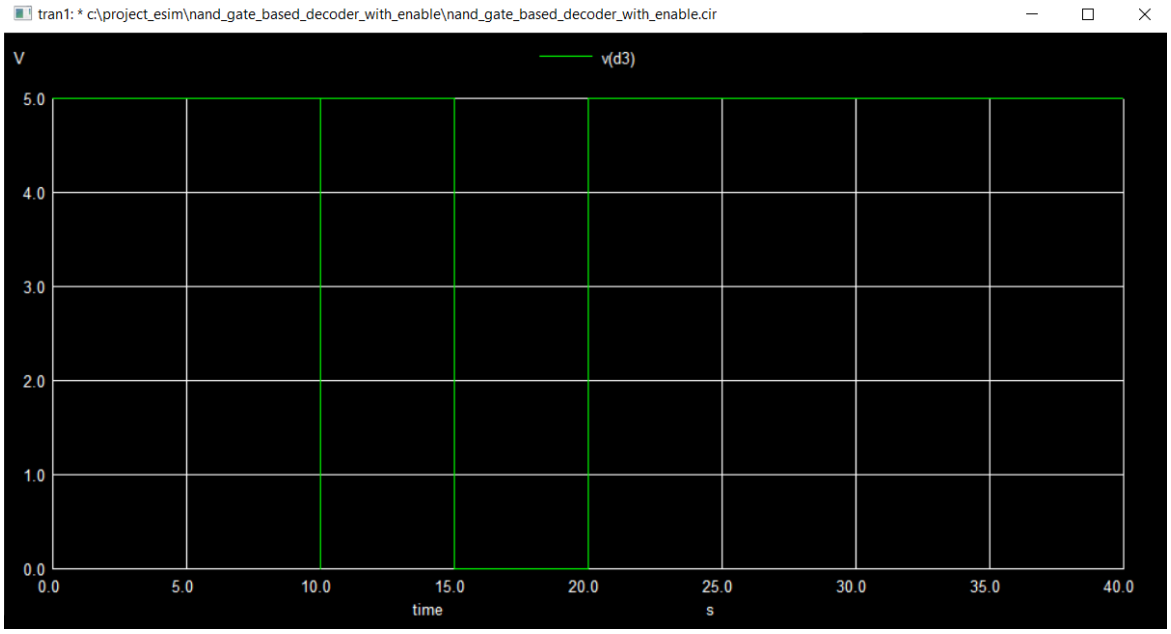
- **D1**


tran1: * c:\project_esim\nand_gate_based_decoder_with_enable\nand_gate_based_decoder_with_enable.cir
V
v(d1)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
5.0
10.0
15.0
20.0
25.0
30.0
35.0
40.0
time
s

- **D2**


tran1: * c:\project_esim\nand_gate_based_decoder_with_enable\nand_gate_based_decoder_with_enable.cir
V
v(d2)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
5.0
10.0
15.0
20.0
25.0
30.0
35.0
40.0
time
s

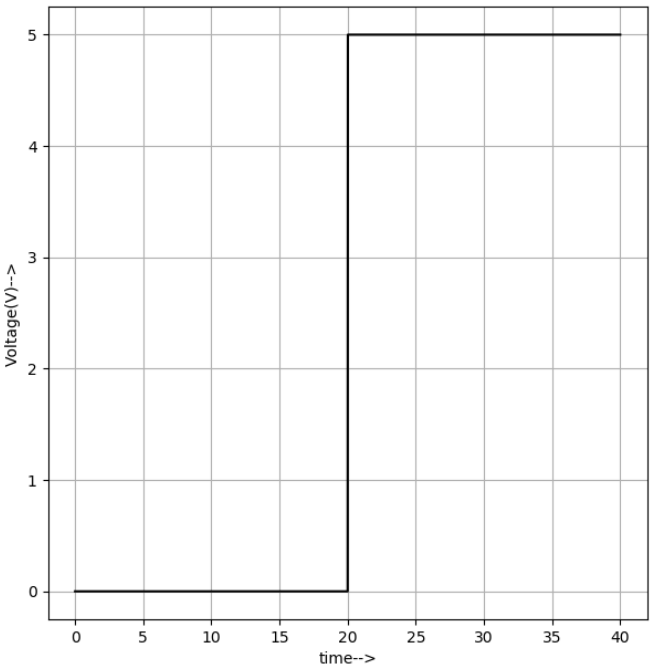
- **D3**


tran1: * c:\project_esim\nand_gate_based_decoder_with_enable\nand_gate_based_decoder_with_enable.cir
V
v(d3)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
5.0
10.0
15.0
20.0
25.0
30.0
35.0
40.0
time
s

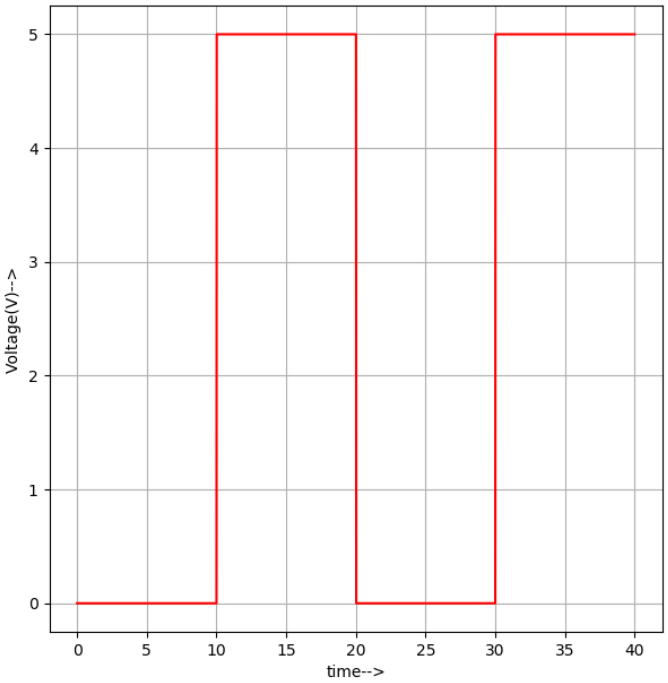
Python plots:

Inputs:

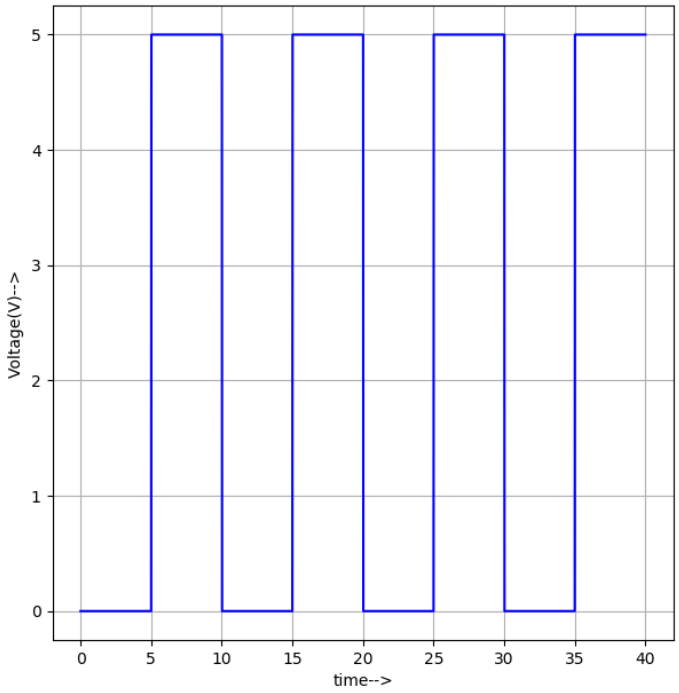
- **E**



- **A**

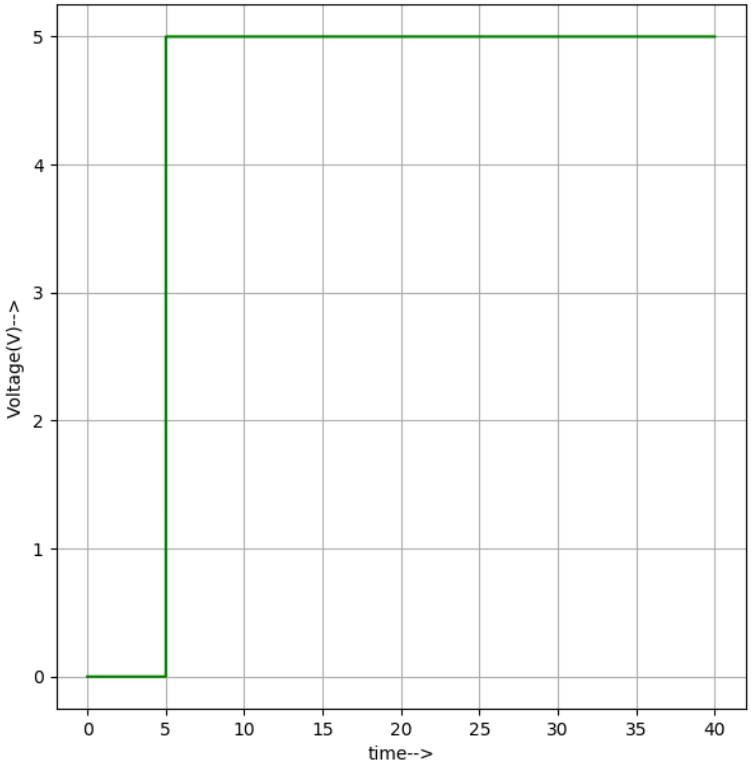


- **B**

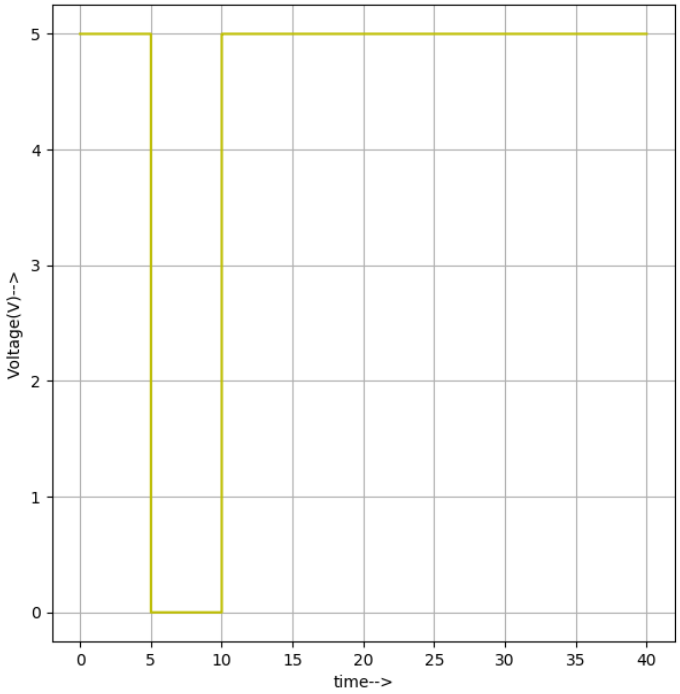

Voltage(V)-->
time-->
0
1
2
3
4
5
0
5
10
15
20
25
30
35
40

Outputs:

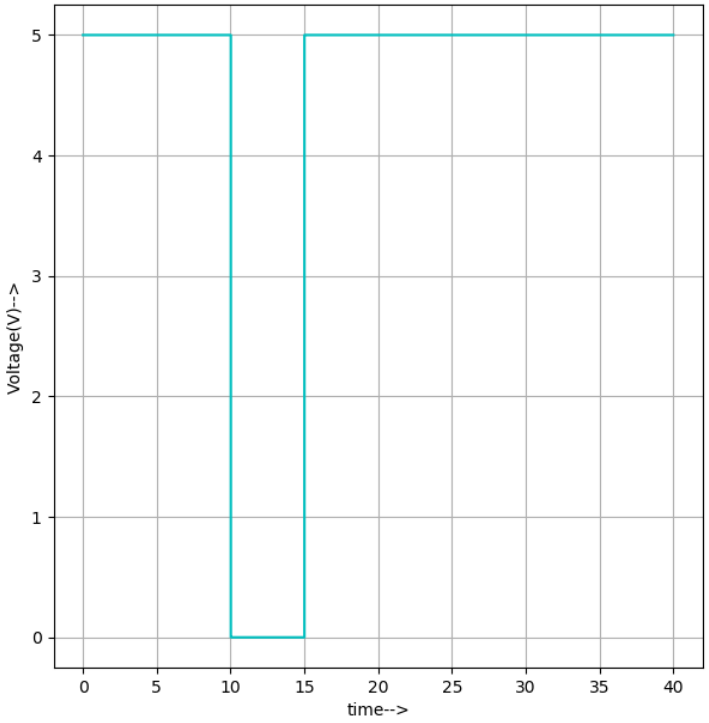
- **D0**


Voltage(V)-->
time-->
0
1
2
3
4
5
0
5
10
15
20
25
30
35
40

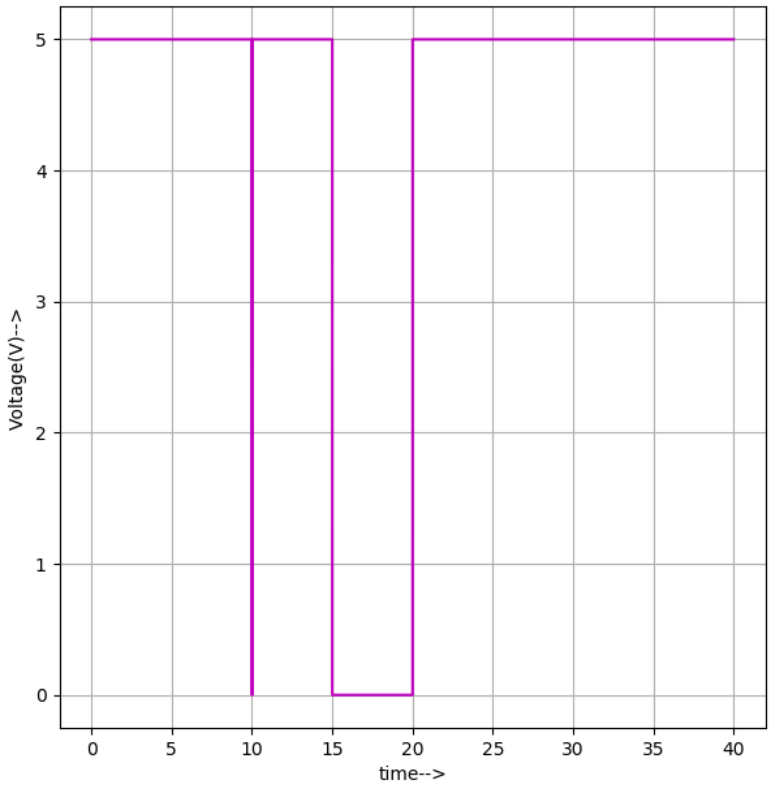
- **D1**


Voltage(V)-->
time-->
0
1
2
3
4
5
0
5
10
15
20
25
30
35
40

- **D2**


Voltage(V)-->
time-->
0
1
2
3
4
5
0
5
10
15
20
25
30
35
40

- **D3**



References:

M. Morris Mano and Michael D.Ciletti – Digital Design: With an introduction to Verilog HDL - Pearson Education – 5th Edition- 2014, Pg no. 152

https://www.electronics-tutorials.ws/combination/comb_5.html

https://en.wikipedia.org/wiki/Binary_decoder