Circuit Simulation Project

https://esim.fossee.in/circuit-simulation-project

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Project Guide: Dr R. Maheshwari

Title of the Circuit: Half Adder using NOR Gates

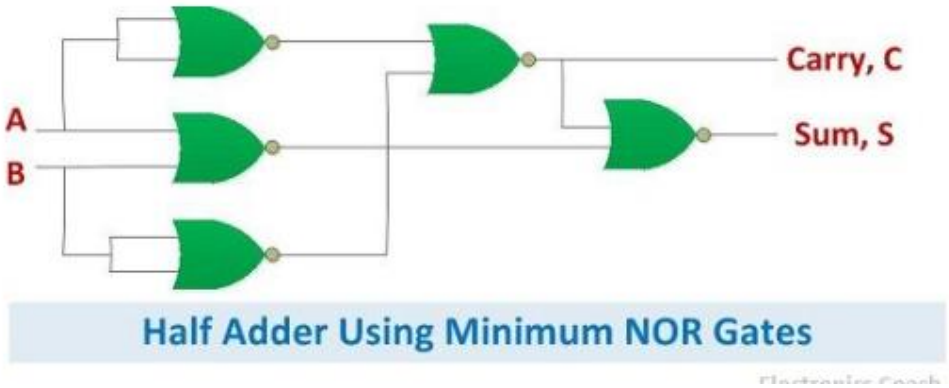
Description:

Half Adder is the digital circuit which can generate the result of the addition of two 1-bit numbers. It consists of two input terminals through which 1-bit numbers can be given for processing. After this, the half adder generates the sum of the numbers and carry if present.

The NOR gate is also a universal gate. Thus, it can also be used for designing of any digital circuit. The Half adder can be designed using 5 NOR gates. This is the minimum number of NOR gates to design half adder.

Firstly, three NOR gates are used in the designing and the output from two of these NOR gates is given to fourth NOR gate. The output from second NOR gate is given to the gate connected at the end. This will generate the sum bit of the addition of two 1-bit numbers.

Circuit Diagram:

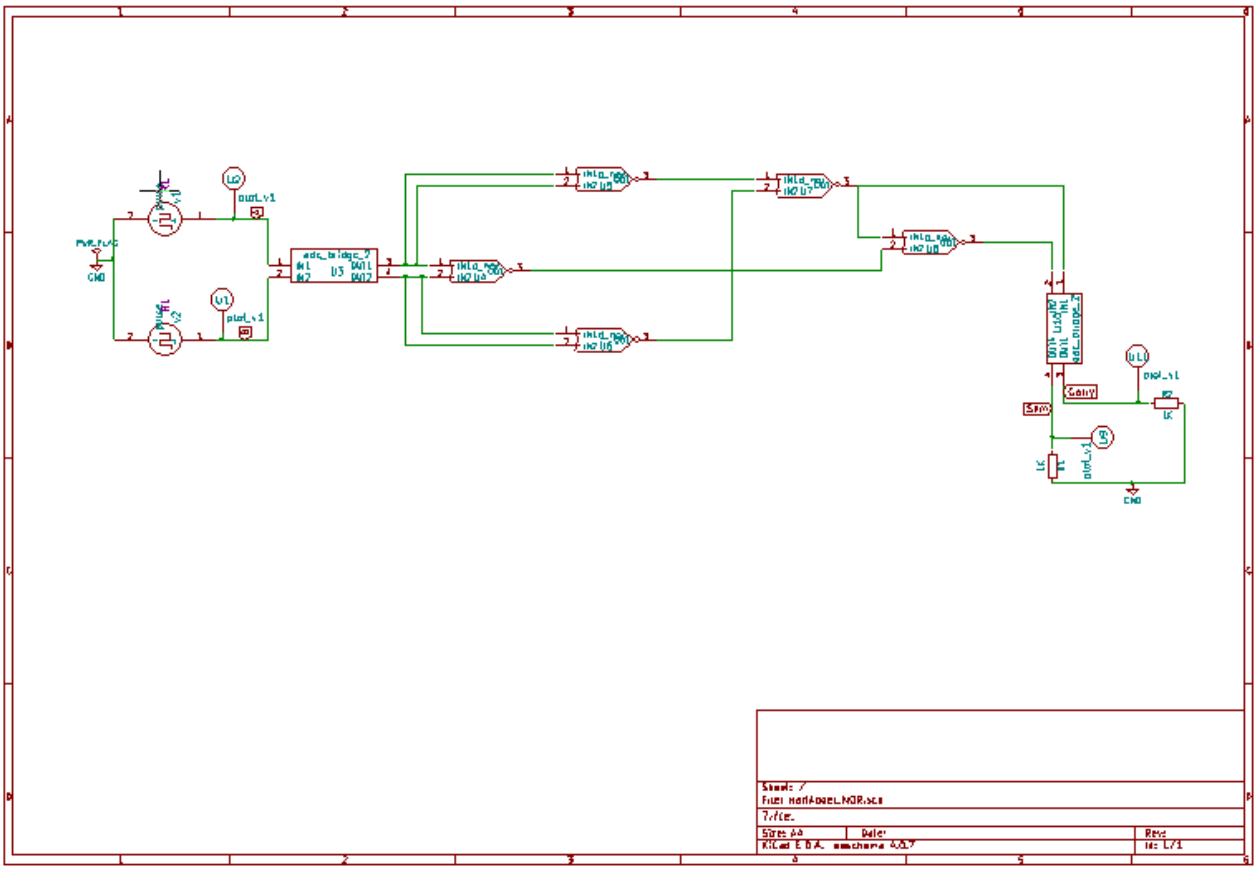


Half Adder Using Minimum NOR Gates

Truth table:

INPUTS		OUTPUTS	
A	B	Sum(S)	Carry(C)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

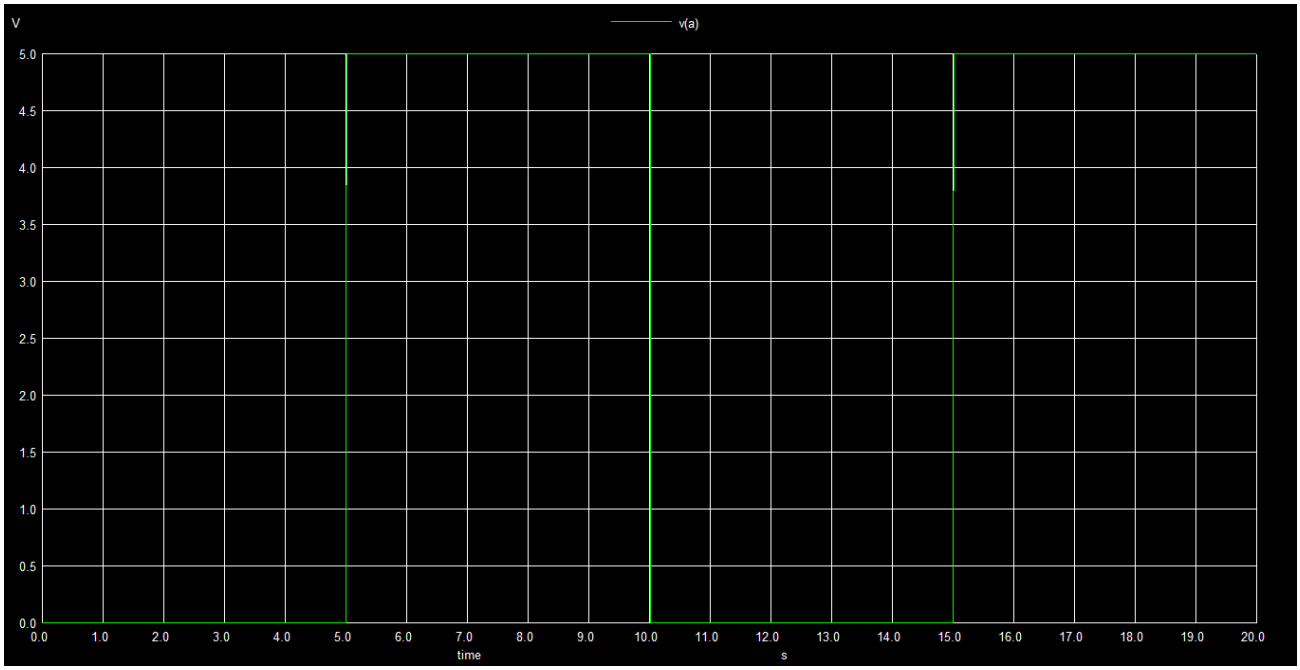
e-Sim Schematic:



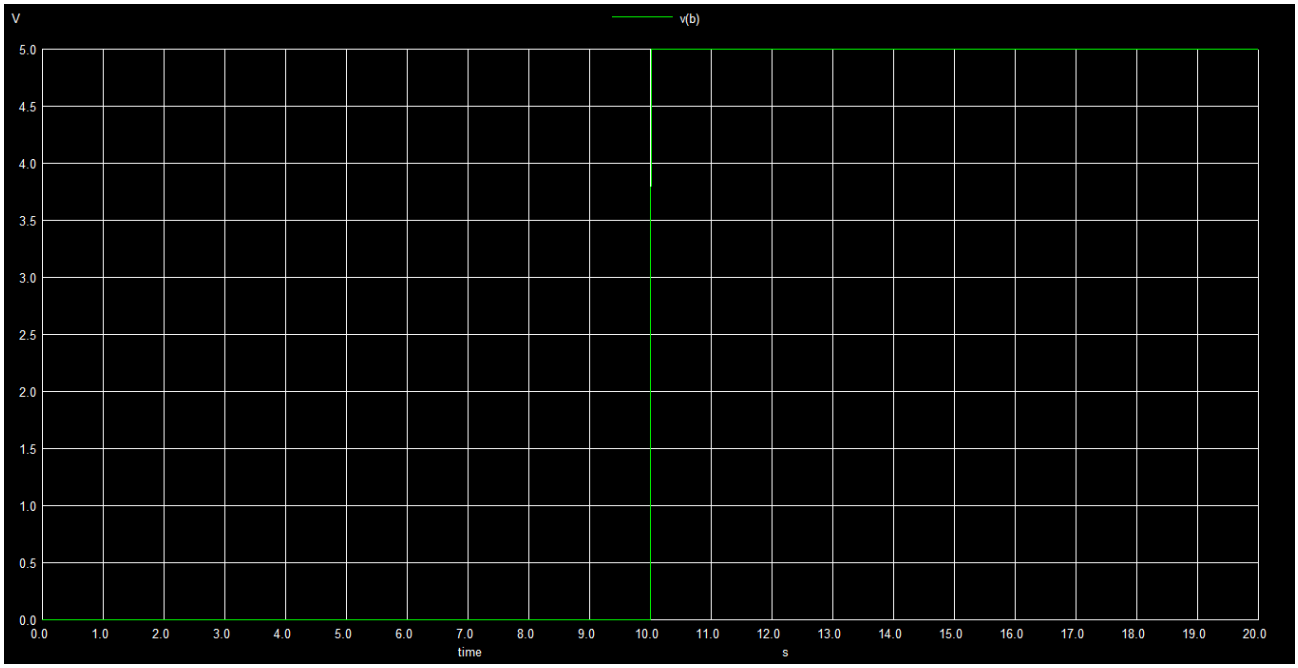
Simulation Results:

1. NgSpice Waveforms:

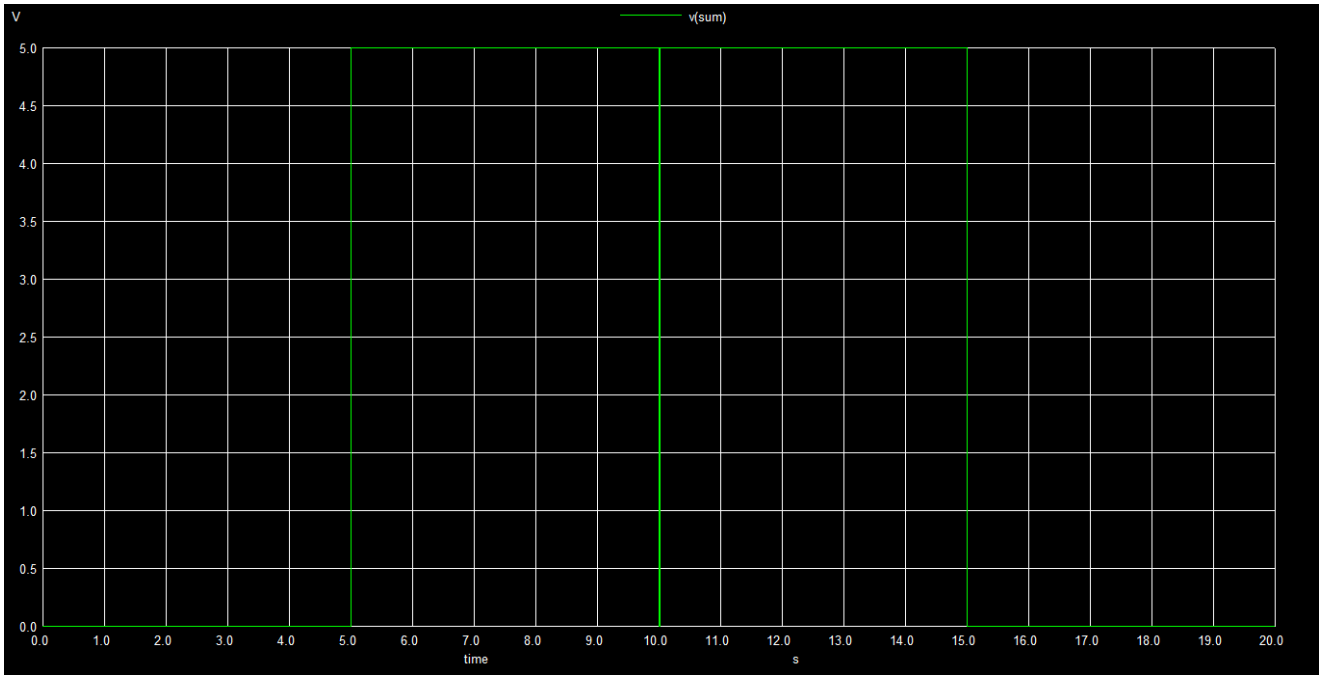
V(a):



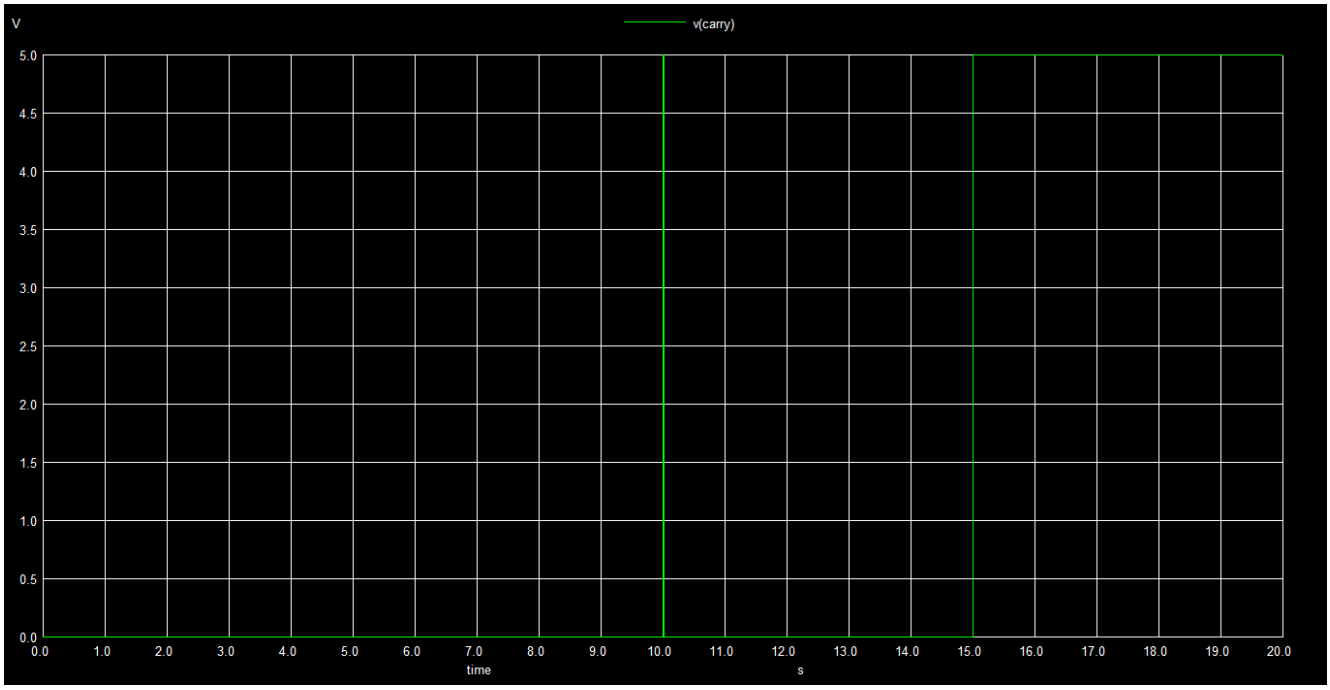
V(b):


V
v(b)
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0.0 1.0 2.0 3.0 4.0 5.0 6.0 7.0 8.0 9.0 10.0 11.0 12.0 13.0 14.0 15.0 16.0 17.0 18.0 19.0 20.0
time
s

Sum:

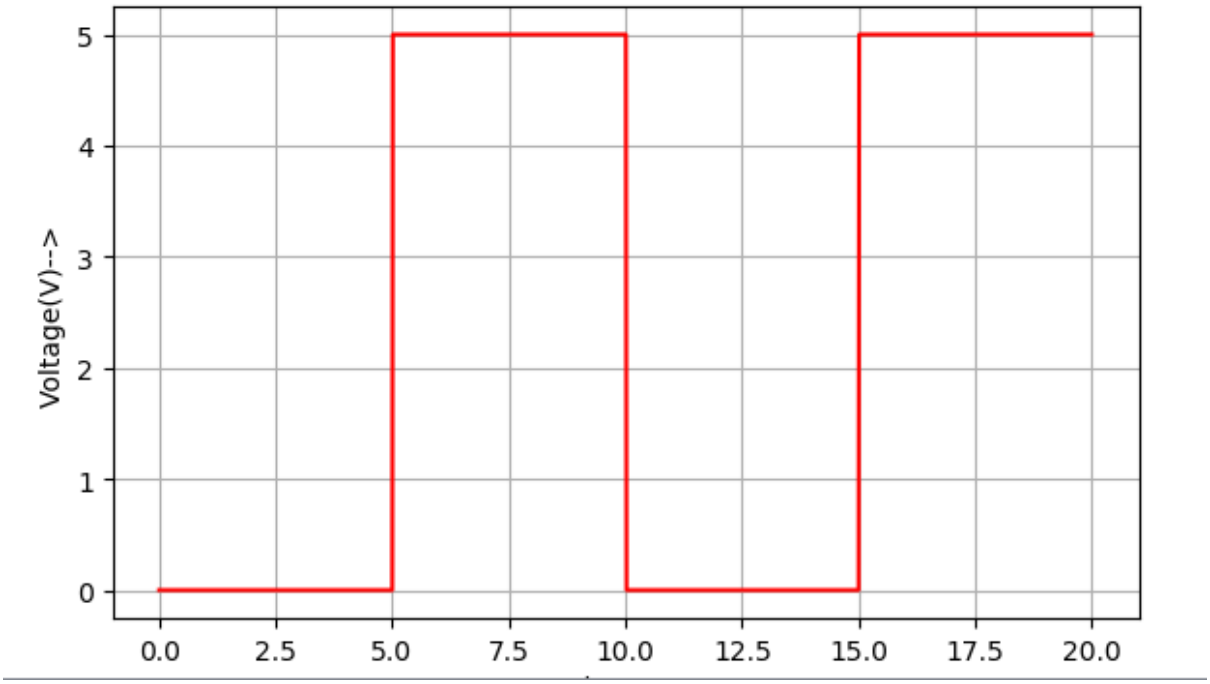

V
v(sum)
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0.0 1.0 2.0 3.0 4.0 5.0 6.0 7.0 8.0 9.0 10.0 11.0 12.0 13.0 14.0 15.0 16.0 17.0 18.0 19.0 20.0
time
s

Carry:

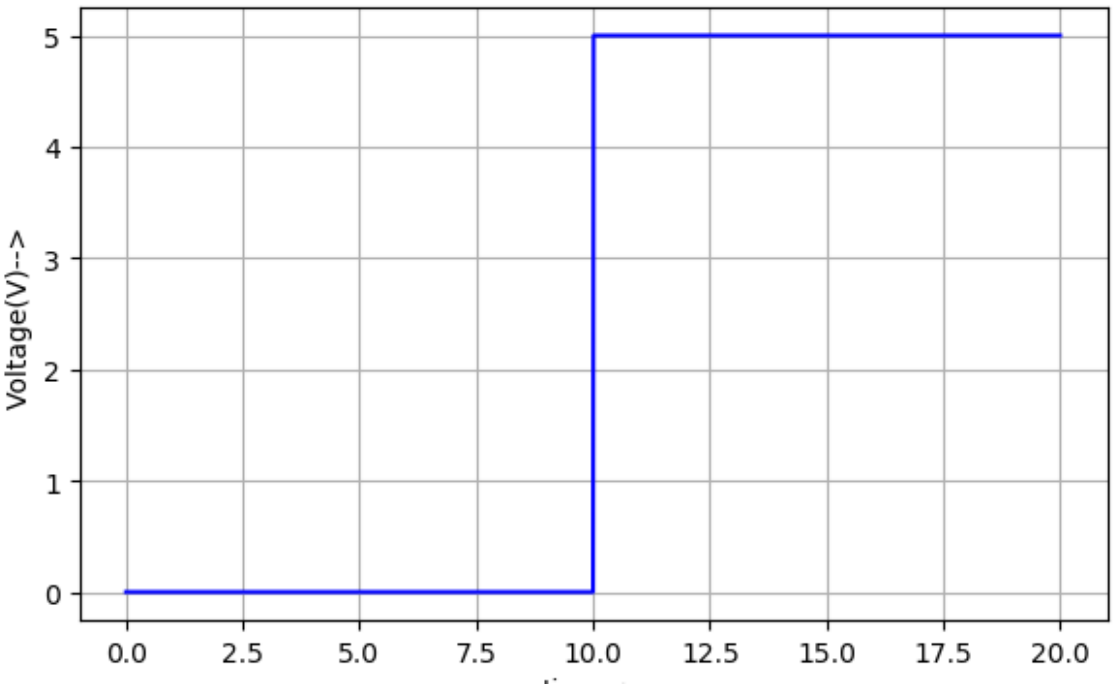


2. Python Waveforms:

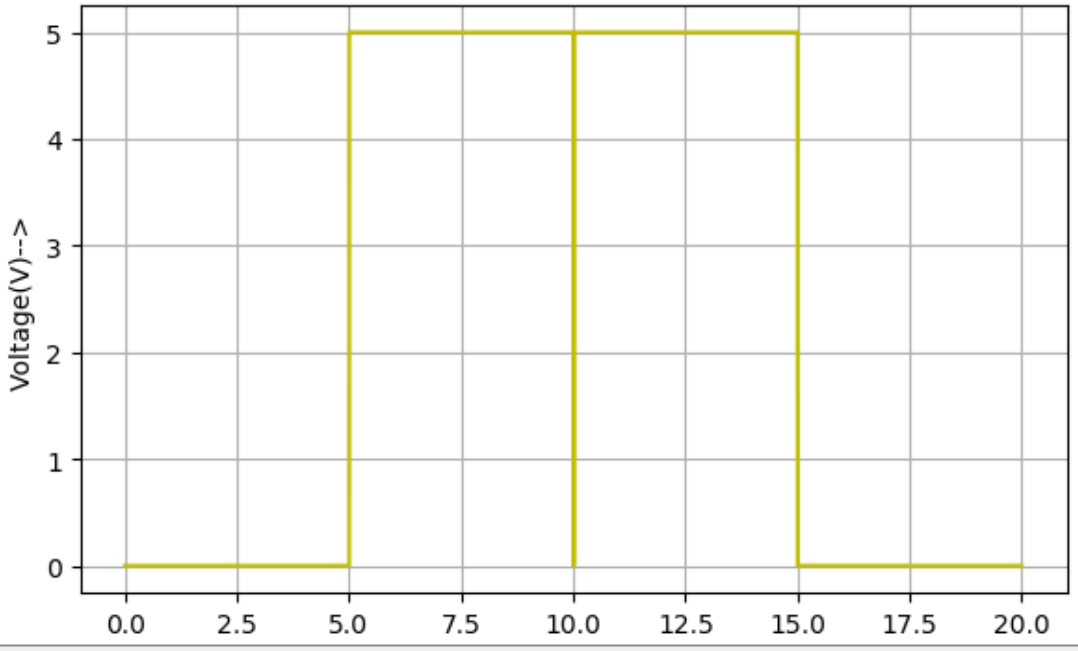
V(a):



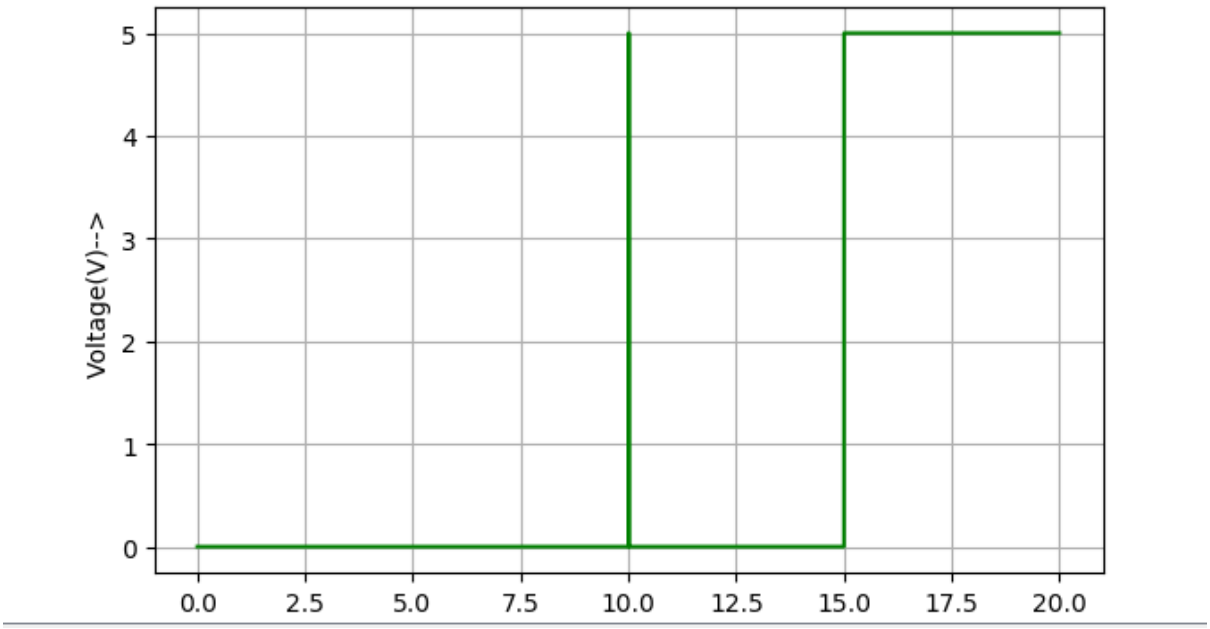
V(b):


Voltage(V)-->
0
1
2
3
4
5
0.0
2.5
5.0
7.5
10.0
12.5
15.0
17.5
20.0

Sum:


Voltage(V)-->
0
1
2
3
4
5
0.0
2.5
5.0
7.5
10.0
12.5
15.0
17.5
20.0

Carry:



Conclusion:

Thus, half adder was designed and the output plots were verified using esim.

References:

https://electronicscoach.com/half-adder.html