Circuit Simulation Project

https://esim.fossee.in/circuit-simulation-project

Name of Participant : Akash S

Project Guide : Dr. Maheswari. R

Title of Project :

Design of Half Adder using NAND gates only and esim subcircuit builder

Theory/Description:

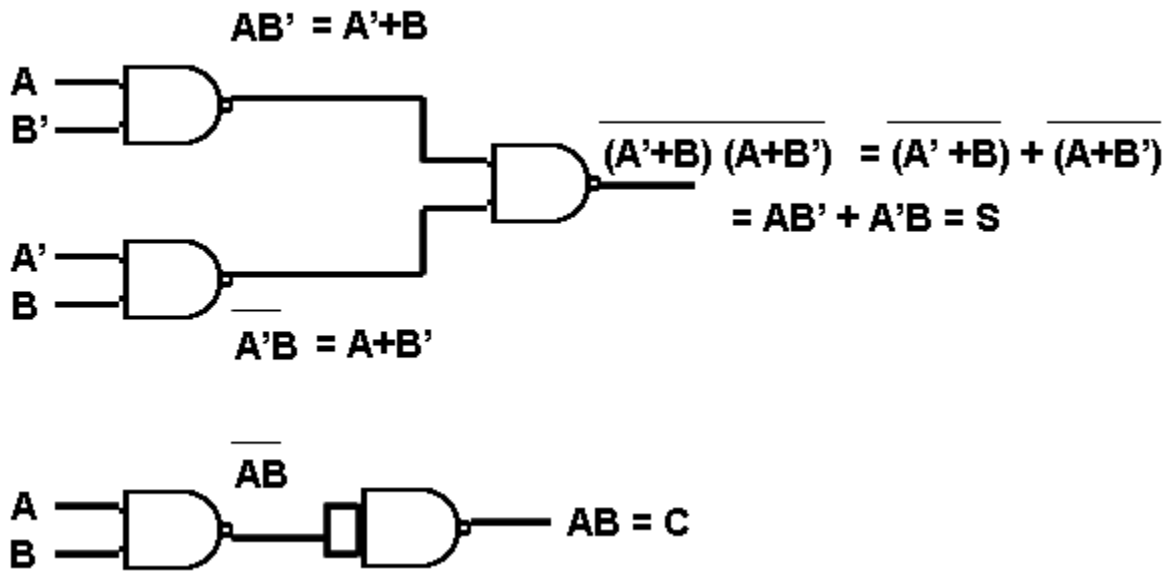
A half adder is a combinational circuit which is used to add numbers. Its input includes the augend and the addend bits. It produces a Sum bit (S) and a Carry bit (C) as its output.

These half adders are extensively used in Arithmetic and Logic Units. They can also act as building blocks in building a full adder circuit. Half adders are also preferred when it comes to the design of calculators and they are also used in calculating addresses and tables in computer systems.

It is possible to build a half adder only with the help of NAND gates since it is a universal gate.

About 5 NAND gates are required in order to build a complete full adder.

Here A and B are the input bits and ‘S’ refers to the Sum bit and ‘C’ refers to the carry bit.



The truth table for half adder circuit :

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Circuit Diagrams:

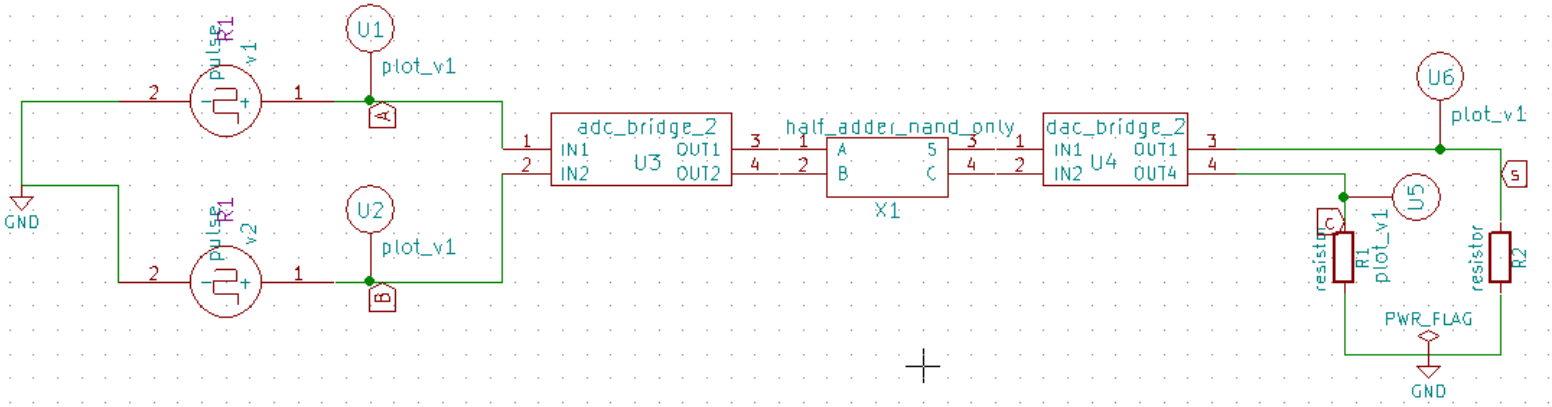


Figure 1: Main Circuit Schematic

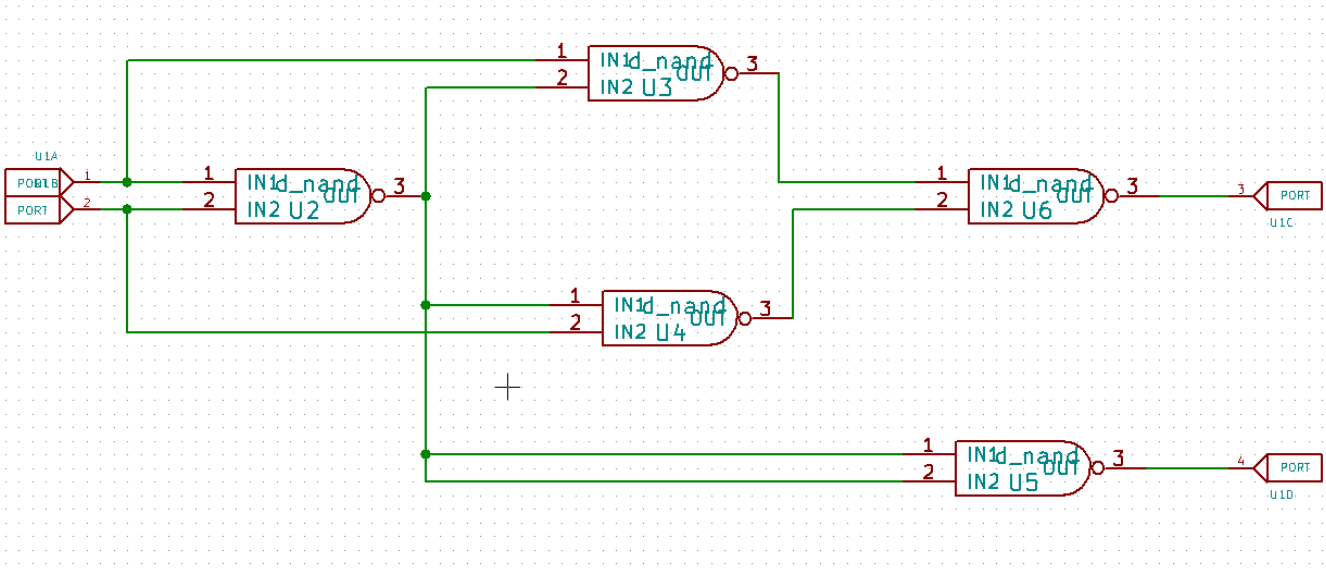


Figure 2: Sub-Circuit Schematic of half adder using NAND gates

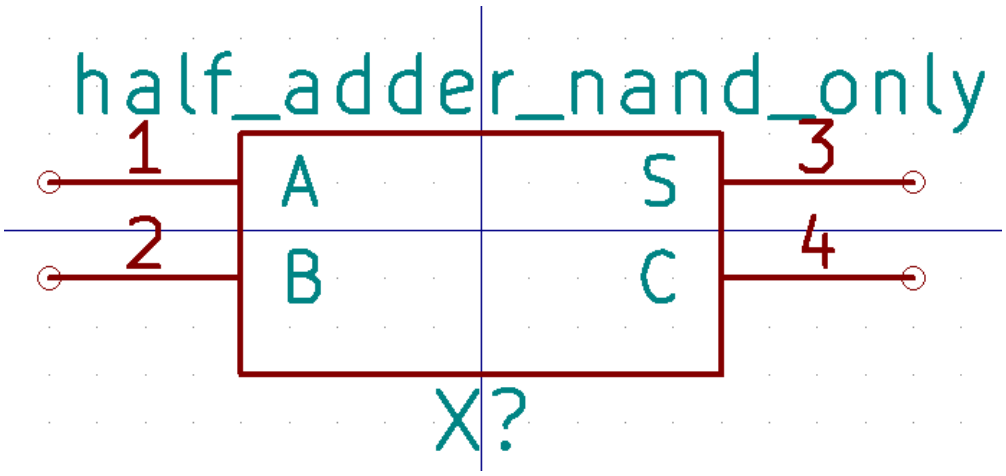
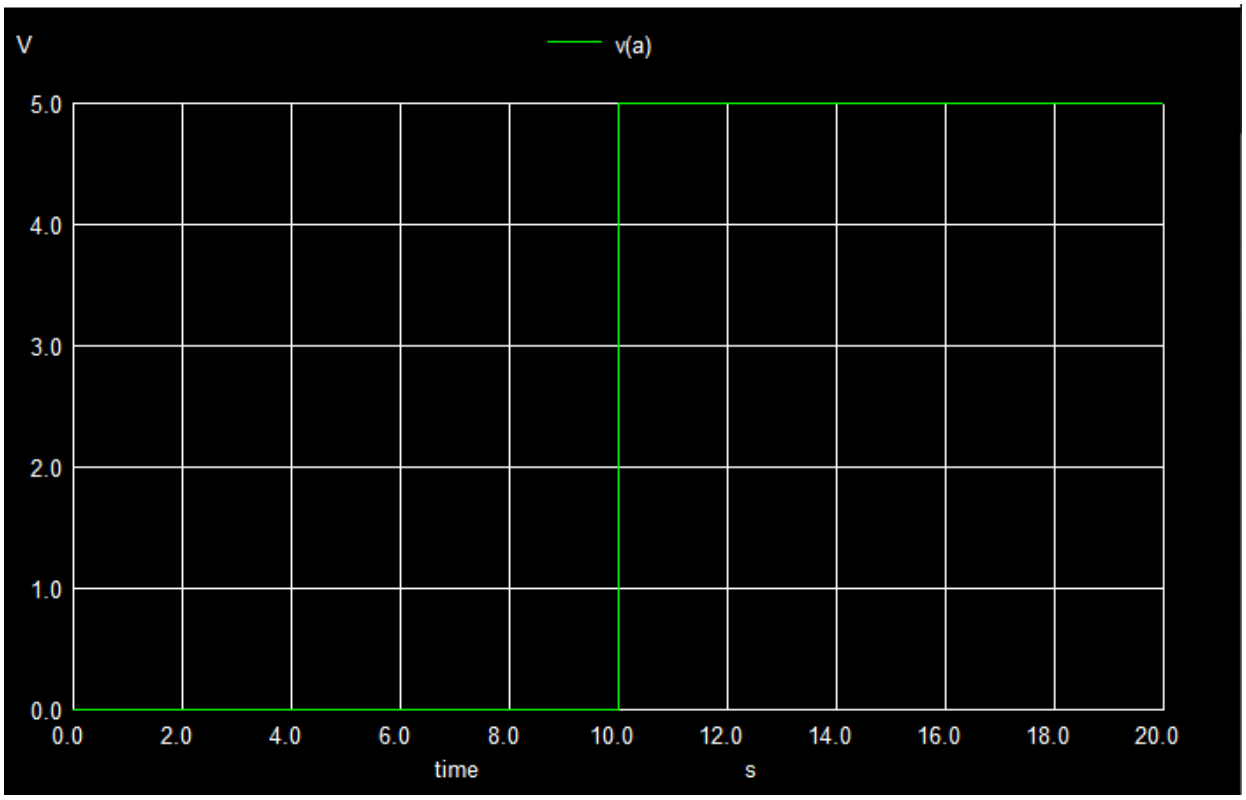


Figure 3: Symbol for half adder using nand gates

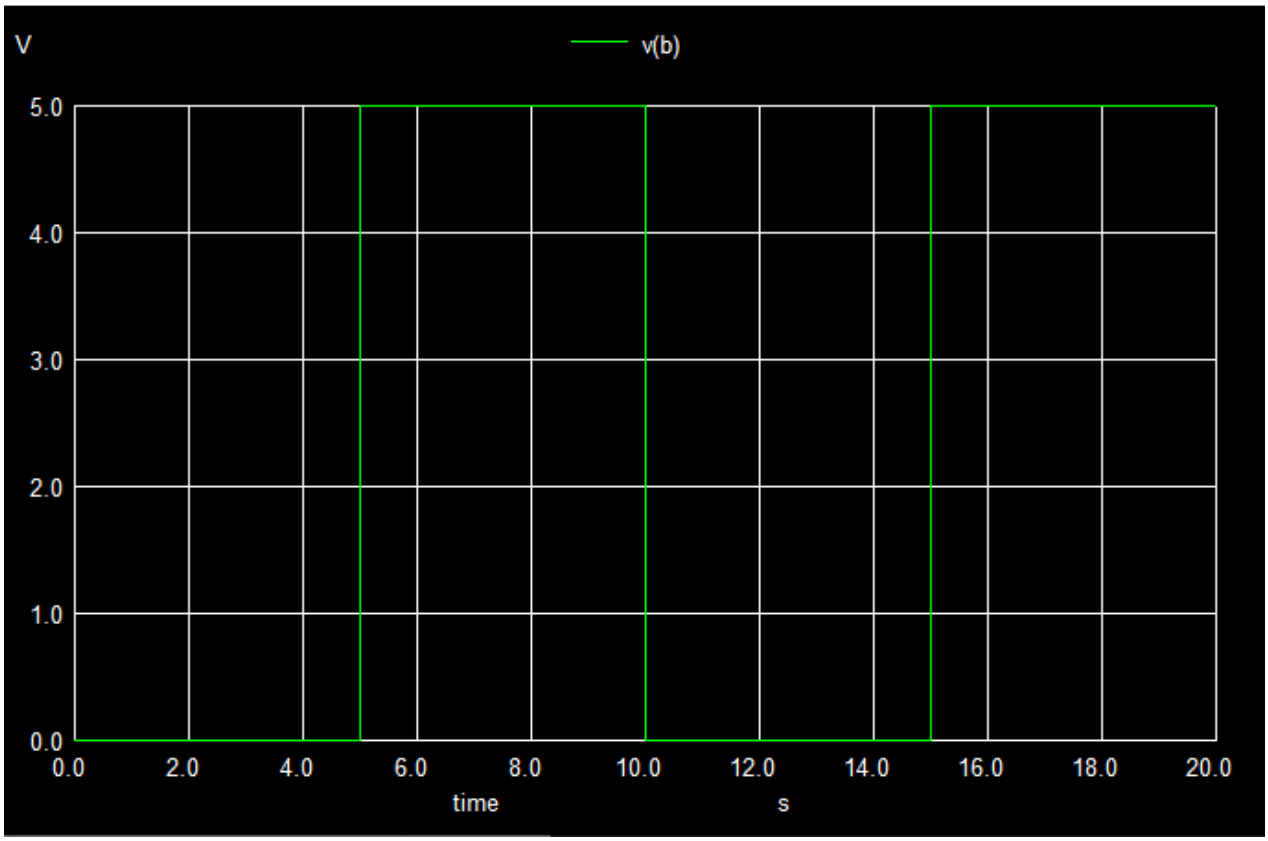
Result/Output:

- **Ngspice Plots :**

  Inputs :

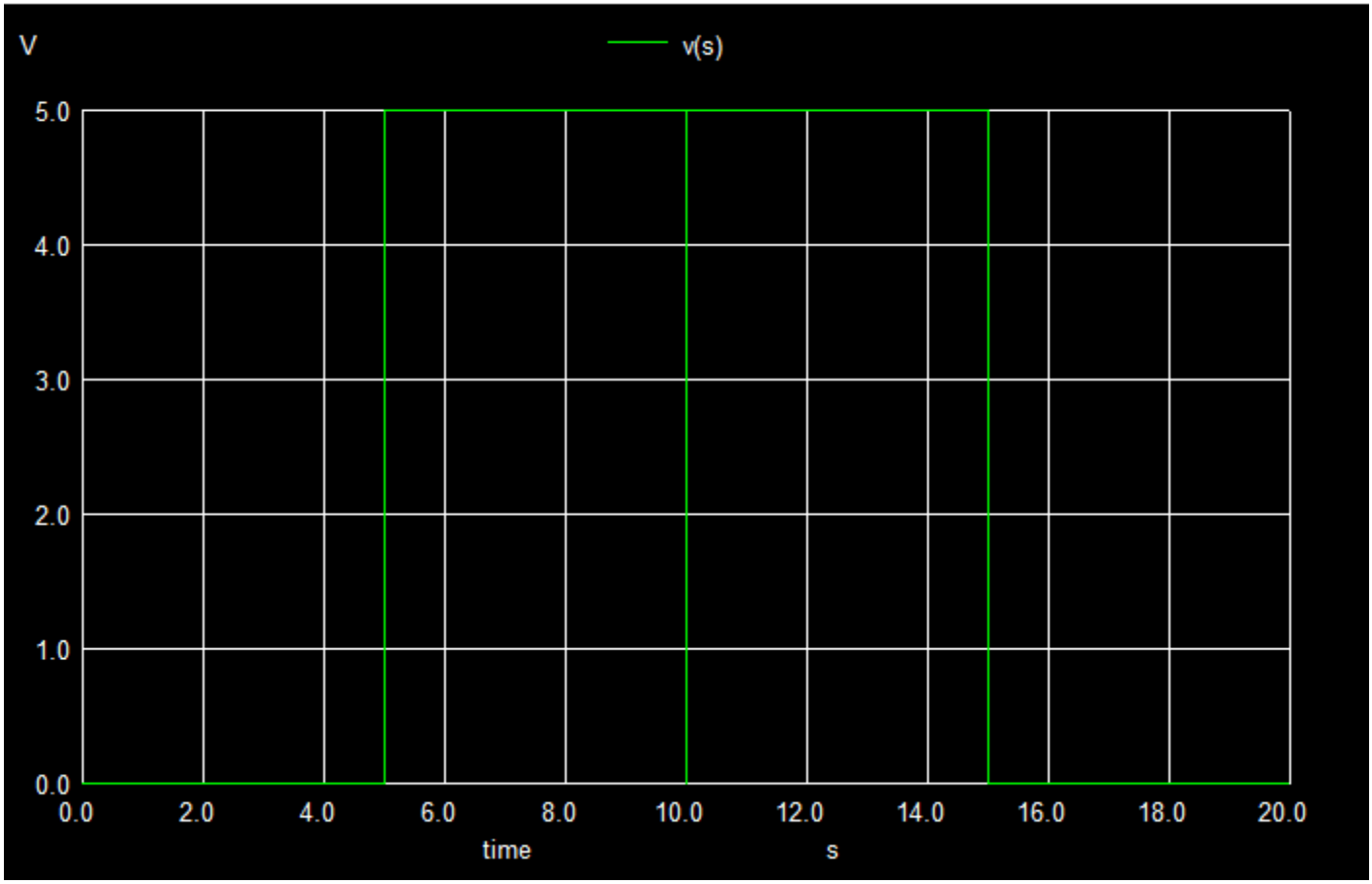


A

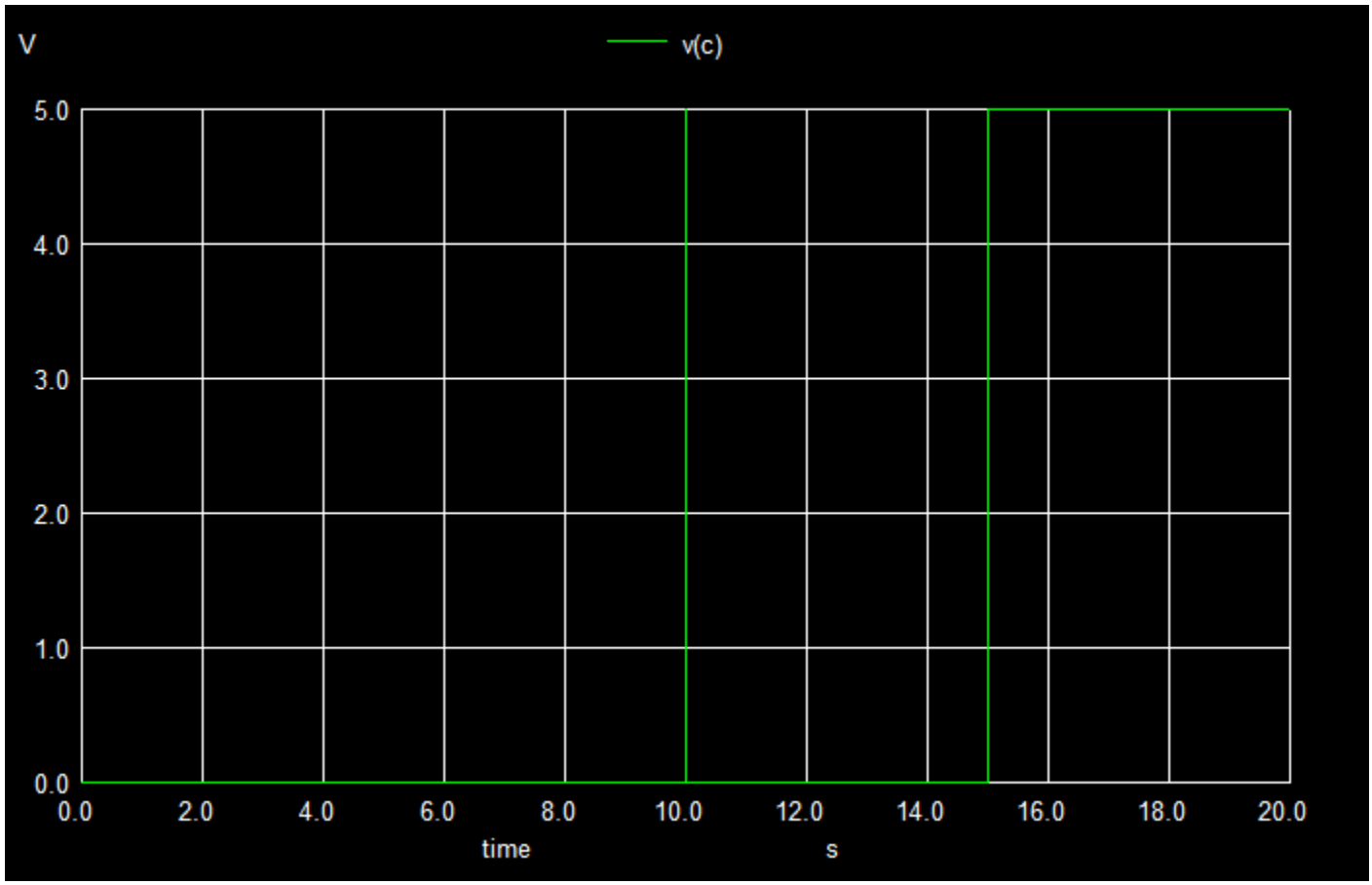


B

Outputs :


V
v(s)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
2.0
4.0
6.0
8.0
10.0
12.0
14.0
16.0
18.0
20.0
time
s

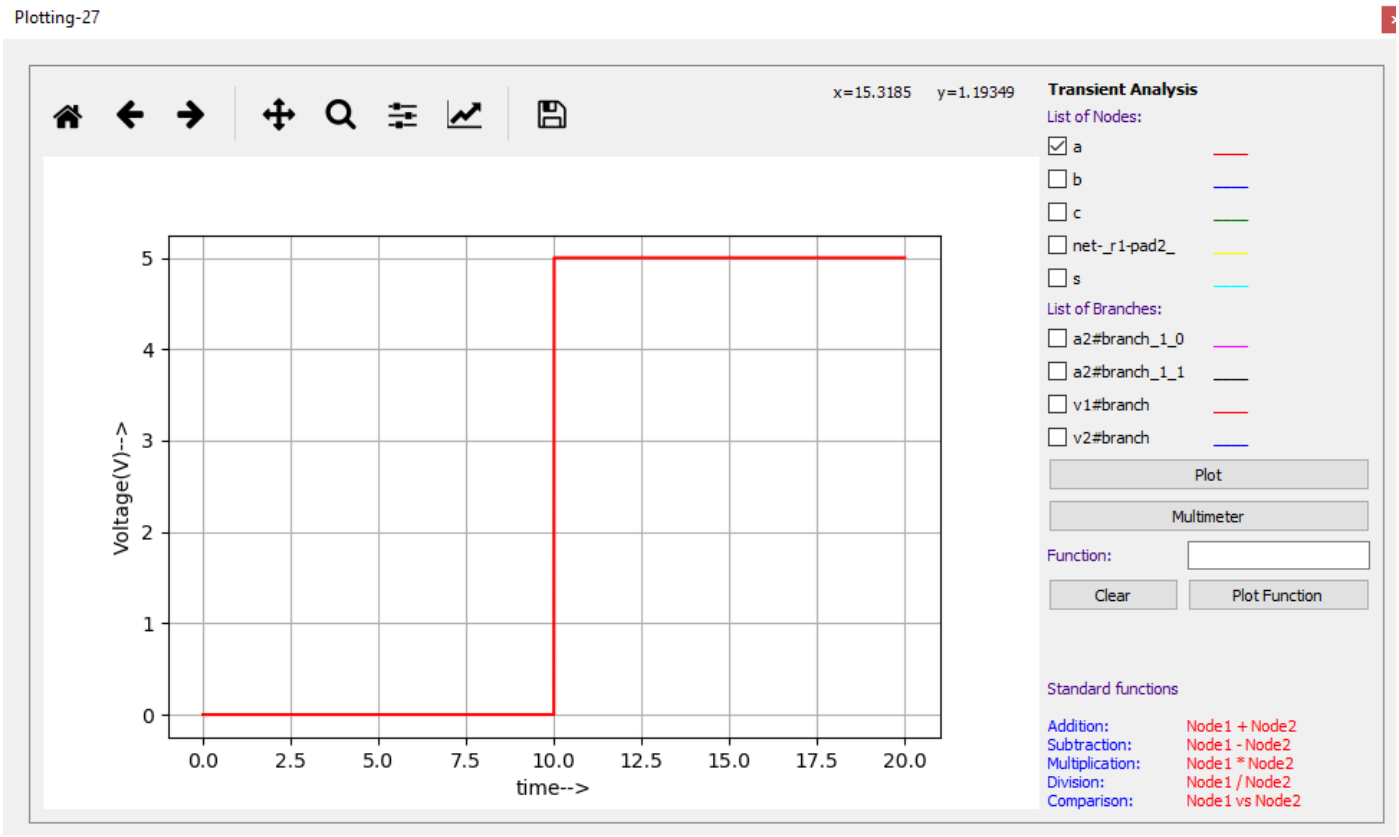
S


V
v(c)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
2.0
4.0
6.0
8.0
10.0
12.0
14.0
16.0
18.0
20.0
time
s

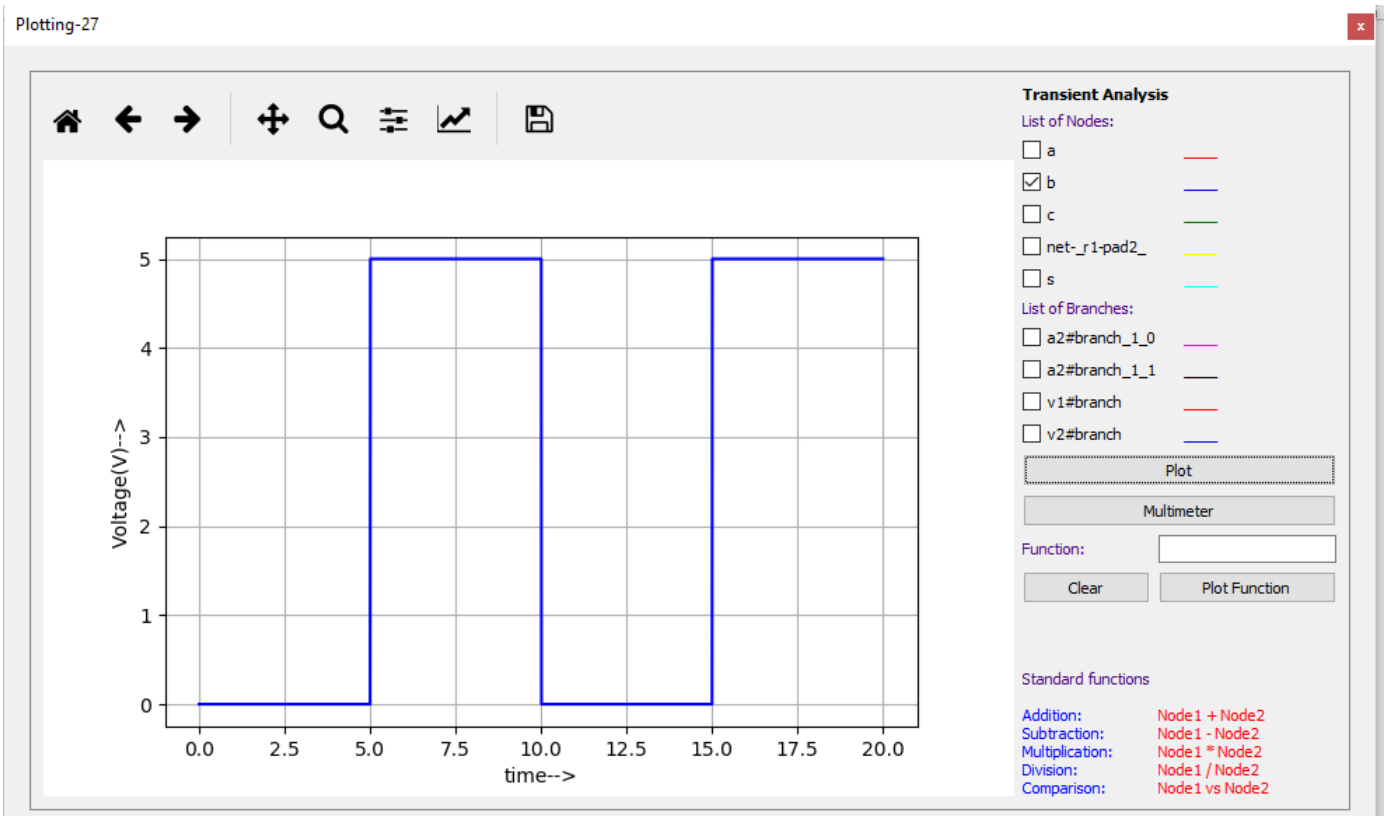
C

- **Python Plots :**

Inputs :

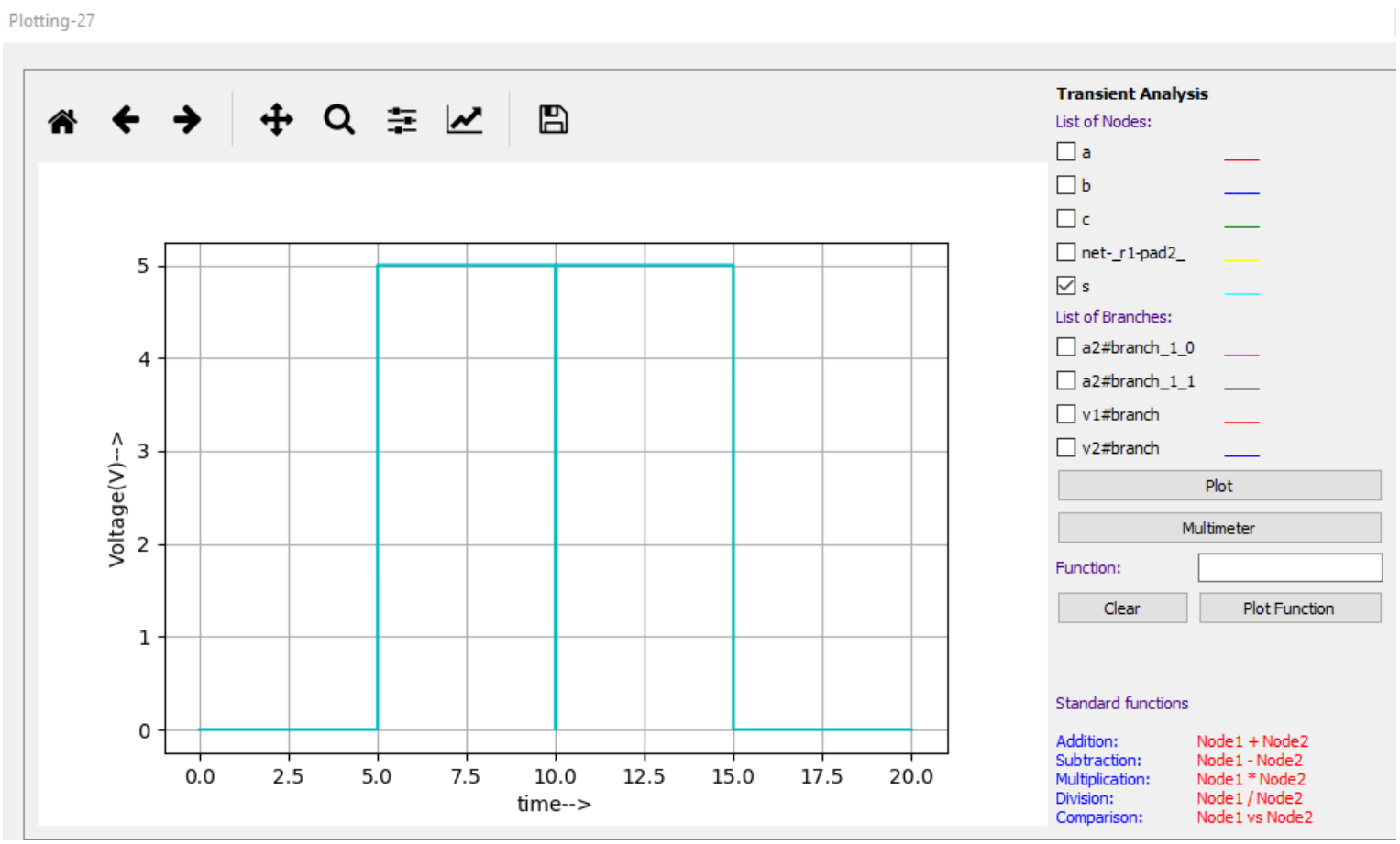


A

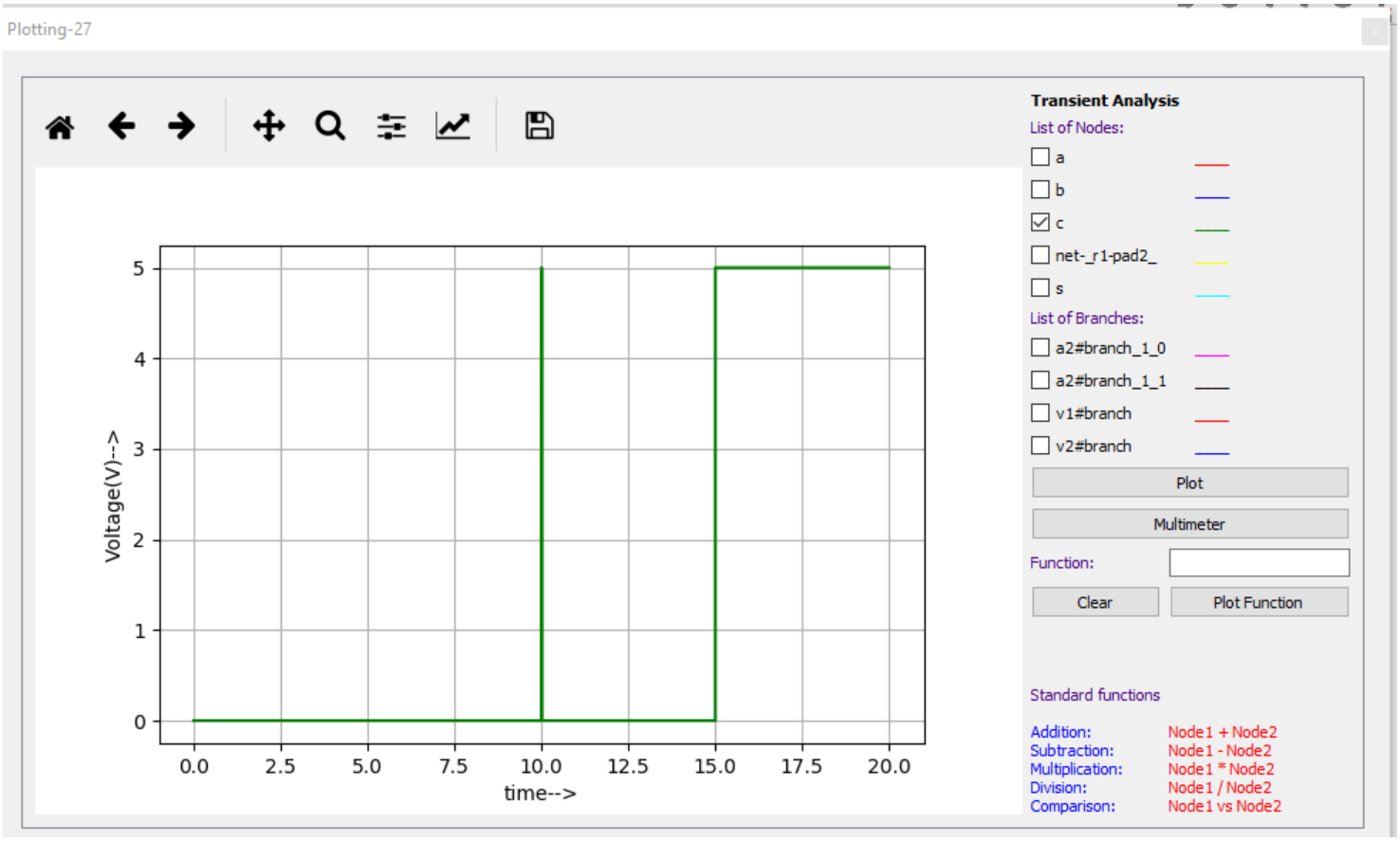


B

Outputs :


Plotting-27
Transient Analysis
List of Nodes:
a
b
c
net-_r1-pad2_
s
List of Branches:
a2#branch_1_0
a2#branch_1_1
v1#branch
v2#branch
Plot
Multimeter
Function:
Clear
Plot Function
Standard functions
Addition: Node1 + Node2
Subtraction: Node1 - Node2
Multiplication: Node1 * Node2
Division: Node1 / Node2
Comparison: Node1 vs Node2
Voltage(V)-->
time-->

S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Voltage(V)-->
time-->

C

References :

https://de-iitr.vlabs.ac.in/exp/half-full-adder/theory.html

https://www.watelectronics.com/what-is-half-adder-circuit-diagram-its-applications/

https://www.circuitstoday.com/half-adder