Circuit Simulation Project

https://esim.fossee.in/circuit-simulation-project

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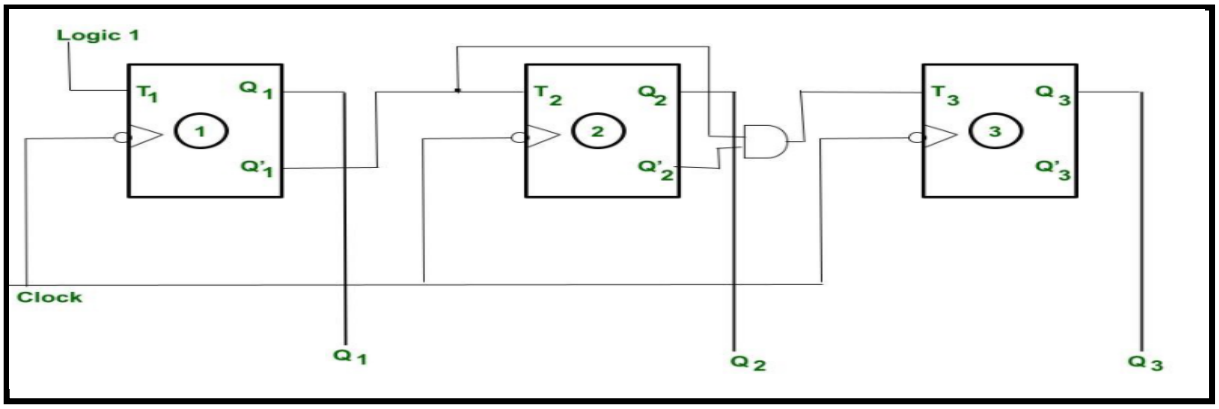
Project Guide: Dr R. Maheswari

Title of the circuit: 3-Bit Synchronous Down Counter

Theory/Description:



In synchronous down counter with JK Flip-Flops, a single clock pulse drives all JK flip-flops. Circuit becomes complex as the number of states increases. Speed is high.

The 3-bit asynchronous up counter consists of 3 JK flip flops and 1 AND gate. The output conditions are Q_2 Q_1 Q_0

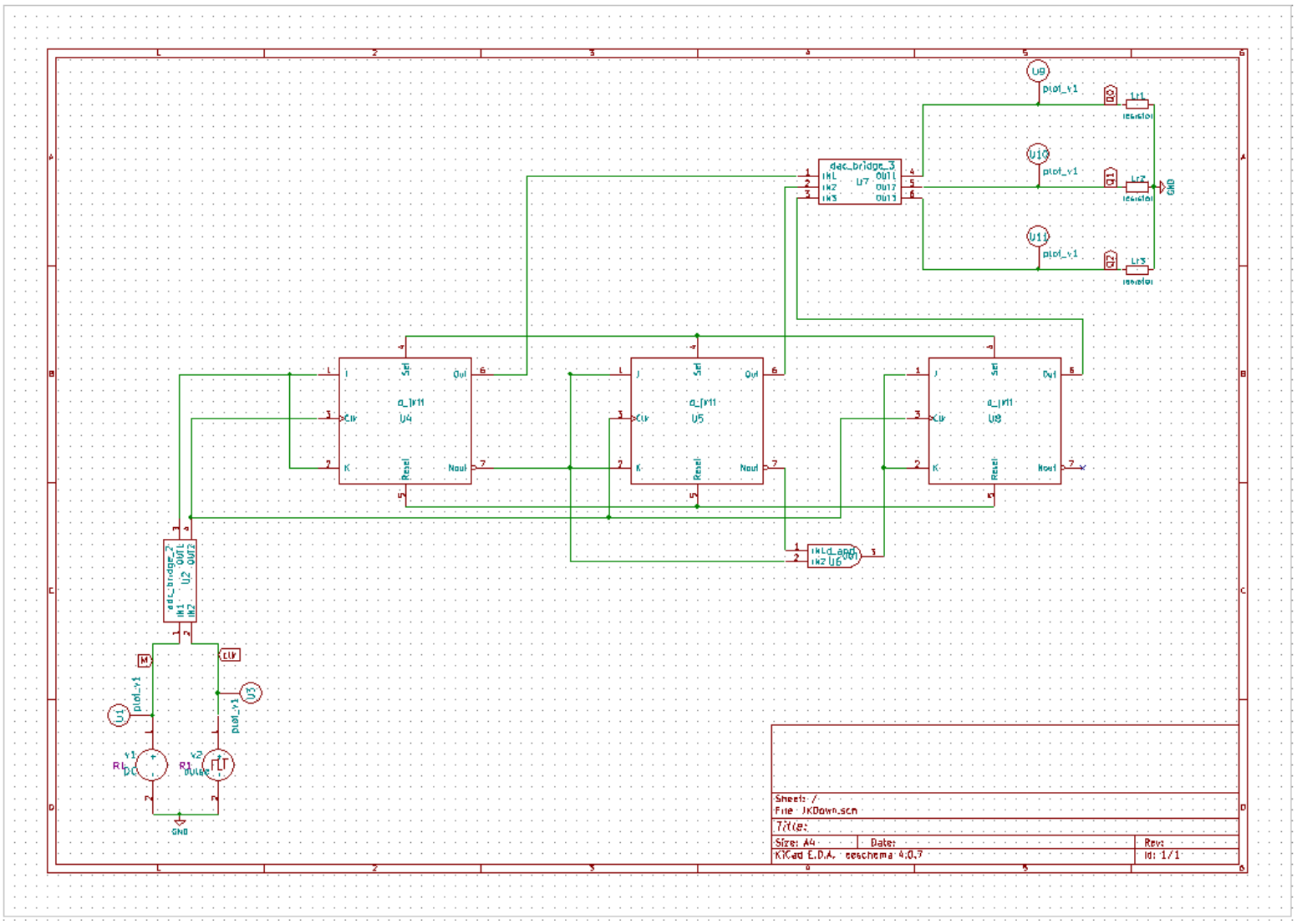
The output of the flip flops is a binary number equivalent to the number of clock pulses received. The output conditions are as shown in the truth table.

Counter State	Q2	Q1	Q0
7	1	1	1
6	1	1	0
5	1	0	1
4	1	0	0
3	0	1	1
2	0	1	0
1	0	0	1
0	0	0	0

e-Sim Required Components

Synchronous Down counter	
Component	**Type**
d_jkff	JK flip flop
pulse	Clock
DC	DC Source for logic high
AND Gate	Logic Gates

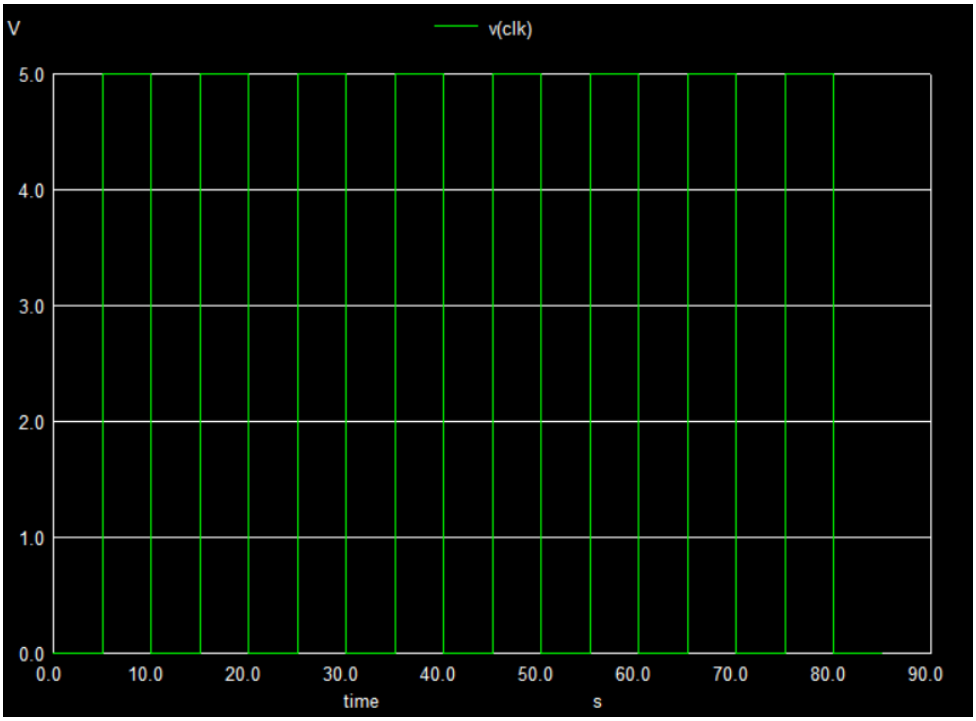
e-Sim Schematic



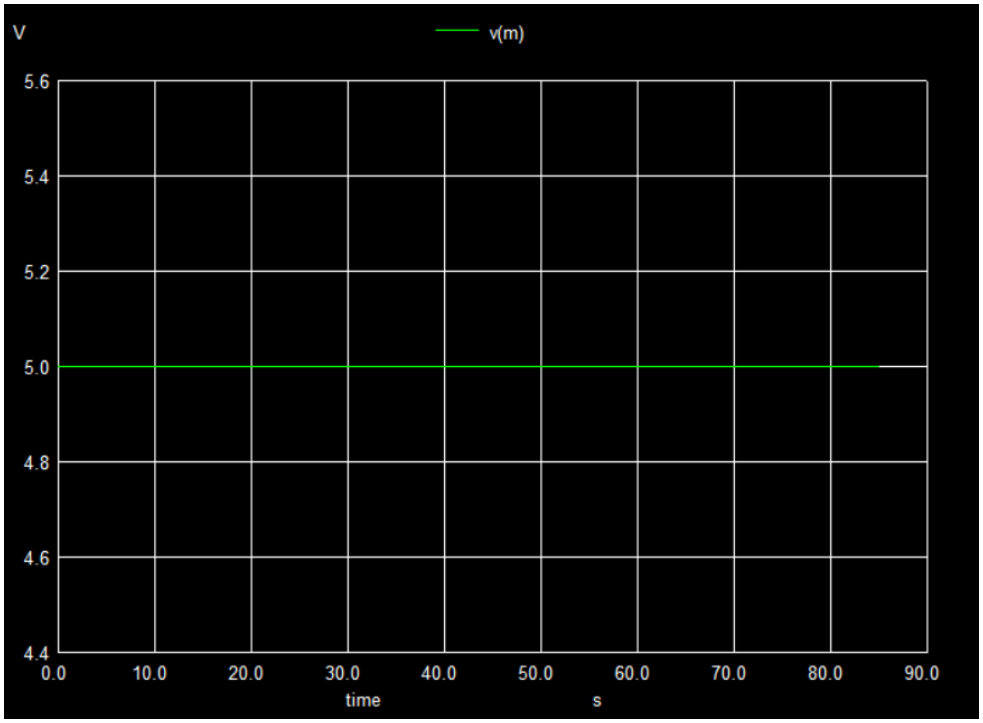
Simulation Result

(i) NG Spice Waveforms:

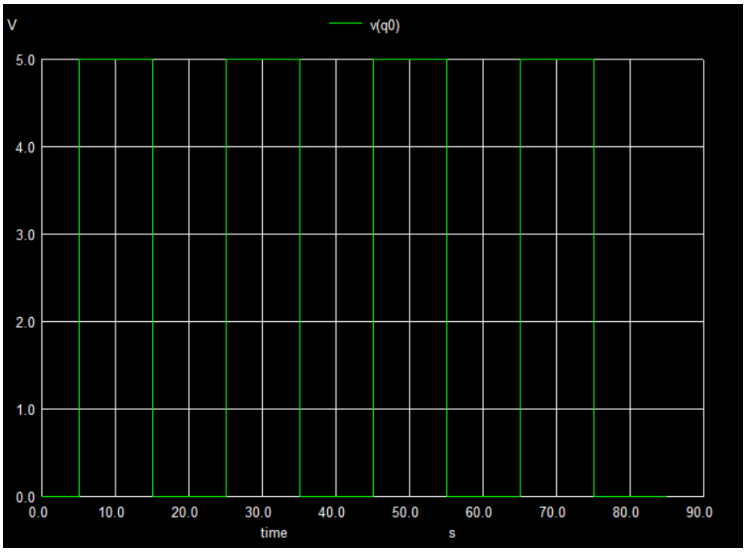
clk (Clock Pulse)



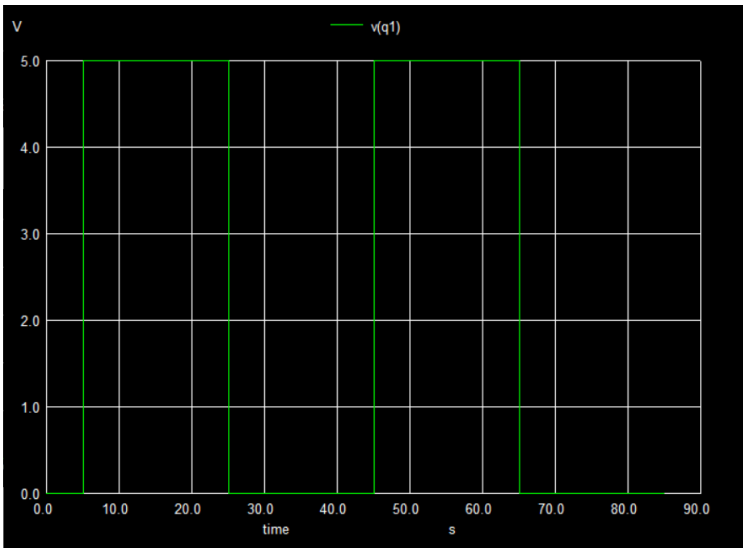
m (Logic High)



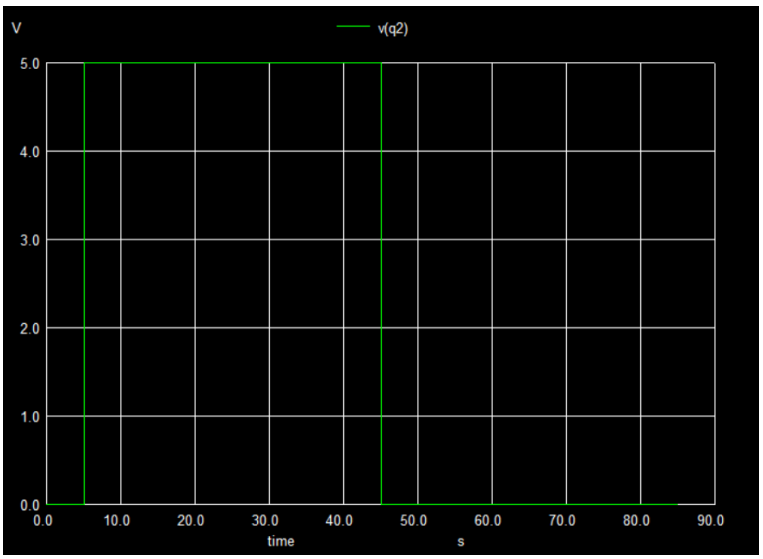
Q_0 (LSB)



Q_1

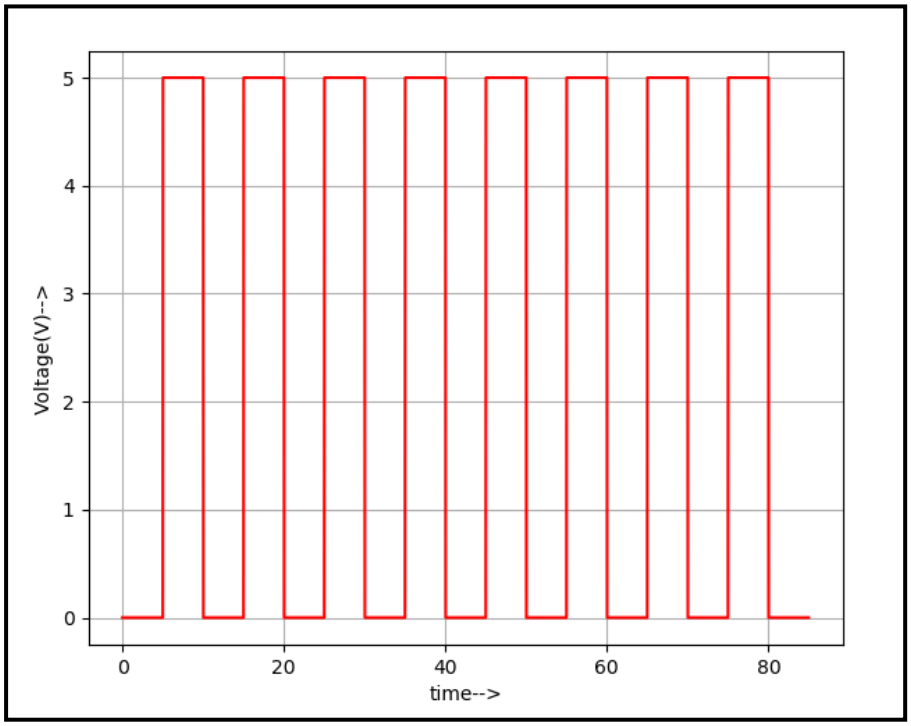


Q_2 (MSB)

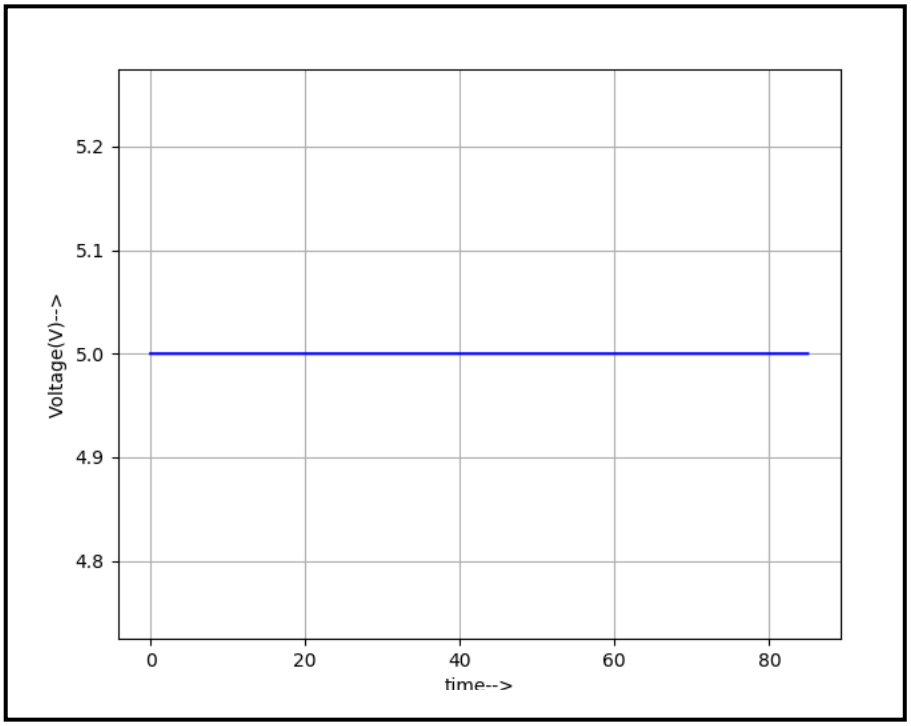


(ii) **Python Waveforms** (for better visualization)

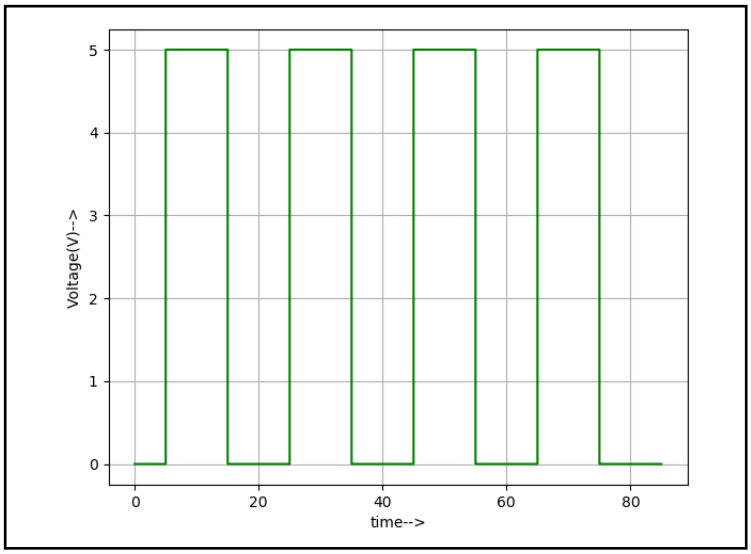
clk



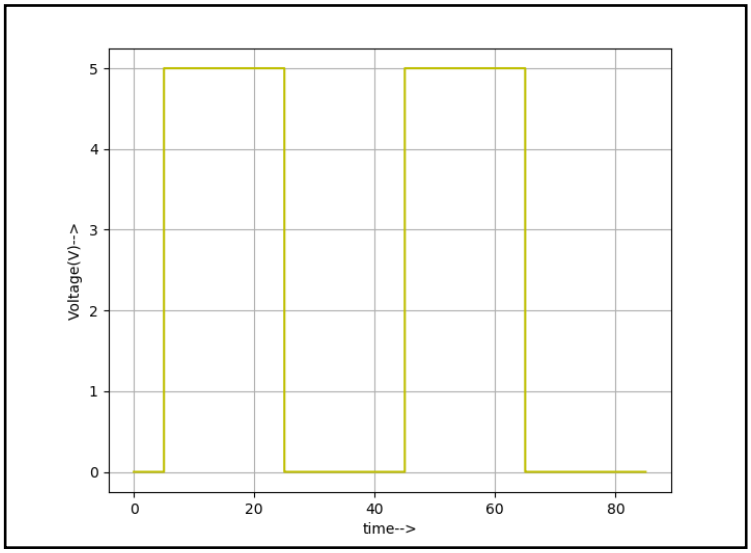
m (Logic High)



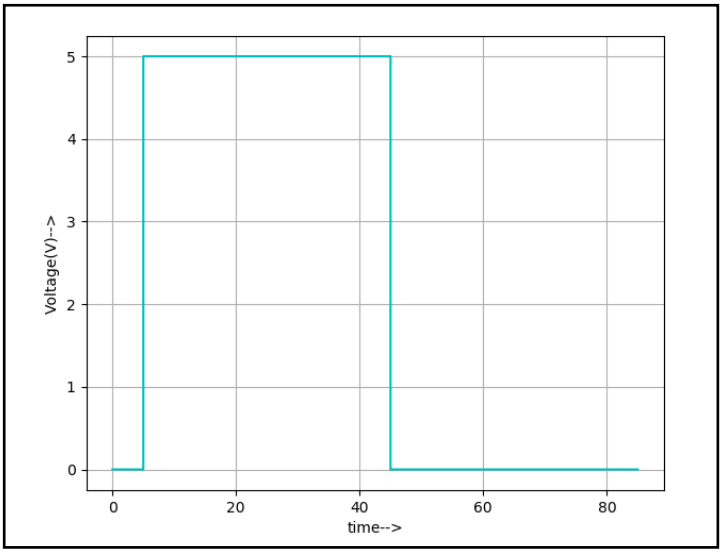
Q_0 (LSB)



Q_1

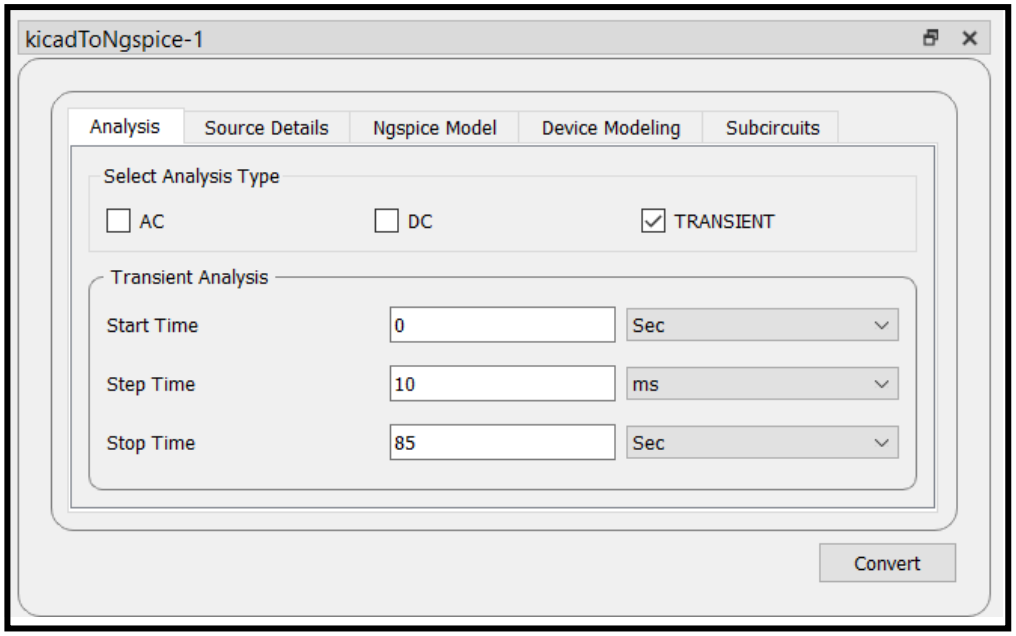


Q_2 (MSB)

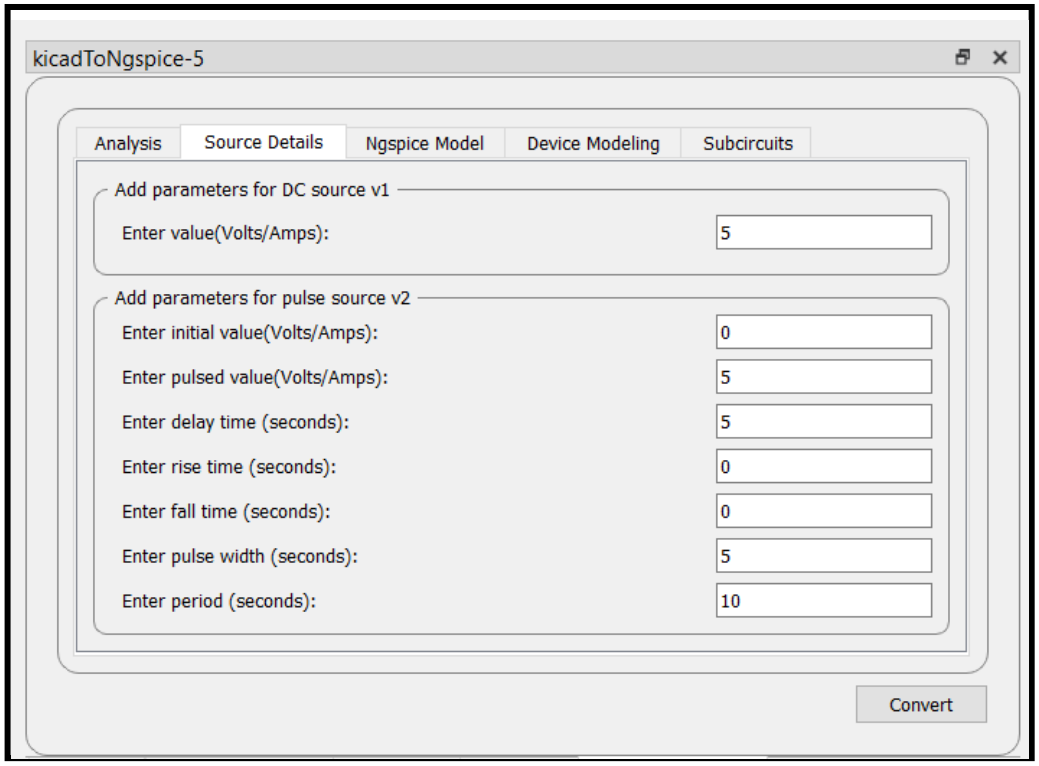


Simulation Parameters for reference:

Transient Analysis



Source Details



Conclusion:

Hence, designed and verified 3-bit synchronous down counter using JK flip flops on eSim

References:

https://www.geeksforgeeks.org/3-bit-synchronous-down-counter/
https://www.tutorialspoint.com/digital_circuits/digital_circuits_counters.htm