Circuit Simulation Project

https://esim.fossee.in/circuit-simulation-project

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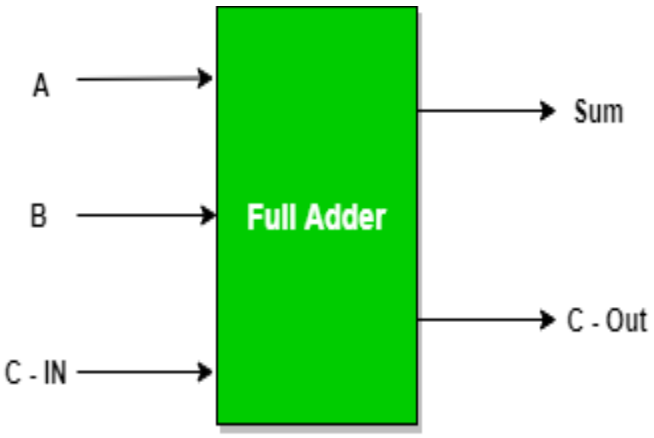
Project Guide: Dr. Maheshwari. R

Project Name: Design of full Adder using NOR gates

Theory:-

Full Adder:-

A full adder is **a digital circuit that performs addition**. Full adders are implemented with logic gates in hardware. A full adder adds three one-bit binary numbers, two operands and a carry bit. The adder outputs two numbers, a sum and a carry bit. The term is contrasted with a half adder, which adds two binary digits.



Full adder Truth Table:-

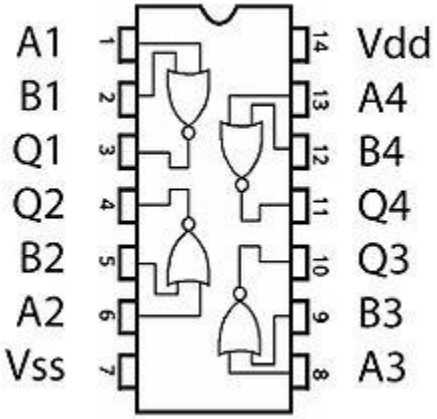
Inputs			Outputs	
A	B	C – IN	Sum	C - Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

NOR Gates:-

The *NOR gate* is a combination OR gate followed by an inverter. Its output is "true" if both inputs are "false." Otherwise, the output is "false."

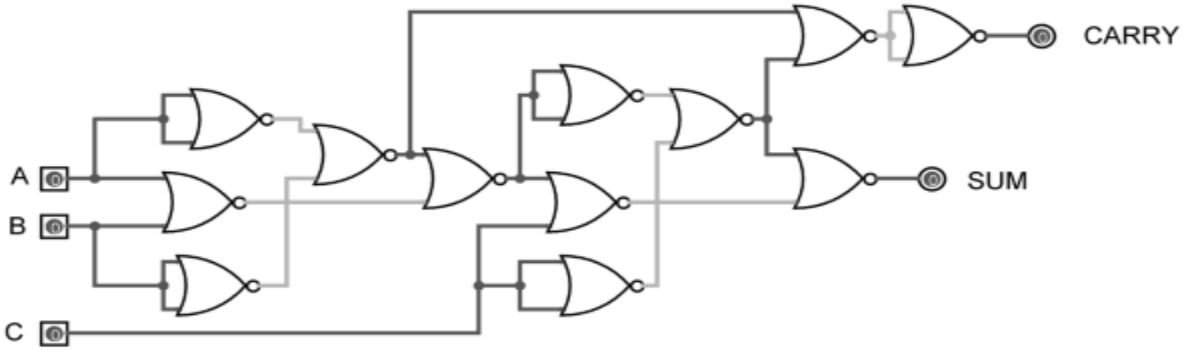
Truth table for NOR gate:-

Inputs		Outputs
X	Y	Z
0	0	1
0	1	0
1	0	0
1	1	0



4001 Quad NOR

Schematic of full adder using NOR gate:-



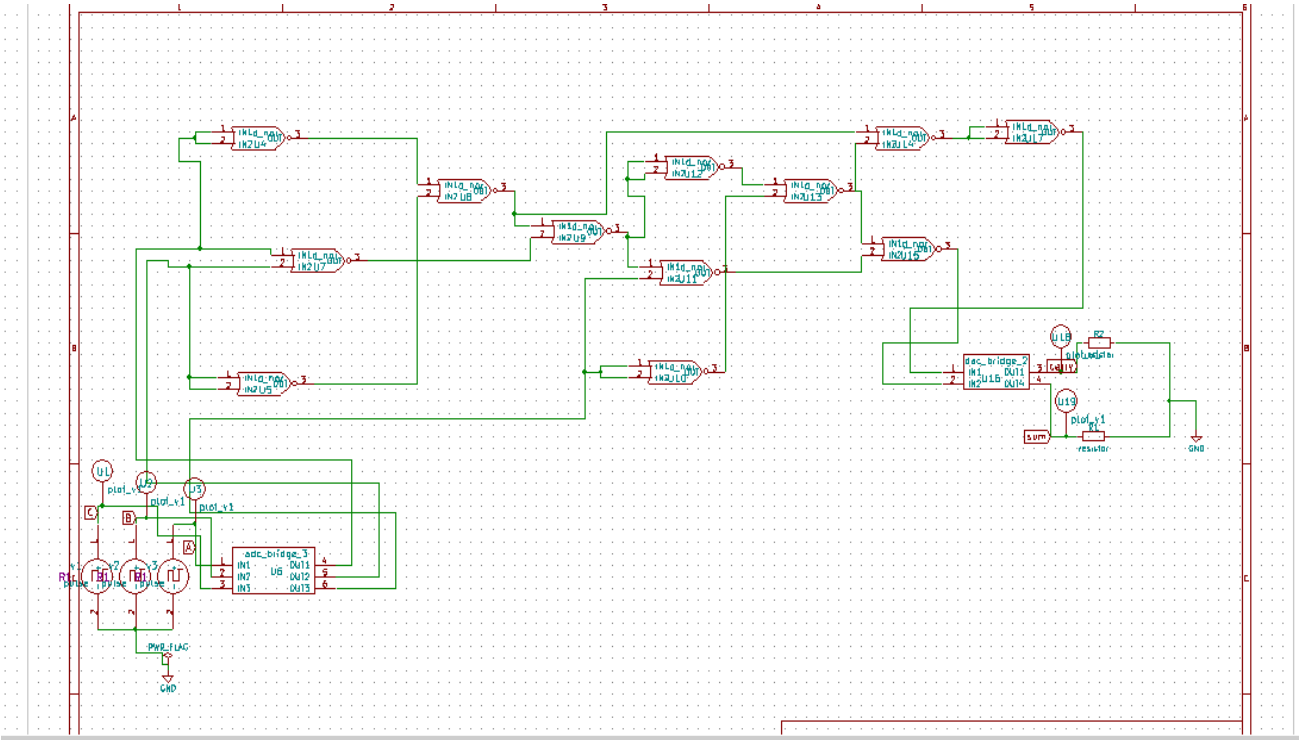
Logical Expression for SUM:

= A’ B’ C-IN + A’ B C-IN’ + A B’ C-IN’ + A B C-IN
= C-IN (A’ B’ + A B) + C-IN’ (A’ B + A B’)
= C-IN XOR (A XOR B)
= (1,2,4,7)

Logical Expression for C-OUT:

= A’ B C-IN + A B’ C-IN + A B C-IN’ + A B C-IN
= A B + B C-IN + A C-IN
= (3,5,6,7)

CIRCUIT DIAGRAM:

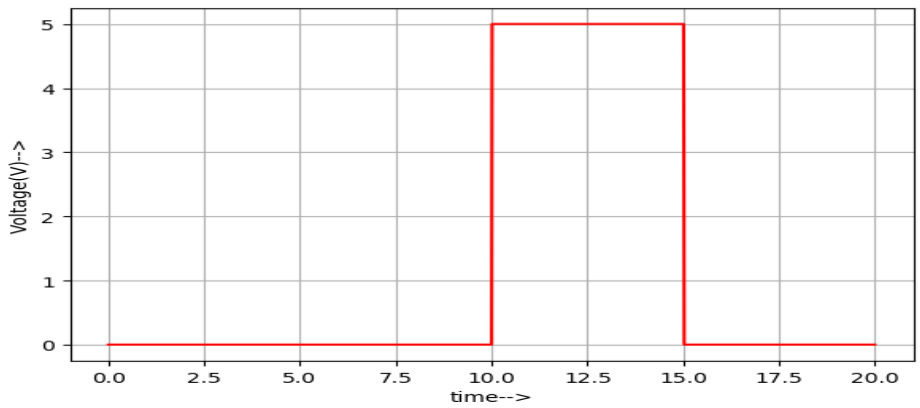


OUTPUTS:-

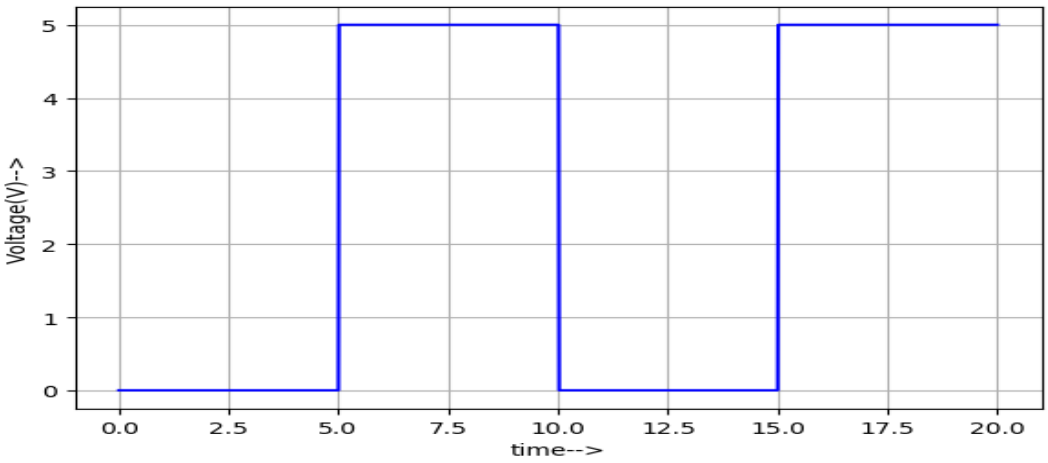
Python plots:-

Inputs:

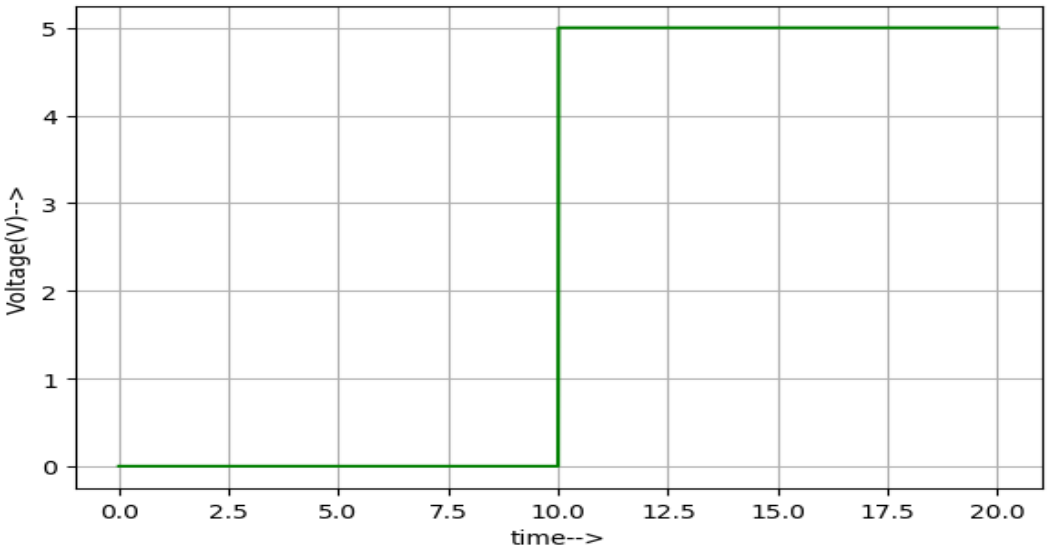
A



B

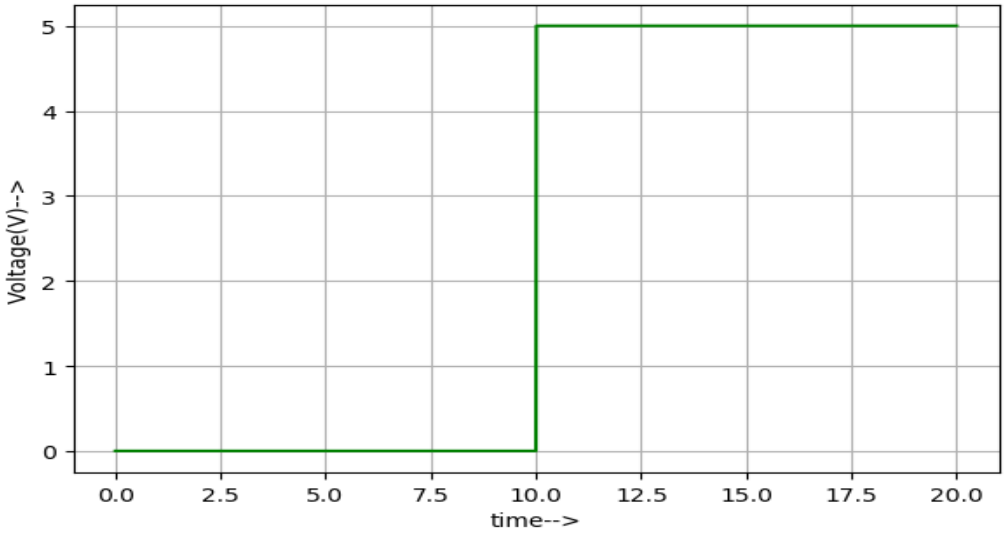


C

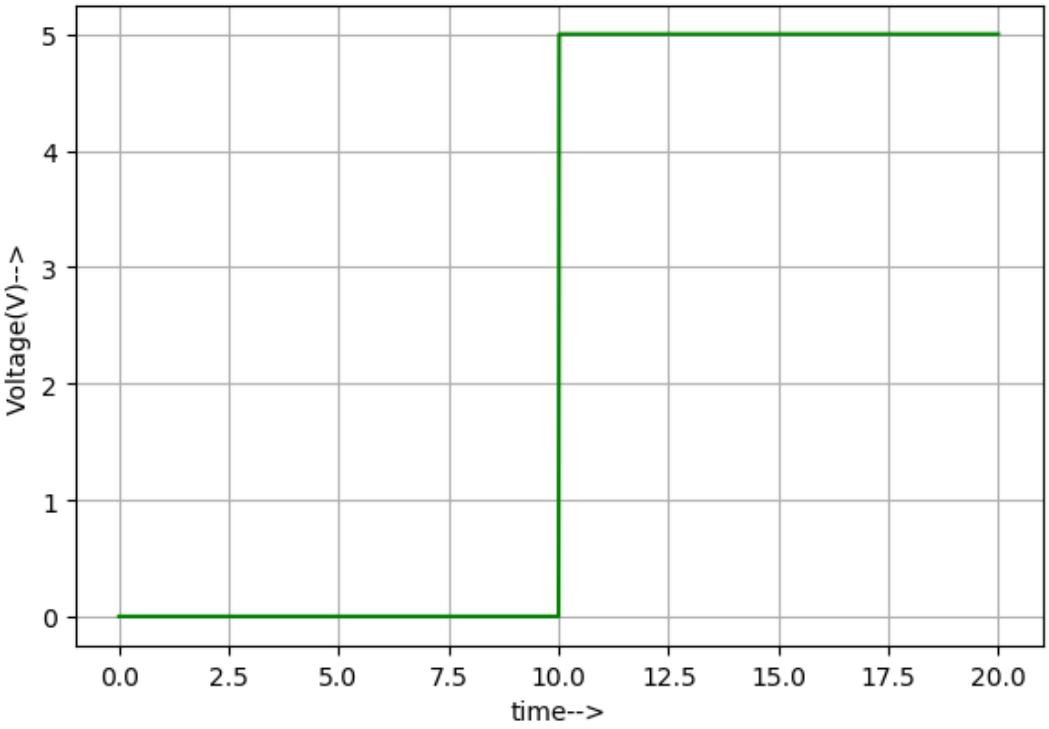


Outputs:-

SUM:-


Voltage(V)-->
time-->
0
1
2
3
4
5
0.0
2.5
5.0
7.5
10.0
12.5
15.0
17.5
20.0

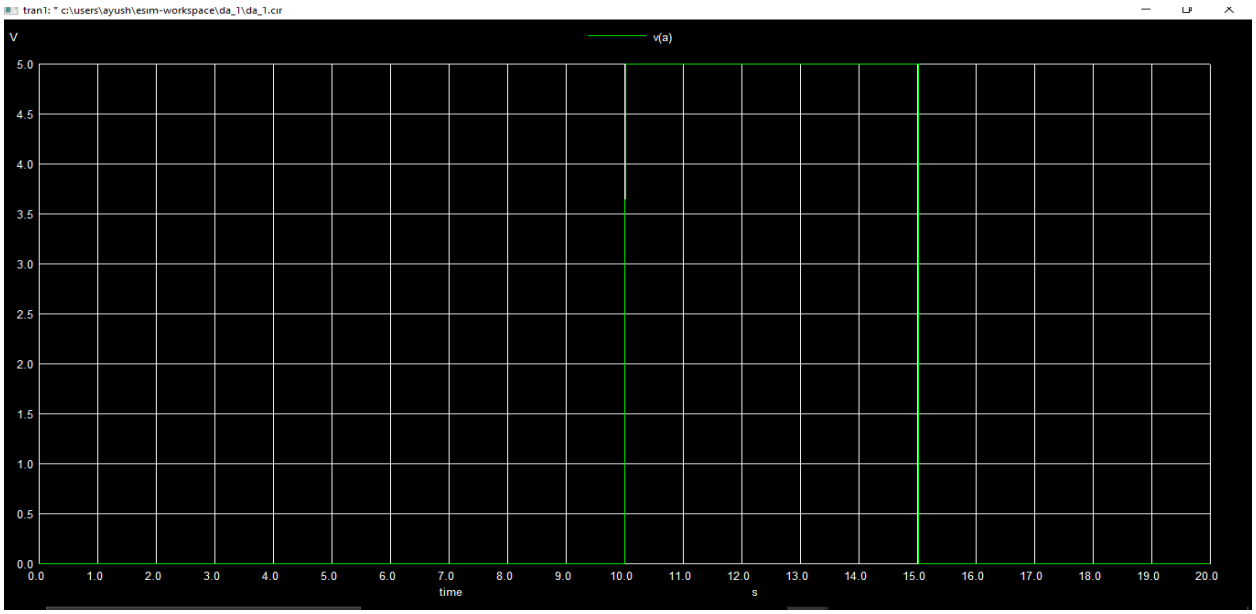
Carry:-


Voltage(V)-->
time-->
0
1
2
3
4
5
0.0
2.5
5.0
7.5
10.0
12.5
15.0
17.5
20.0

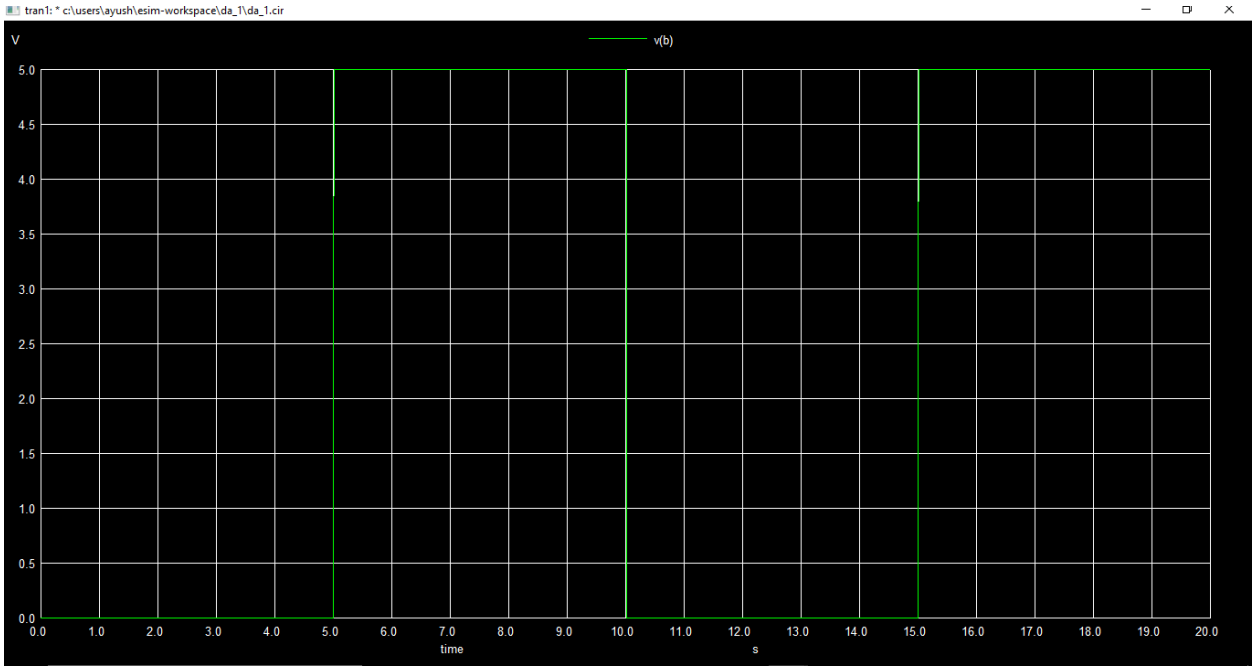
Ngspice Plots:-

Inputs:-

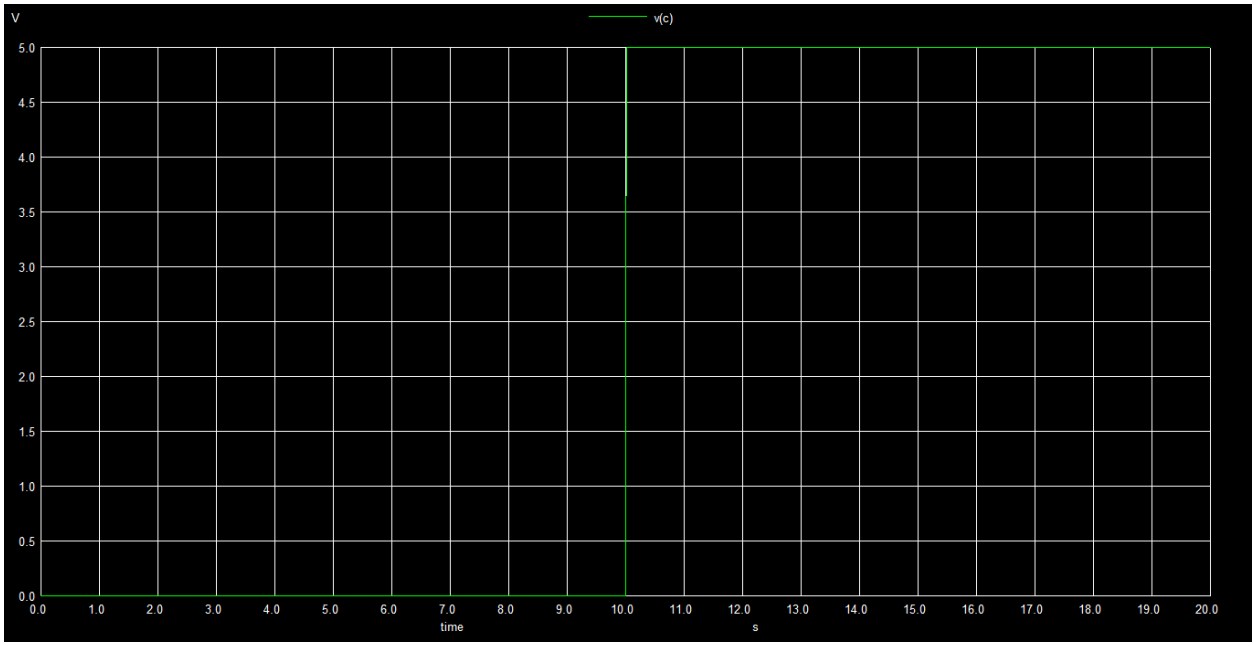
A



B

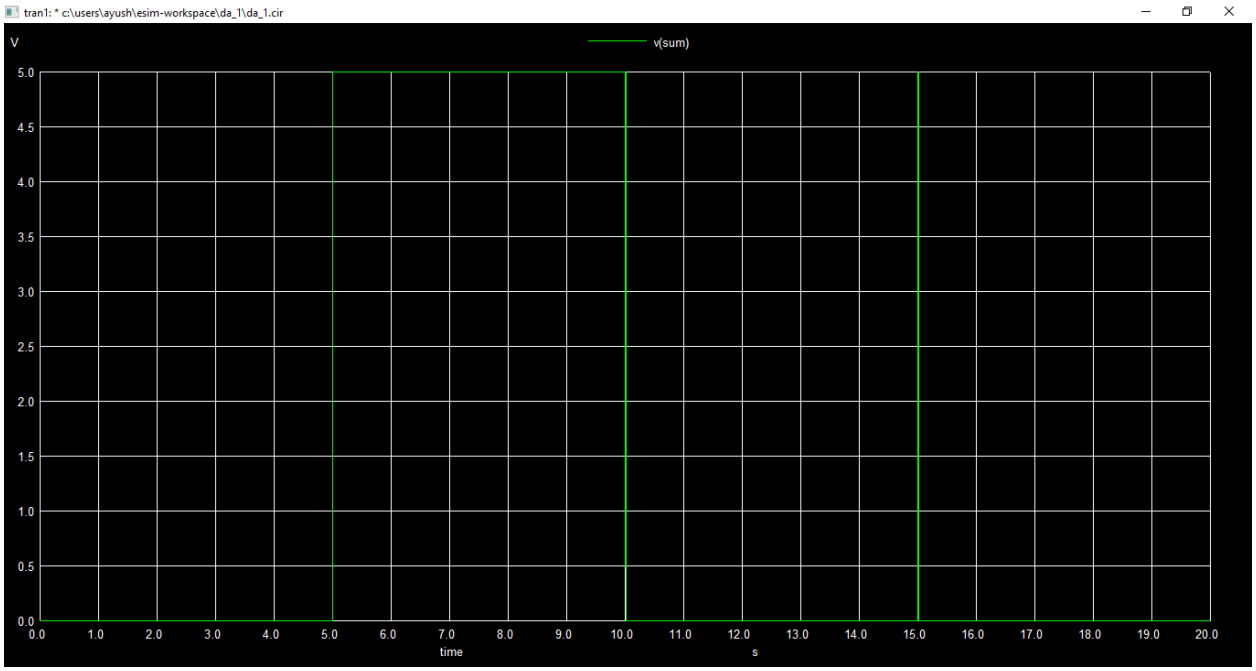


C

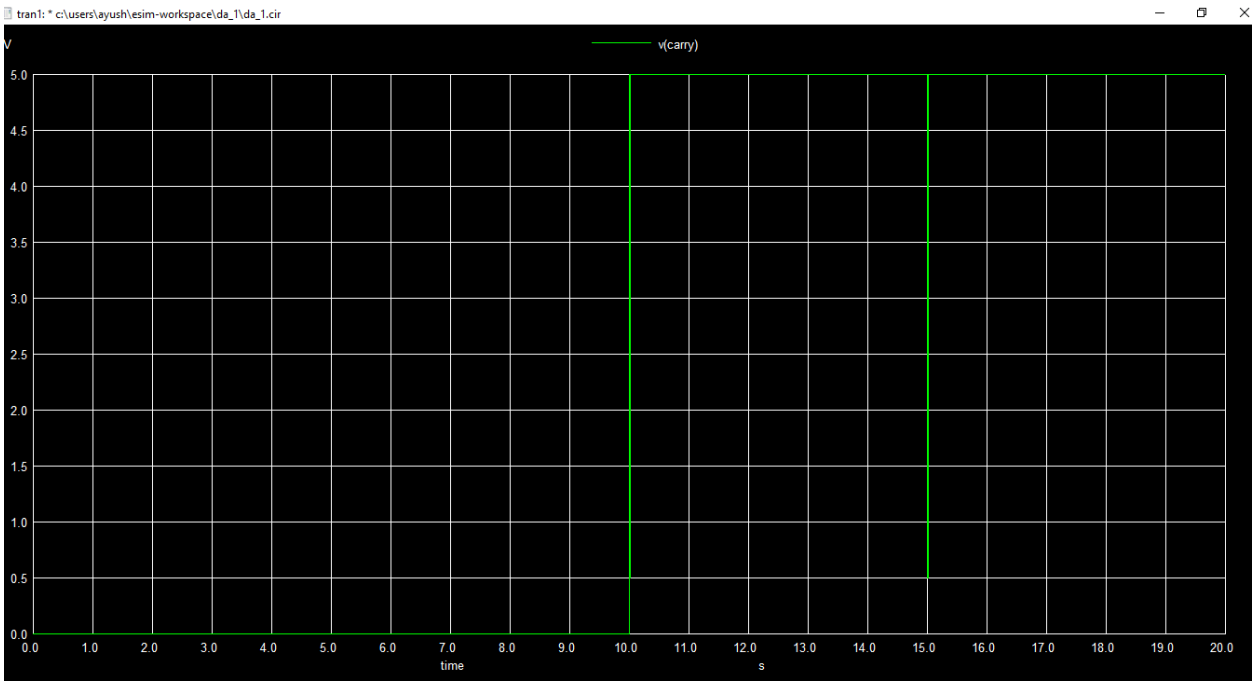


Outputs:-

Sum:-



Carry:-



References:-

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- https://de-iitr.vlabs.ac.in/exp/half-full-adder/theory.html
- https://www.youtube.com/watch?v=9ymwX1Pzybk
- https://vimaxmedia.com/yv85f9/full-adder-using-nor-gate