IMPLEMENTATION OF FULL SUBTRACTOR WITH NOR GATE ONLY

(using two half subtractor sub-circuits with nor gate only)

Theory /description:-

1.TRUTH TABLE FOR HALF SUBTRACTOR :-

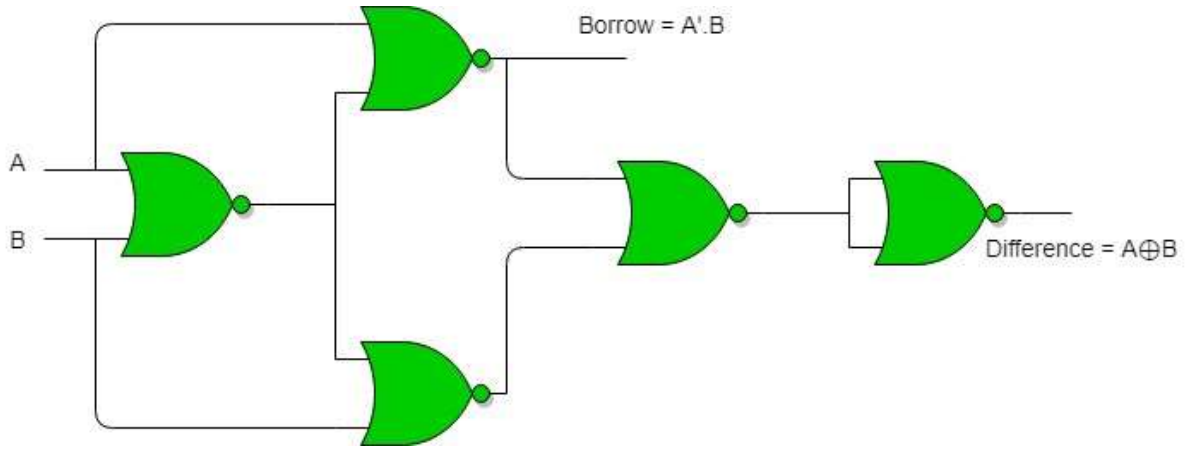
Inputs		Outputs	
A	B	Diff	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

The half subtractor is a building block for subtracting two binary numbers. It has two inputs and two outputs. This circuit is used to subtract two single bit binary numbers A and B. The 'diff' and 'borrow' are two output states of the half subtractor with the above truth table. The SOP form of the Diff and Borrow is as follows:

Diff=A'B+AB'. Borrow = A'B.

2.Implementation of Half Subtractor using NOR gates :

Total 5 NOR gates are required to implement half subtractor.



3.truth table for full subtractor :-

Inputs			Outputs	
A	B	$Borrow_{in}$	Diff	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

A full subtractor is a combinational circuit that performs subtraction of two bits, one is minuend and other is subtrahend, taking into account borrow of the previous adjacent lower minuend bit. This circuit has three inputs and two outputs. The three inputs A, B and Bin, denote the minuend, subtrahend, and previous borrow, respectively. The two outputs, D and Bout represent the difference and output borrow, respectively.

Logical expressions :-

1. D = A'B'Bin + A'BBin' + AB'Bin' + ABBin

= Bin(A'B' + AB) + Bin'(AB' + A'B)

= Bin(A XNOR B) + Bin'(A XOR B)

= Bin (A XOR B)' + Bin'(A XOR B)

= Bin XOR (A XOR B)

= (A XOR B) XOR Bin

2.Bout = A'B'Bin + A'BBin' + A'BBin + ABBin

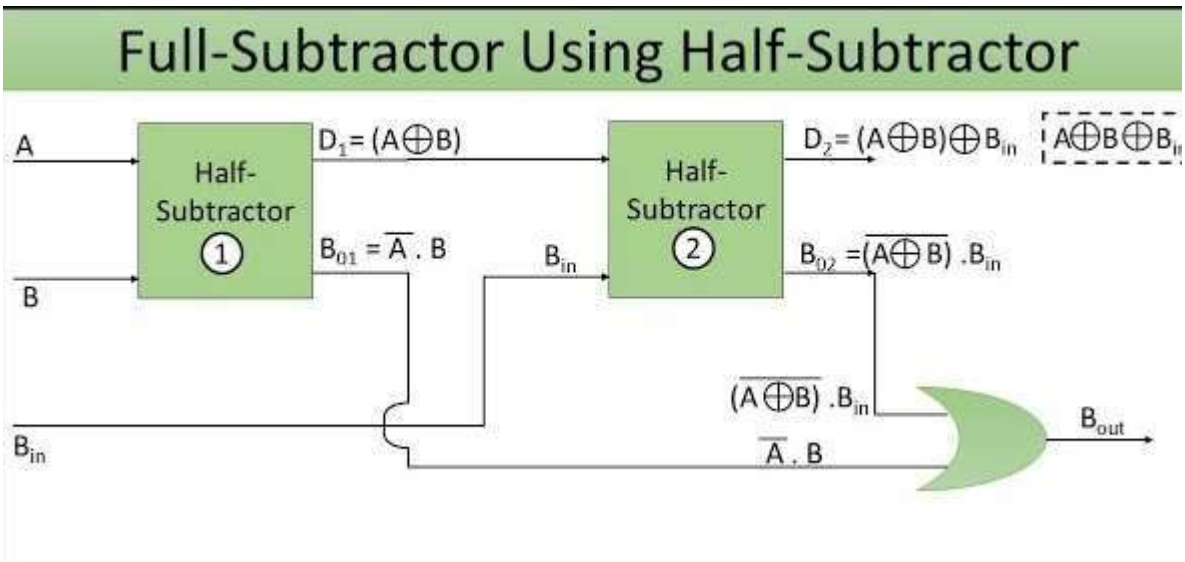
= A'B'Bin +A'BBin' + A'BBin + A'BBin + A'BBin + ABBin

= A'Bin(B + B') + A'B(Bin + Bin') + BBin(A + A')

= A'Bin + A'B + BBin

Circuit diagram :-

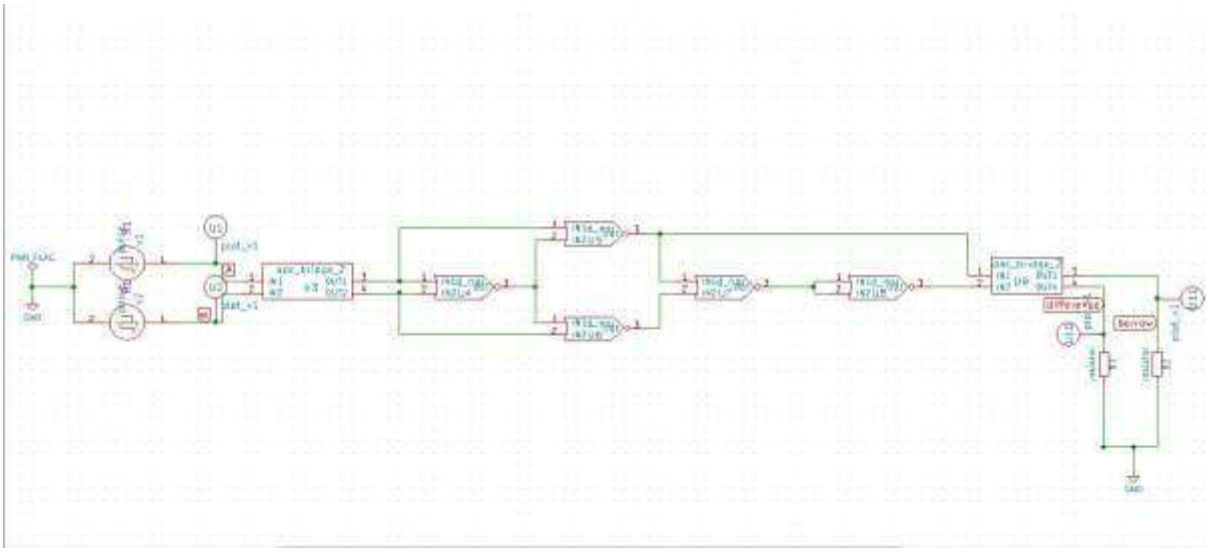
Implementation of full subtractor using two half-subtractor



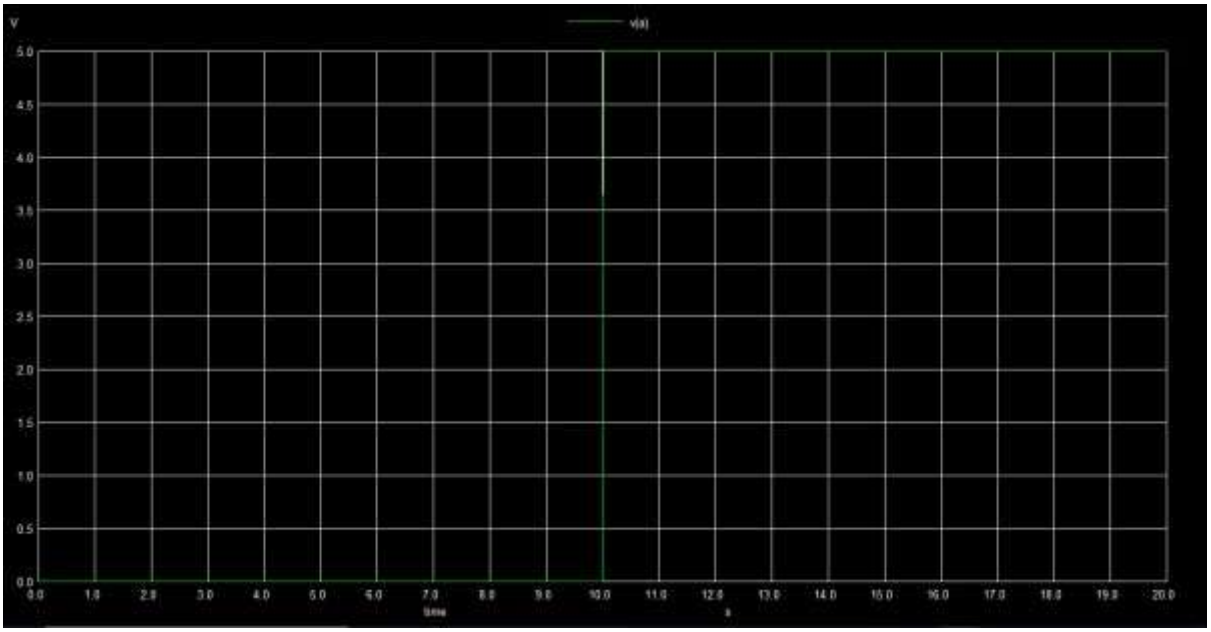
**for e-sim I have chosen the sub-circuit for half-subtractor

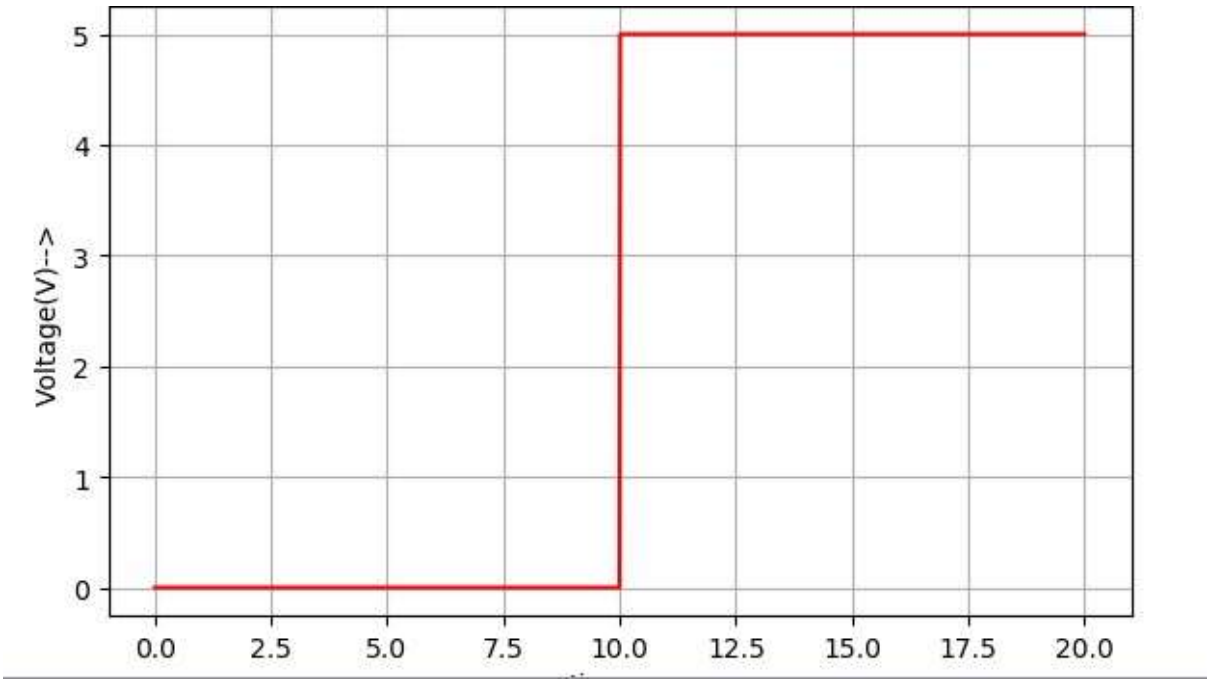
e-sim circuit diagrams with appropriate results:-

1.half-subtractor(using nor gate only) :-

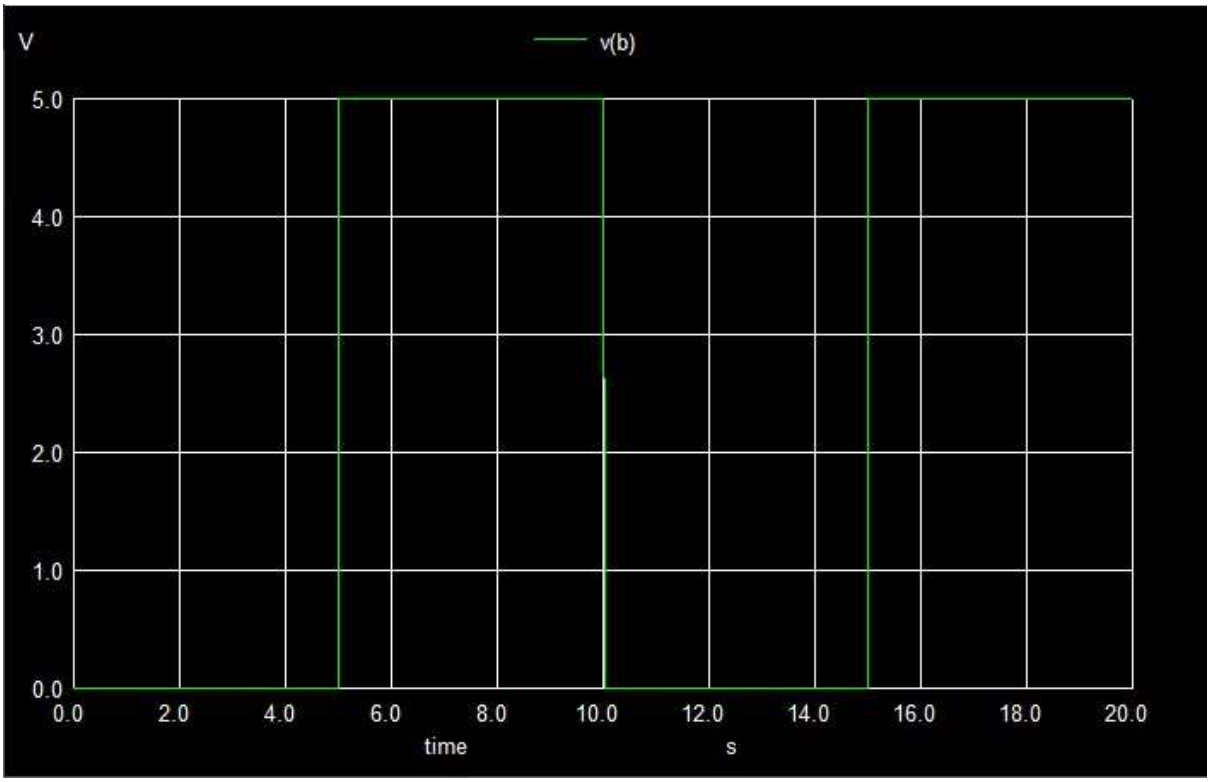


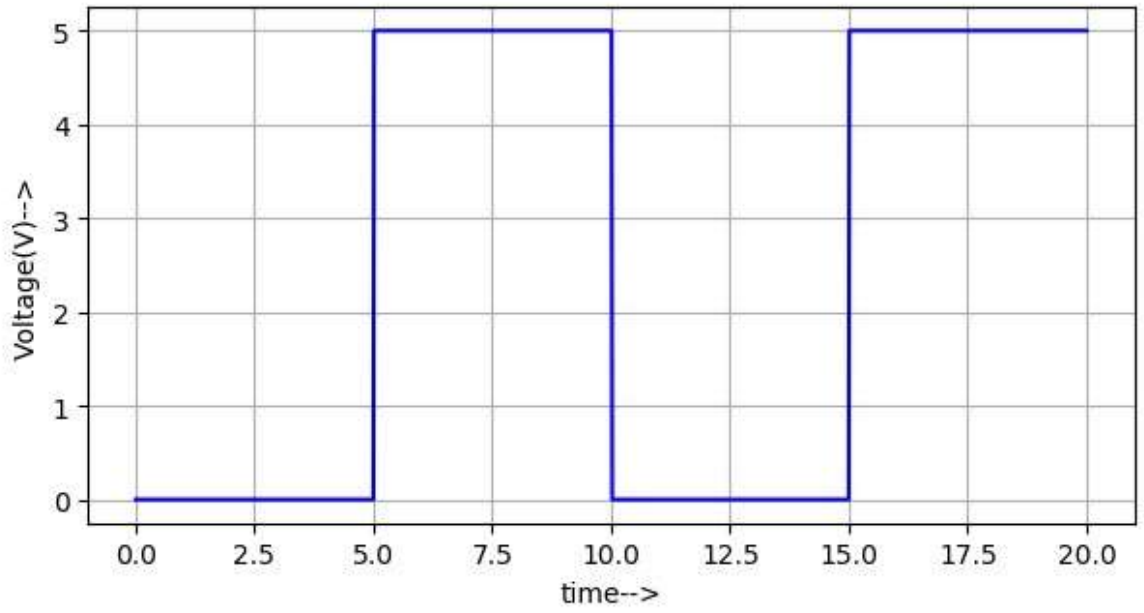
A.



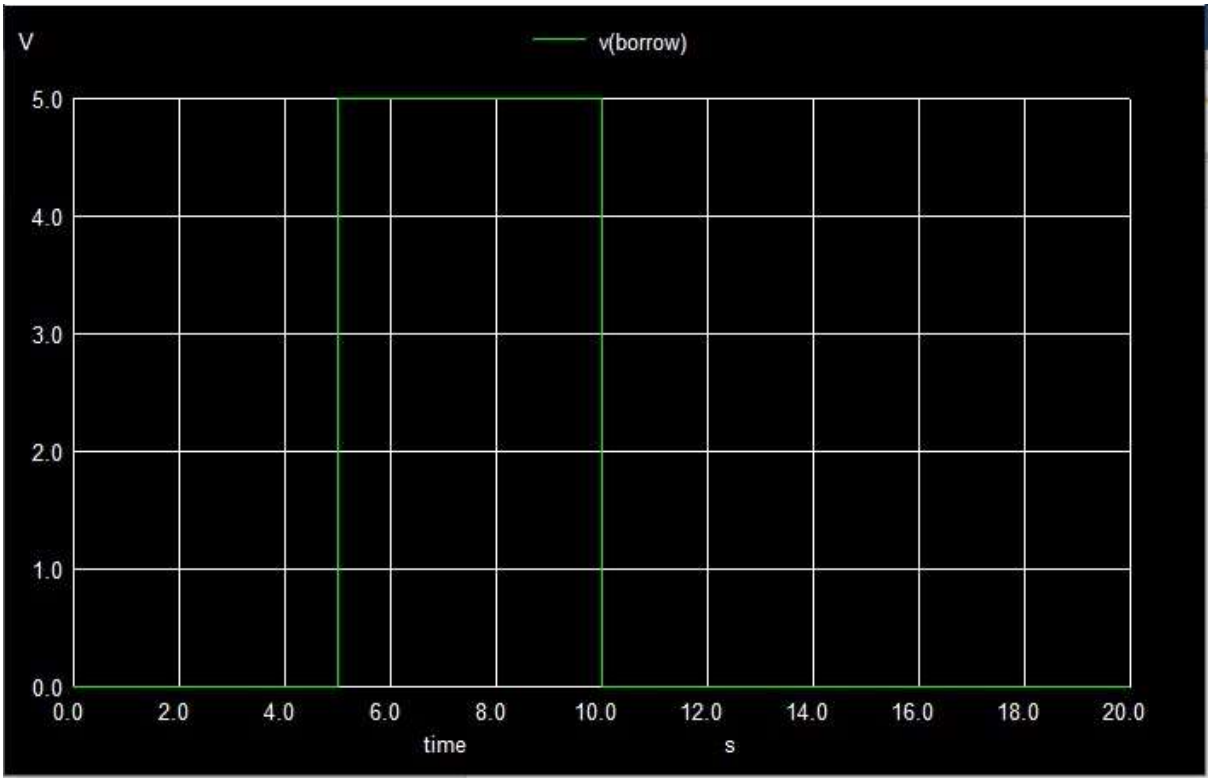

Voltage(V)-->
5
4
3
2
1
0
0.0
2.5
5.0
7.5
10.0
12.5
15.0
17.5
20.0

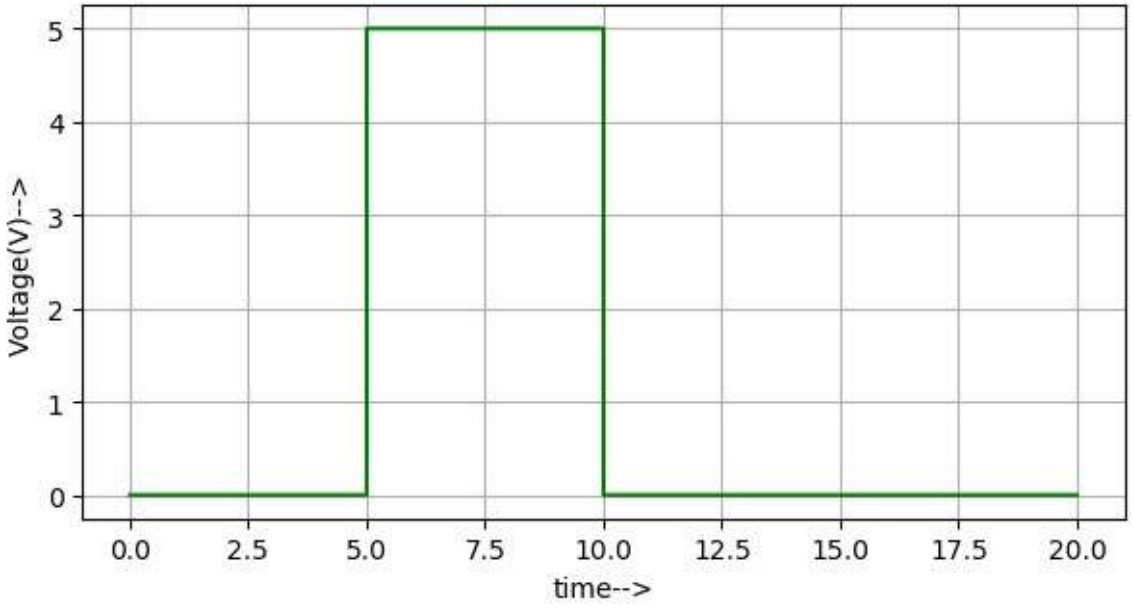
B.


V
v(b)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
2.0
4.0
6.0
8.0
10.0
12.0
14.0
16.0
18.0
20.0
time
s

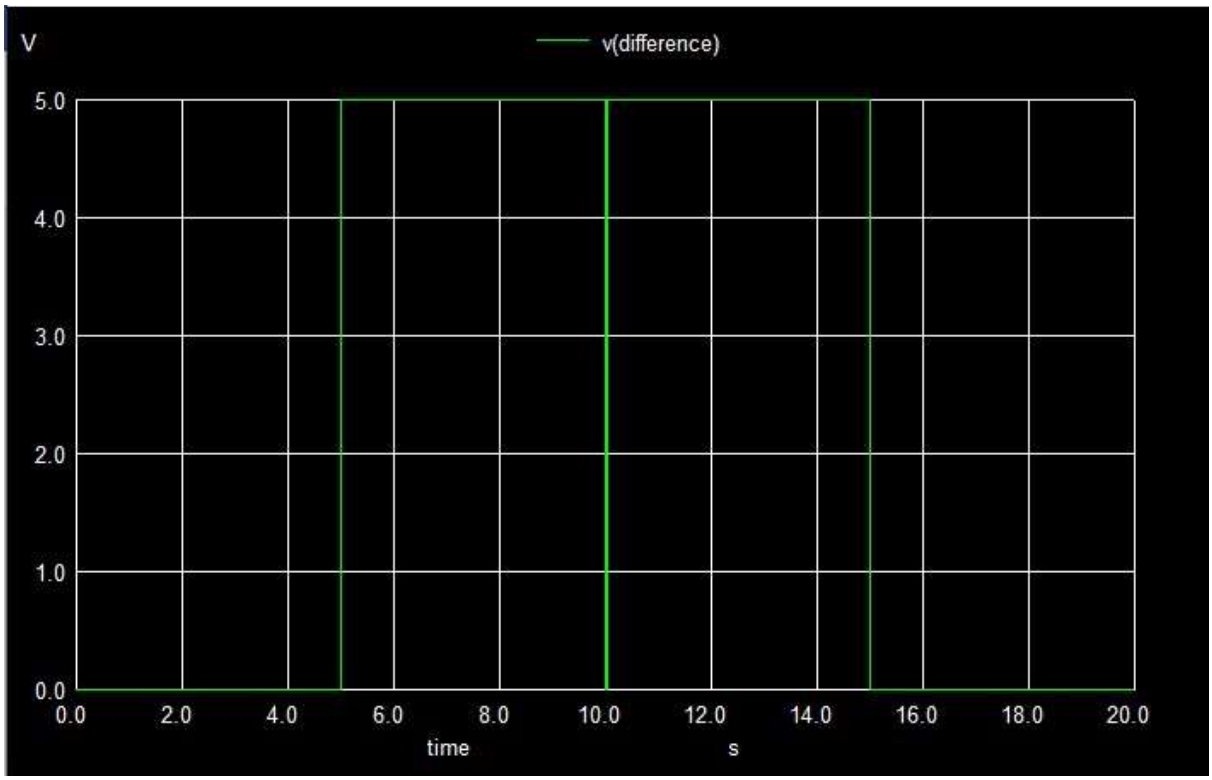

Voltage(V)-->
5
4
3
2
1
0
0.0
2.5
5.0
7.5
10.0
12.5
15.0
17.5
20.0
time-->

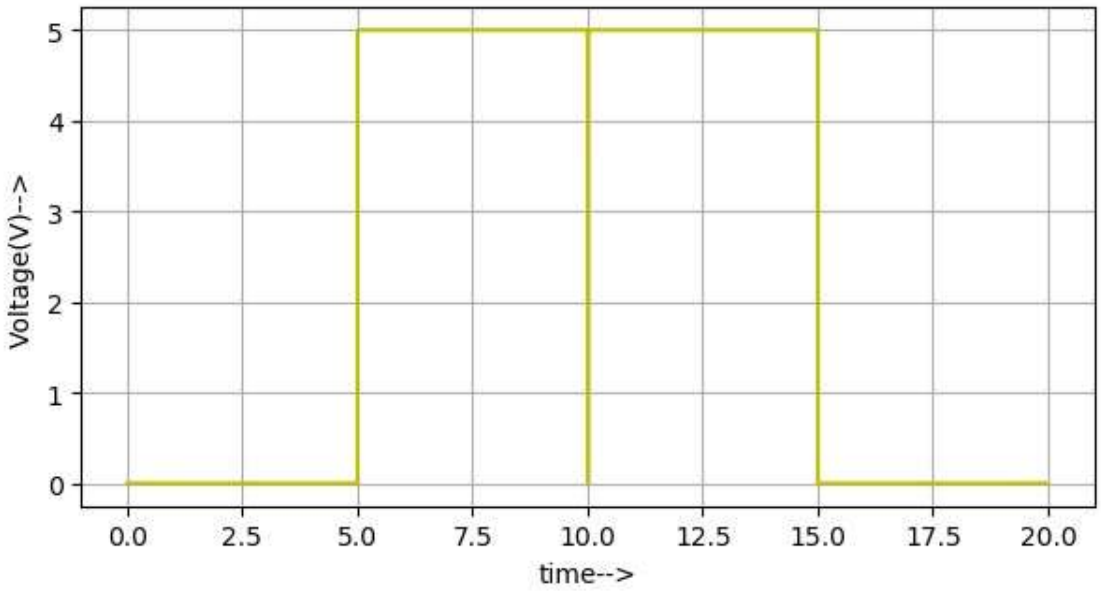
BORROW.


V
v(borrow)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
2.0
4.0
6.0
8.0
10.0
12.0
14.0
16.0
18.0
20.0
time
s

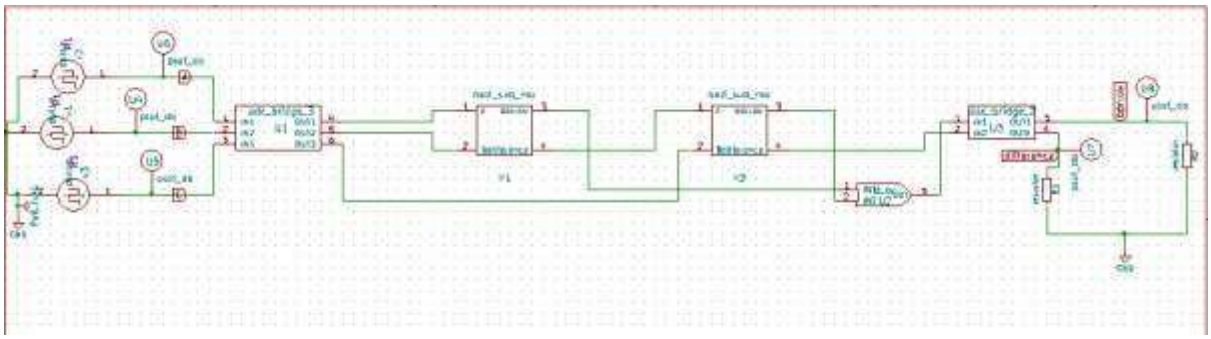

Voltage(V)-->
5
4
3
2
1
0
0.0
2.5
5.0
7.5
10.0
12.5
15.0
17.5
20.0
time-->

DIFFERENCE.

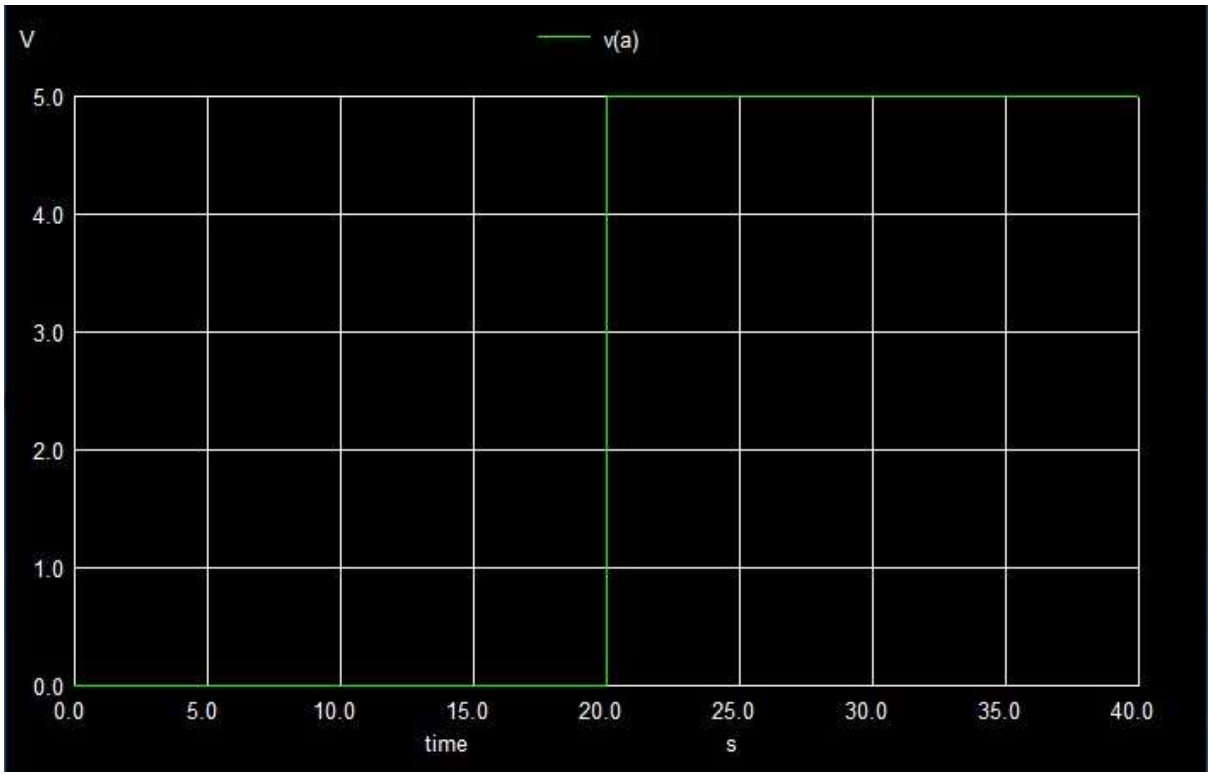

V
v(difference)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
2.0
4.0
6.0
8.0
10.0
12.0
14.0
16.0
18.0
20.0
time
s

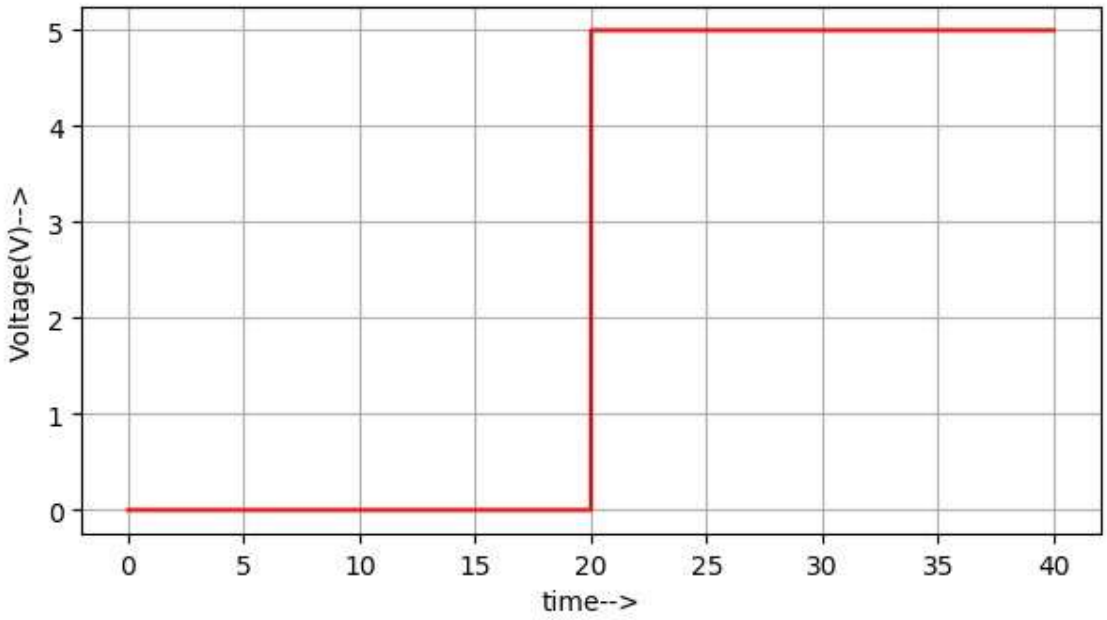

5
4
3
2
1
0
Voltage(V)-->
0.0
2.5
5.0
7.5
10.0
12.5
15.0
17.5
20.0
time-->

2.full subtractor (using 2 half subtractors as a sub-circuit)

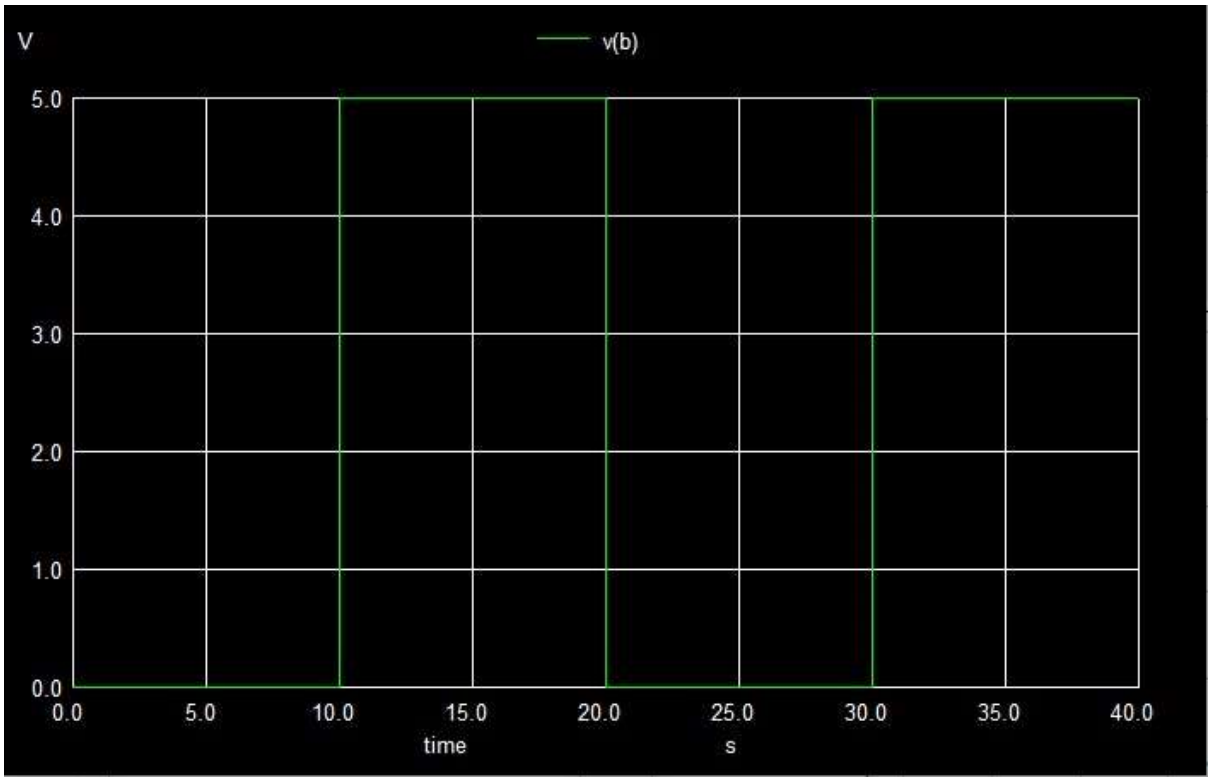


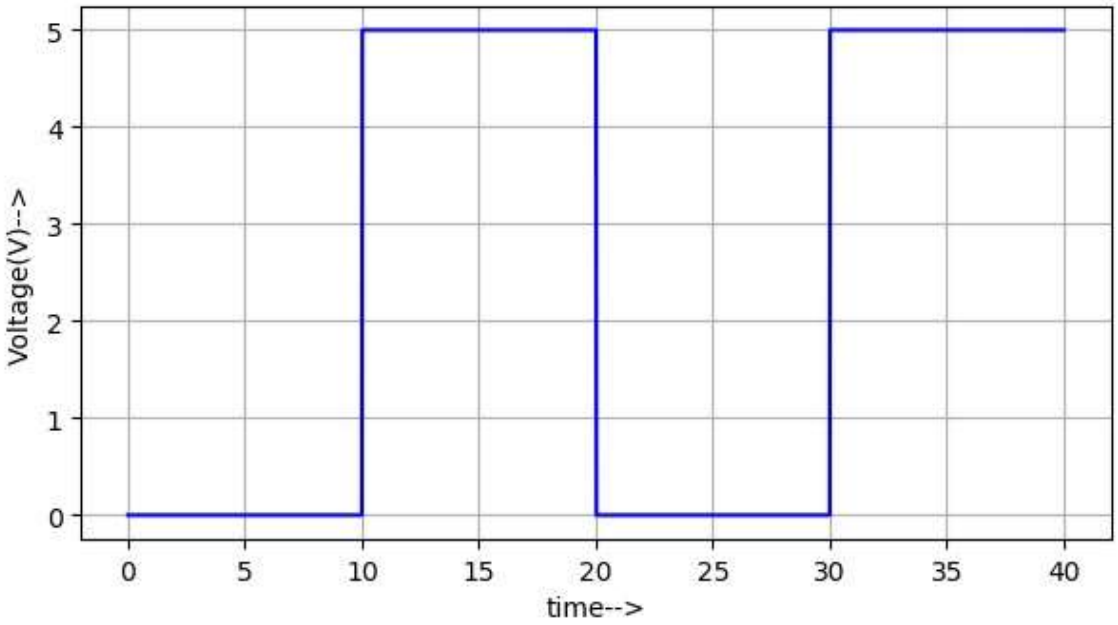
A.



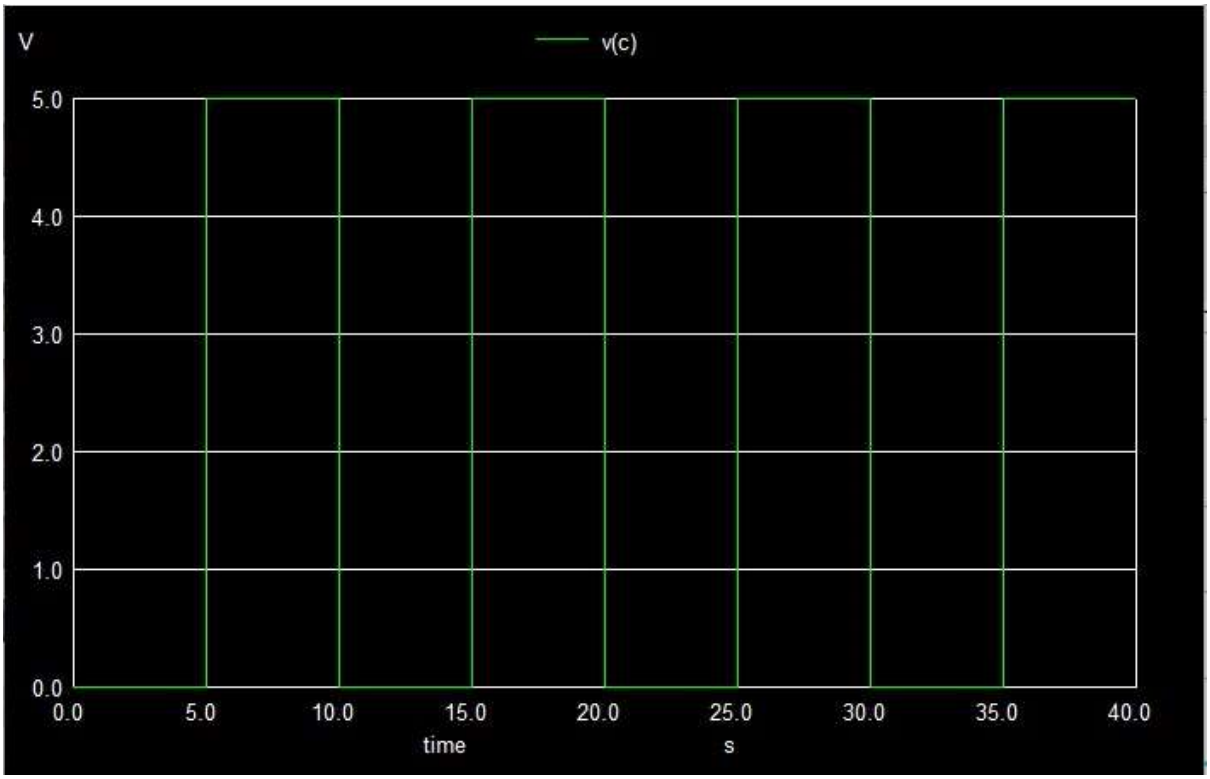

Voltage(V)-->
time-->
0
1
2
3
4
5
0
5
10
15
20
25
30
35
40

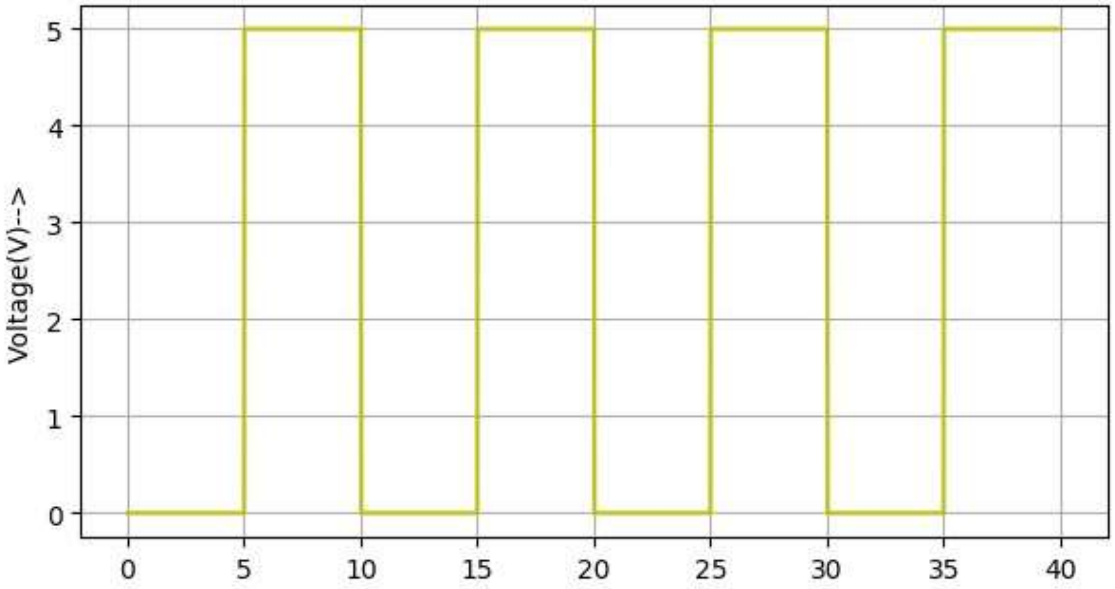
B.


V
v(b)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
5.0
10.0
15.0
20.0
25.0
30.0
35.0
40.0
time
s

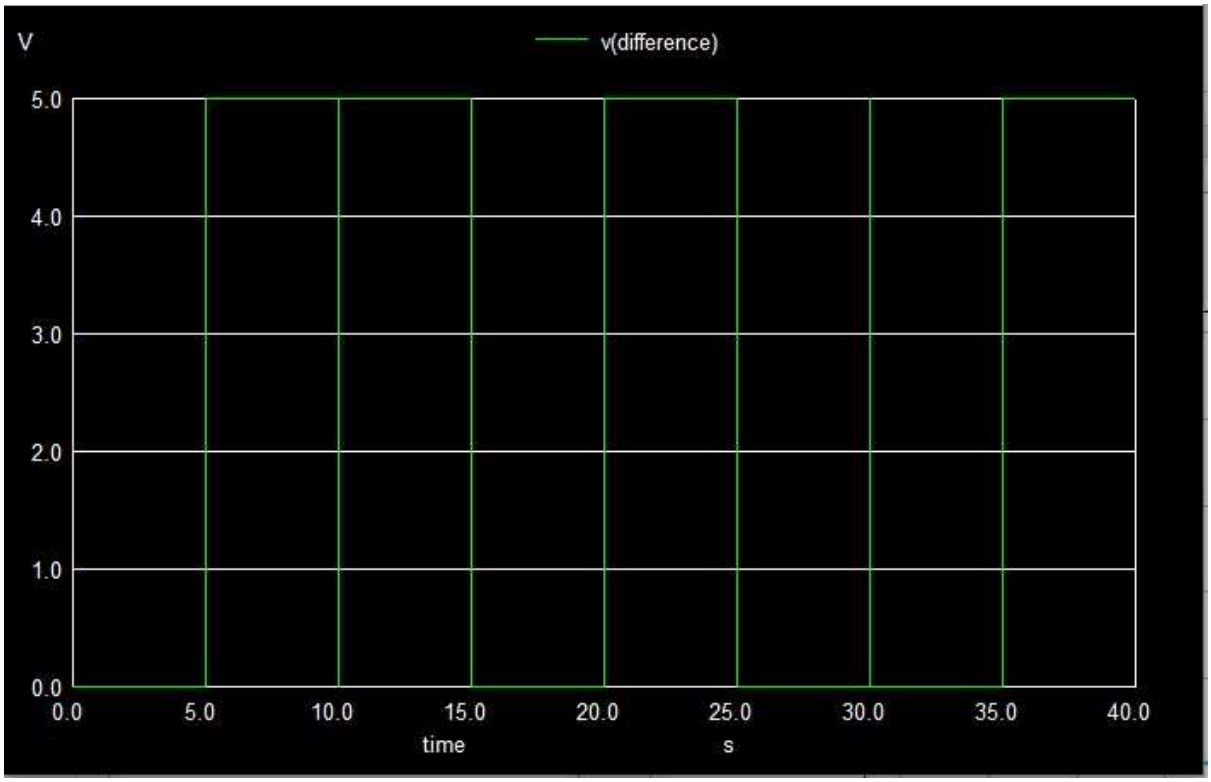

Voltage(V)-->
time-->
0
1
2
3
4
5
0
5
10
15
20
25
30
35
40

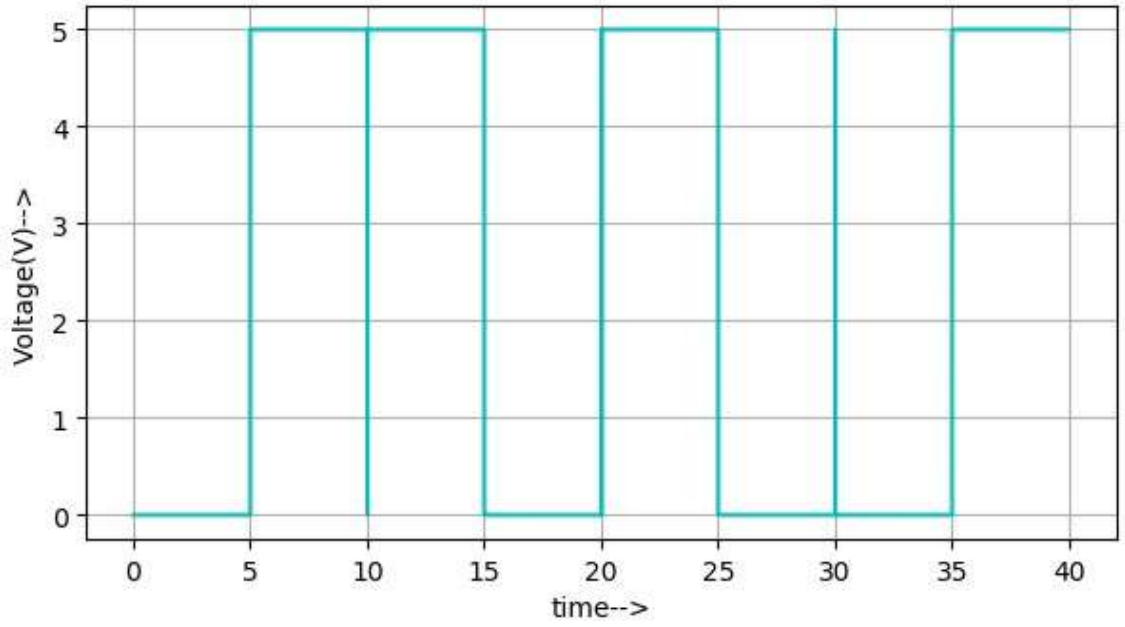
C.


V
v(c)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
5.0
10.0
15.0
20.0
25.0
30.0
35.0
40.0
time
s

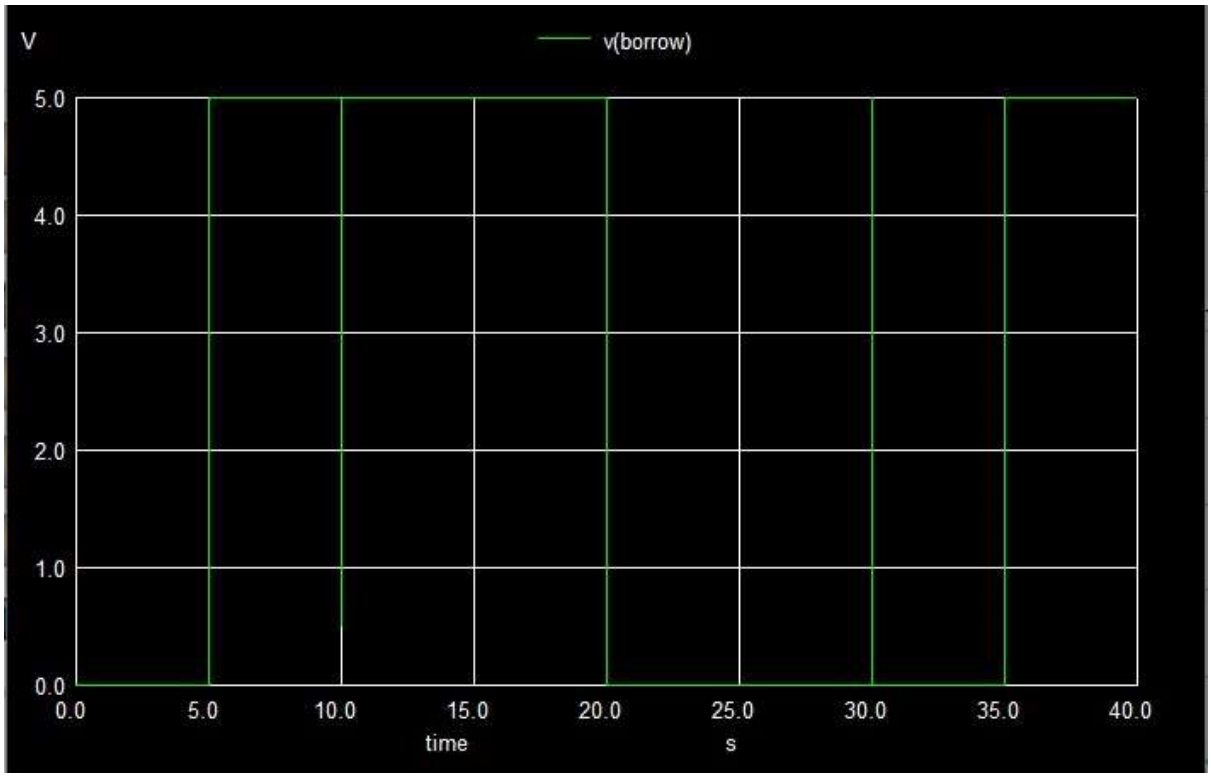

Voltage(V)-->
5
4
3
2
1
0
0
5
10
15
20
25
30
35
40

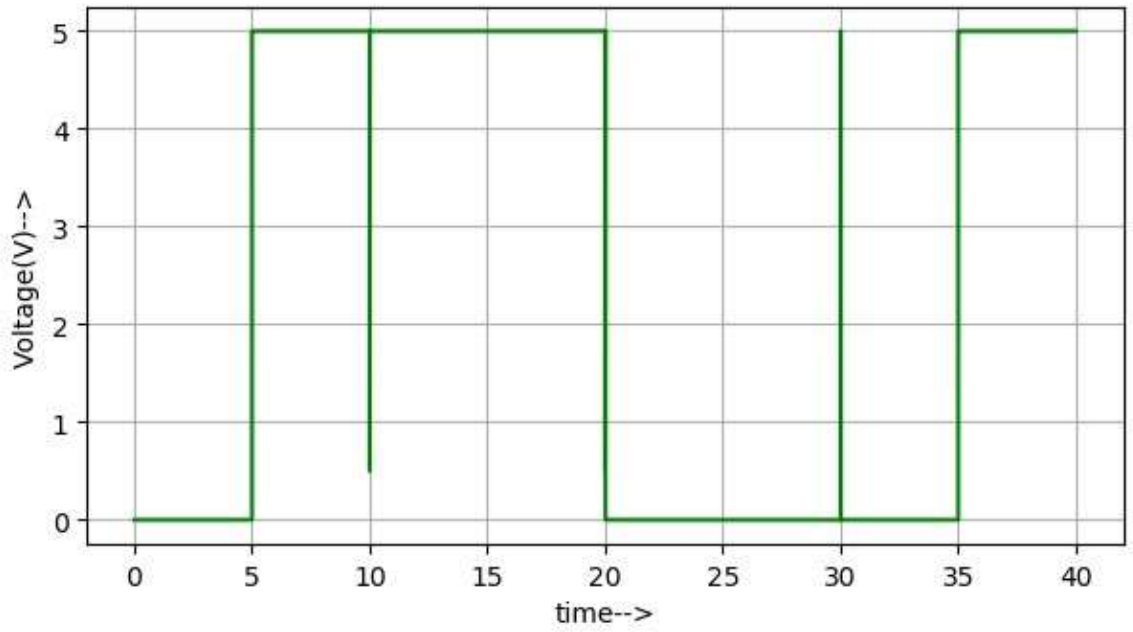
DIFFERENCE


V
v(difference)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
5.0
10.0
15.0
20.0
25.0
30.0
35.0
40.0
time
s


Voltage(V)-->
time-->
0
1
2
3
4
5
0
5
10
15
20
25
30
35
40

BORROW.


V
v(borrow)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
5.0
10.0
15.0
20.0
25.0
30.0
35.0
40.0
time
s



CONCLUSION :-

Thus we can implement full subtractor using 2 half subtractors as a subcircuit using NOR gate only.

REFERENCES :-

1. https://www.geeksforgeeks.org/half-adder-half-subtractor-using-nandnor-gates/
2. https://www.youtube.com/watch?v=PBfdiLf1myM
3. https://www.javatpoint.com/half-subtractor-in-digital-electronics
4. https://www.javatpoint.com/full-subtractor-in-digital-electronics