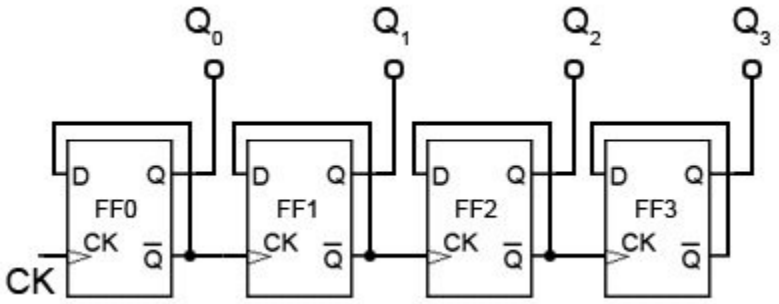
Title of the project: 4-bit Ripple Counter

Theory:

To design a 4-bit asynchronous up counter

1. Take four D flip-flop. If all four flip-flops are negative edge triggered than the resultant counter will be the up counter in case if the Qn of flip-flop are applied to the clk input of next flip-flop. But If the Qnbar is applied than the resultant counter will be the down counter.
2. Apply clk to the first flip-flop.
3. Apply VCC common to all the flip flop.
4. Draw the clk diagram.



Basic circuit connections for the 4-bit Ripple Counter

Let us assume that the 4 Q outputs of the flip flops are initially 0000. When the rising edge of the clock pulse is applied to the FF0, then the output Q0 will change to logic 1 and the next clock pulse will change the Q0 output to logic 0. This means the output state of the clock pulse toggles (changes from 0 to1) for one cycle.

As the Q' of FF0 is connected to the clock input of FF1, then the clock input of second flip flop will become 1. This makes the output of FF1 to be high (i.e., Q1 = 1), which indicates the value 20. In this way the next clock pulse will make the Q0 to become high again.

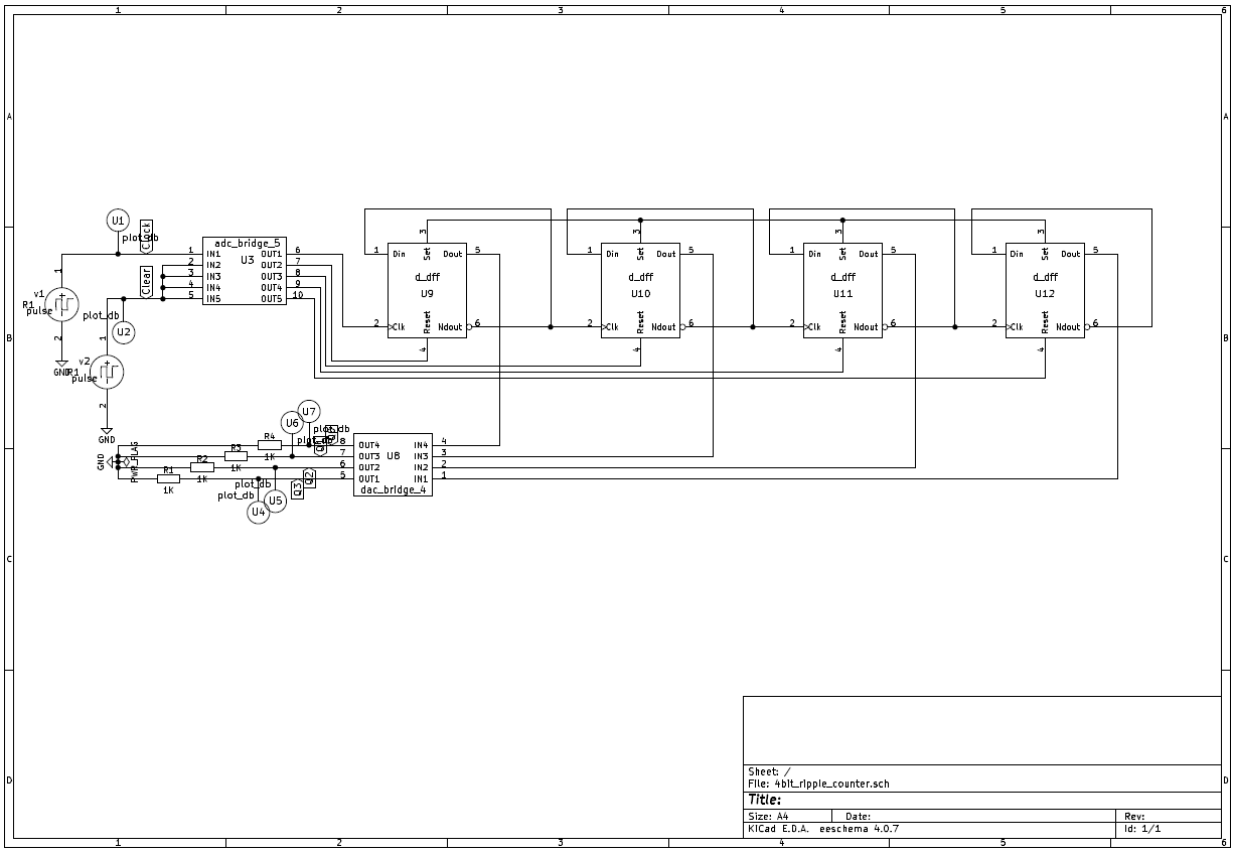
So now both Q0 and Q1 are high, this results in making the 4-bit output 11002. Now if we apply the fourth clock pulse, it will make the Q0 and Q1 to low state and toggles the FF2. So, the output Q2 will become 0010¬2.

CK	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Truth table for the 4-bit ripple counter using D flip-flops

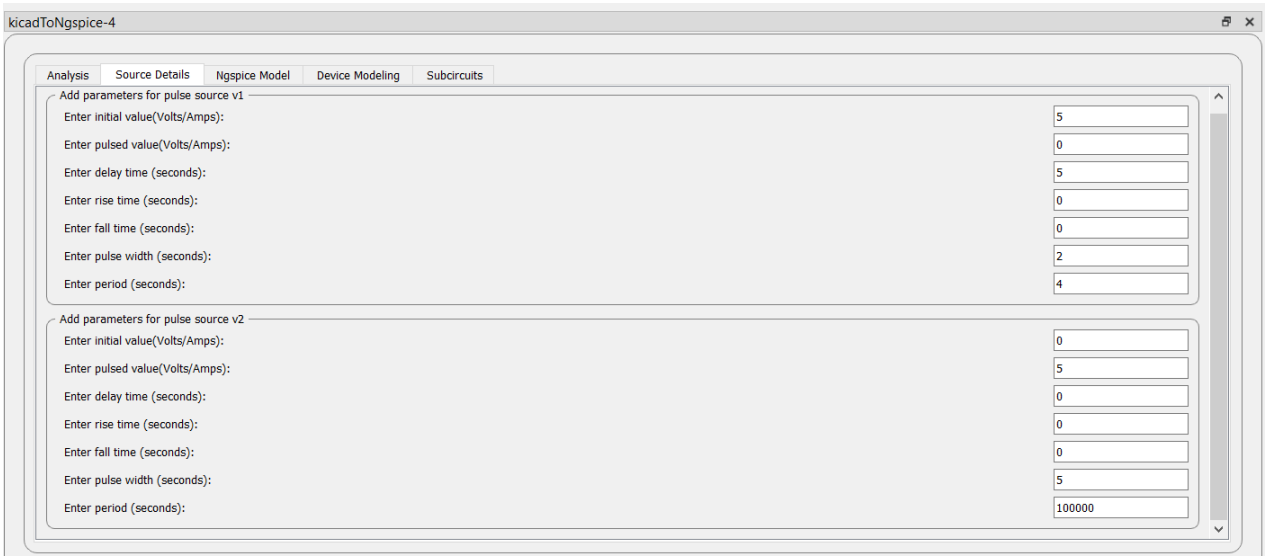
Schematic Diagram:

The circuit schematic of the 4-bit ripple counter in eSim is shown below:

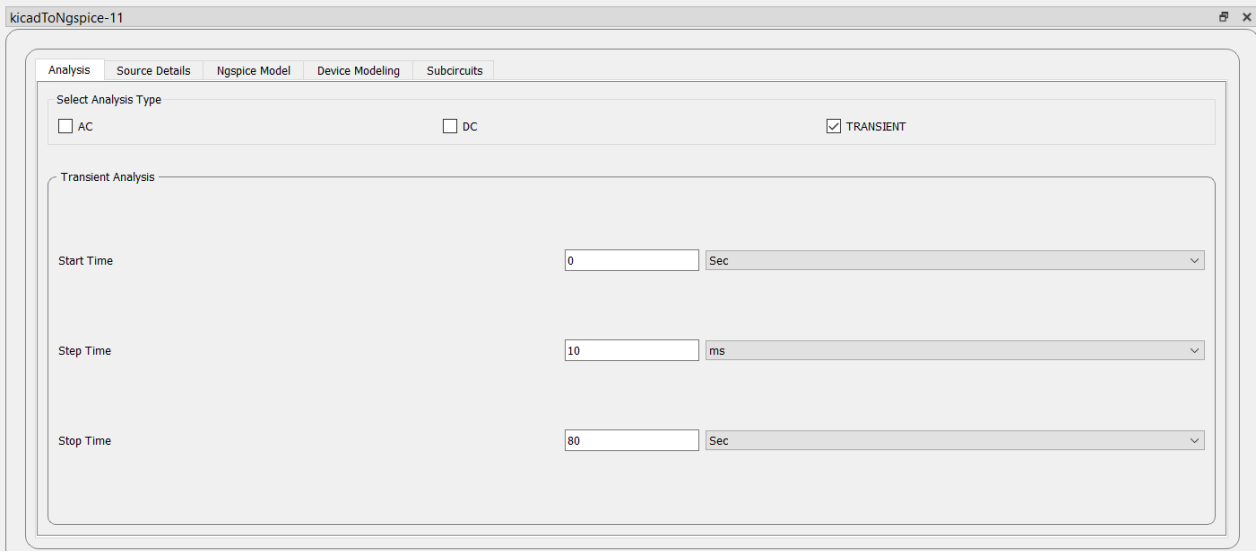


Circuit diagram for 4-bit ripple counter using D flip flops in eSim

Source and analysis details for reference:



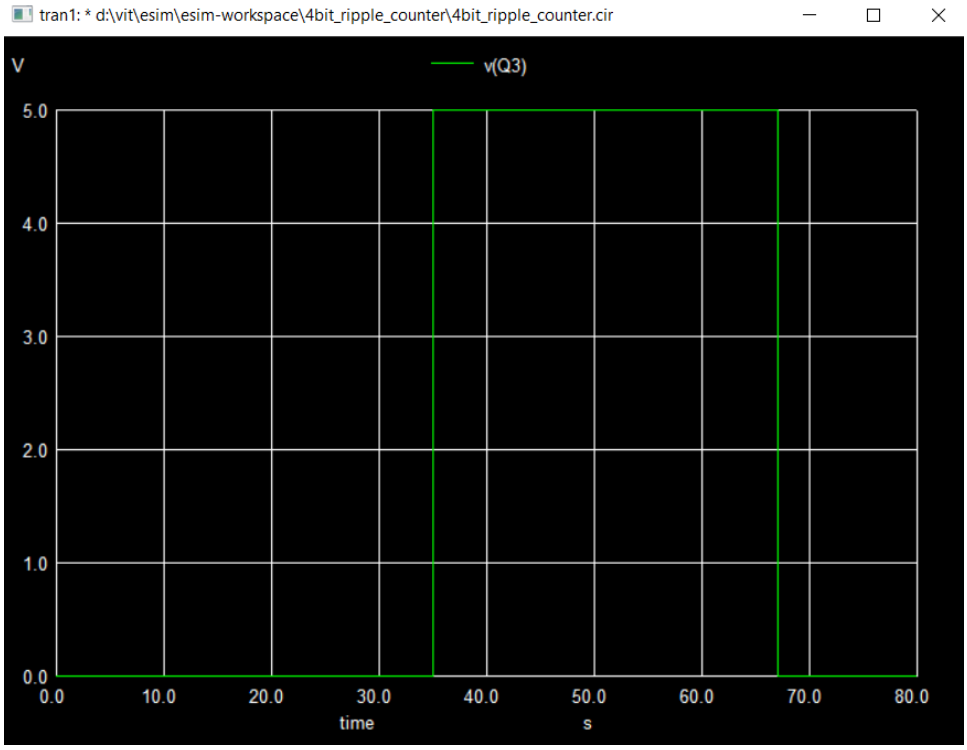
Source details used for the simulation



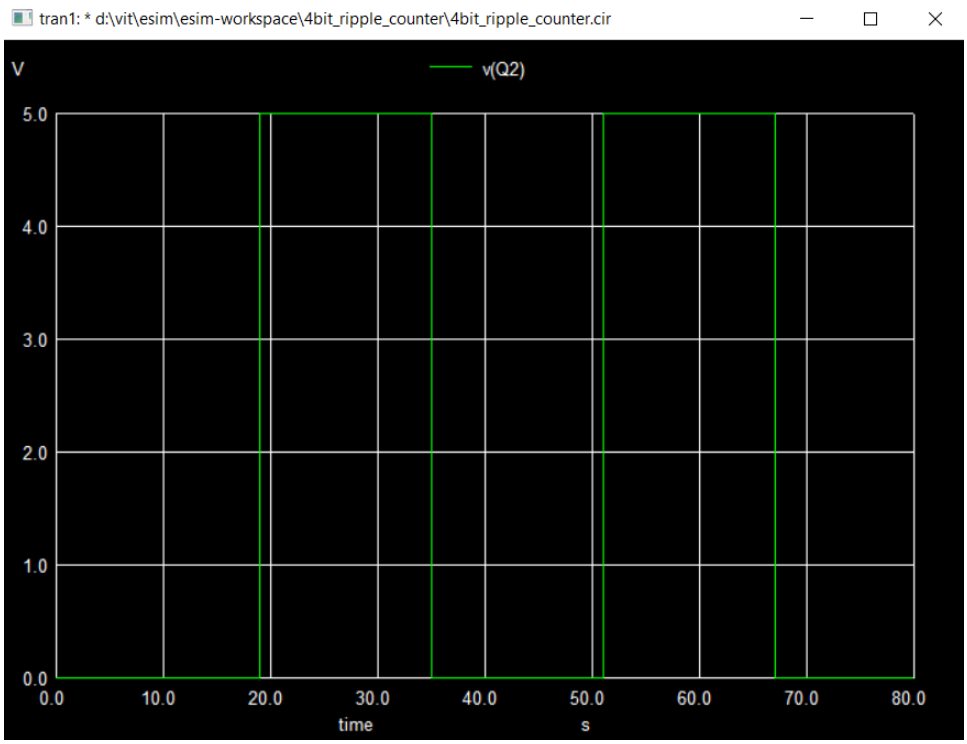
Analysis details used for this simulation

Simulation Results:

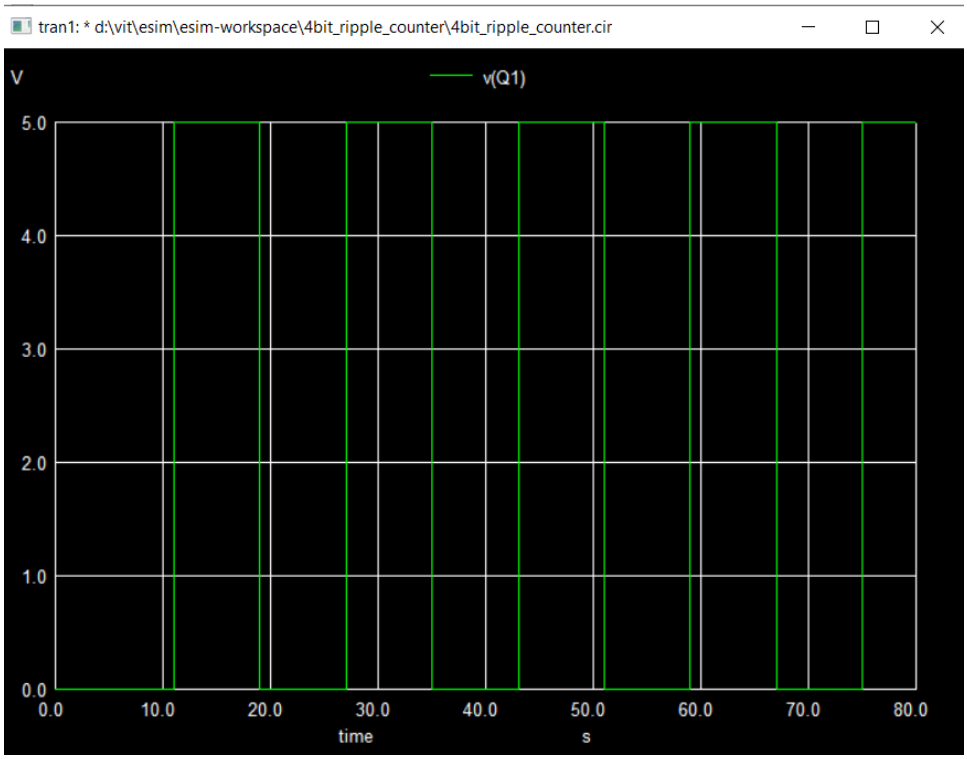
1) Ngspice Plots:



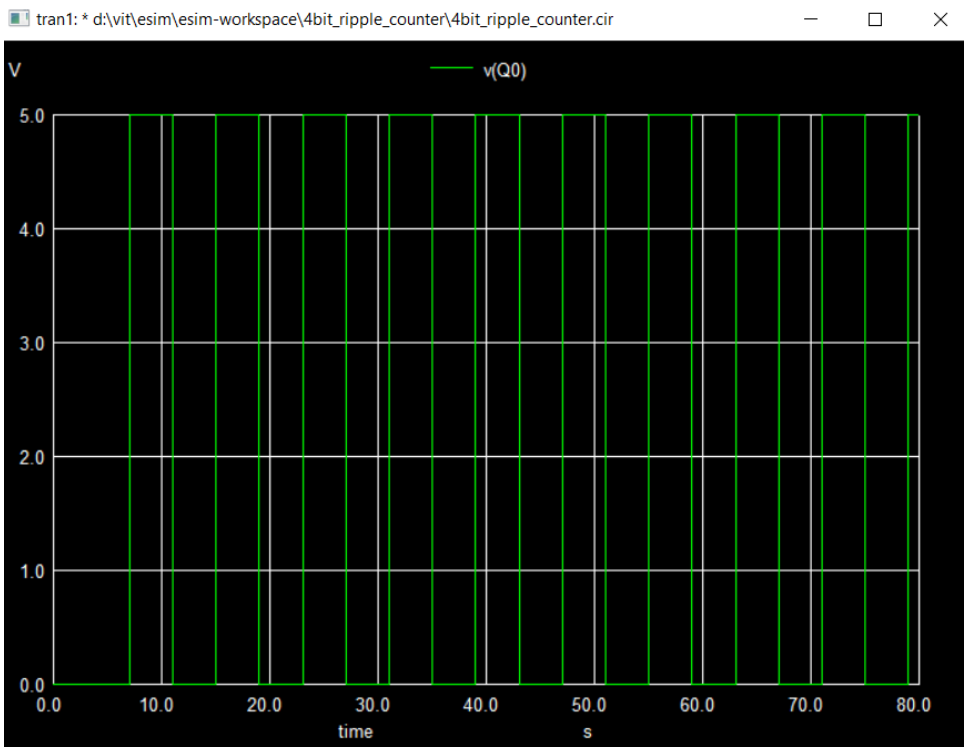
Ngspice plot for the output Q3



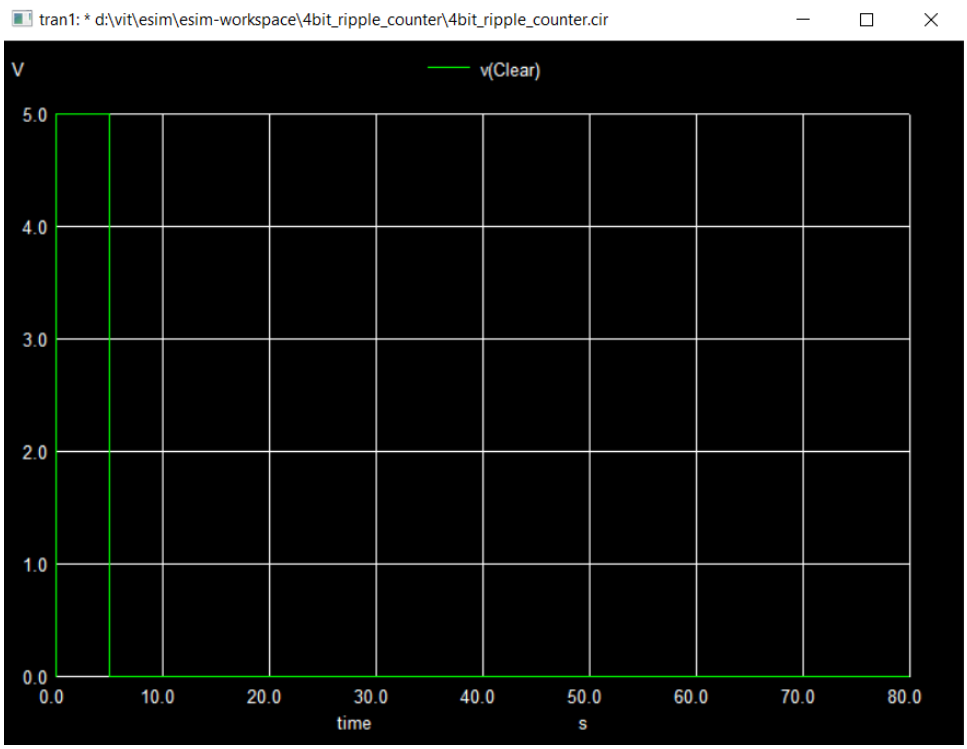
Ngspice plot for the output Q2



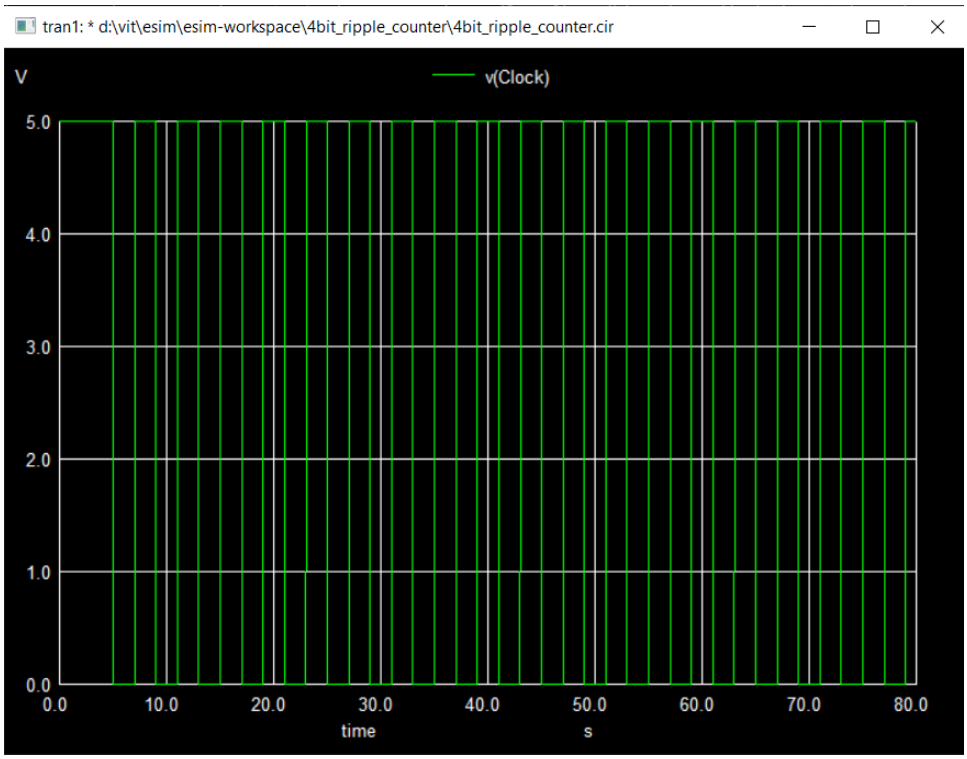
Ngspice plot for the output Q1



Ngspice plot for the output Q0

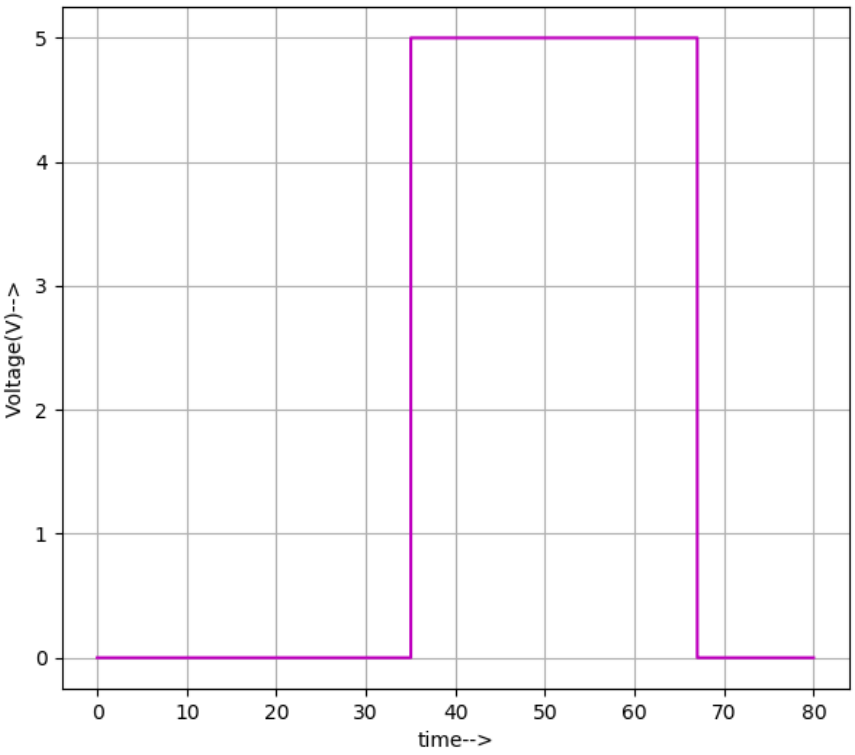


Ngspice plot for the clear pulse

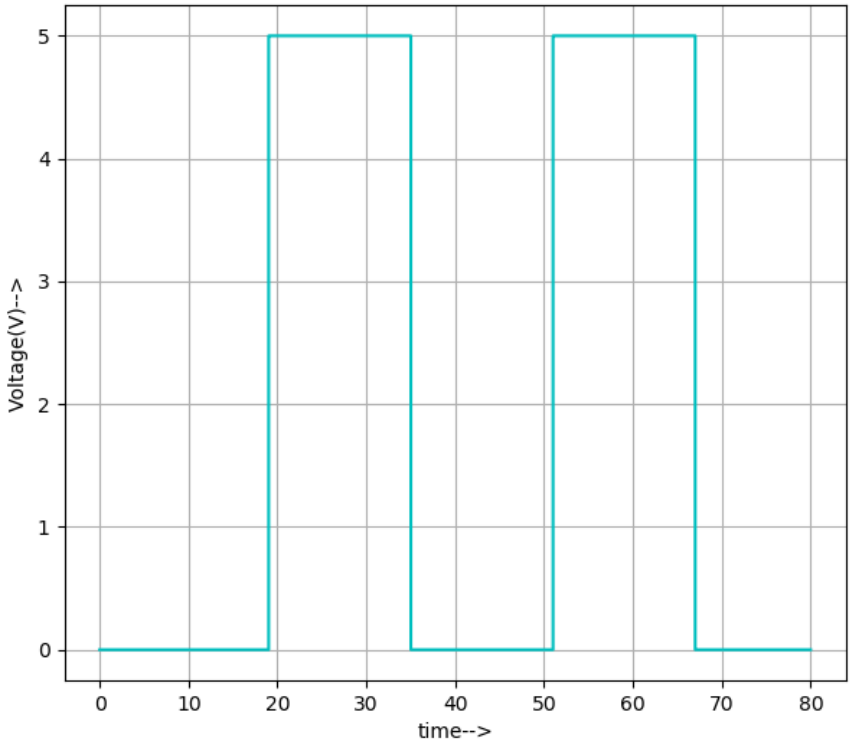


Ngspice plot for the clock pulse

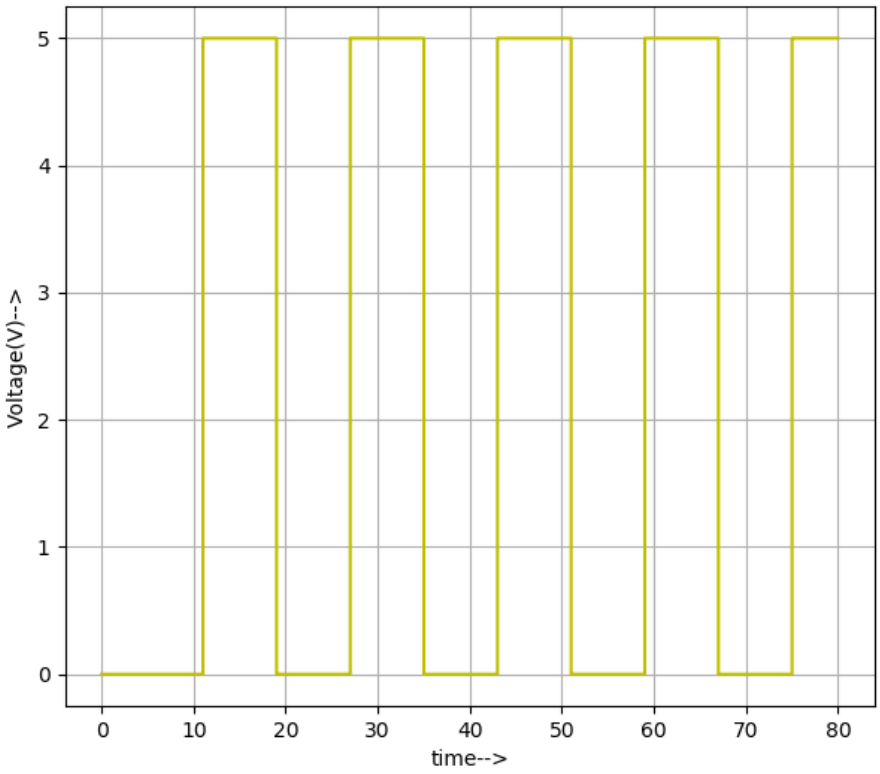
2) Python Plots:



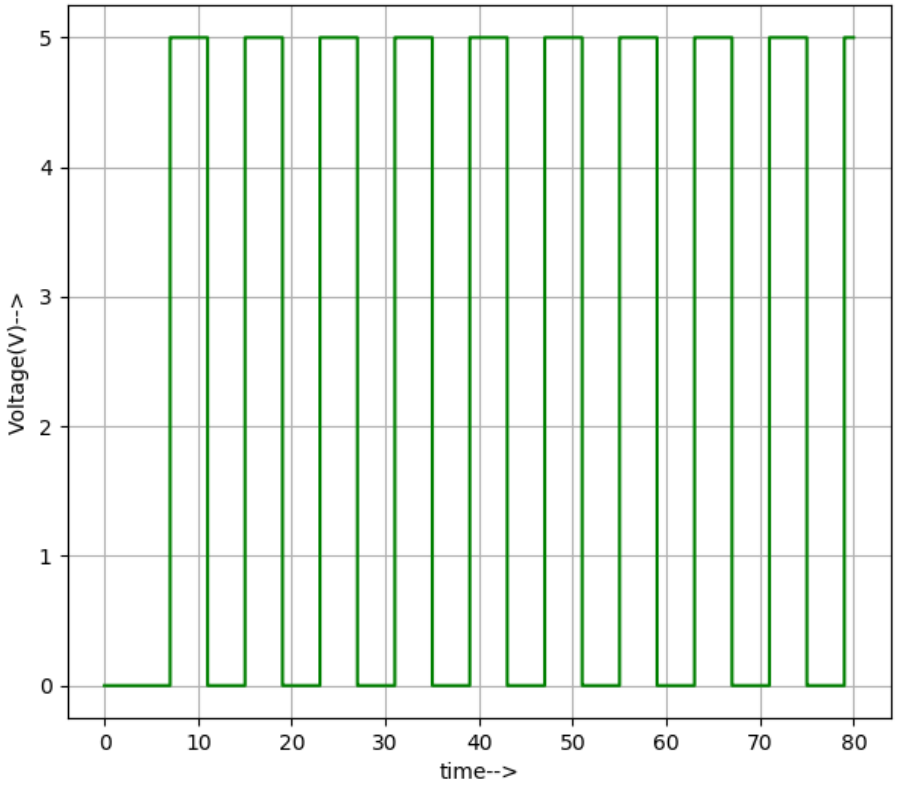
Python plot for the output Q3



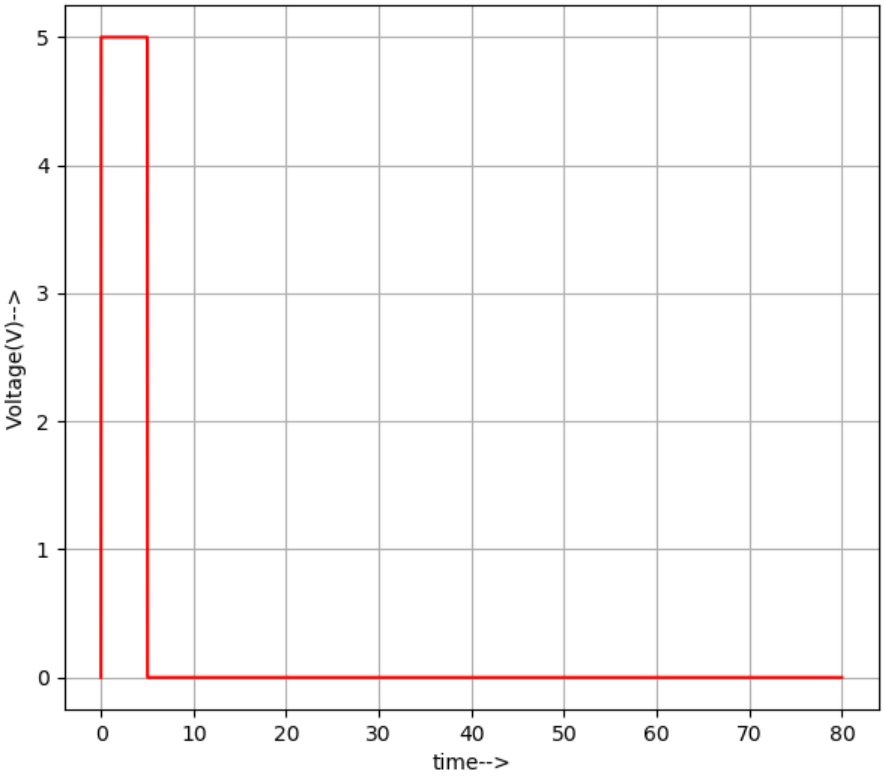
Python plot for the output Q2



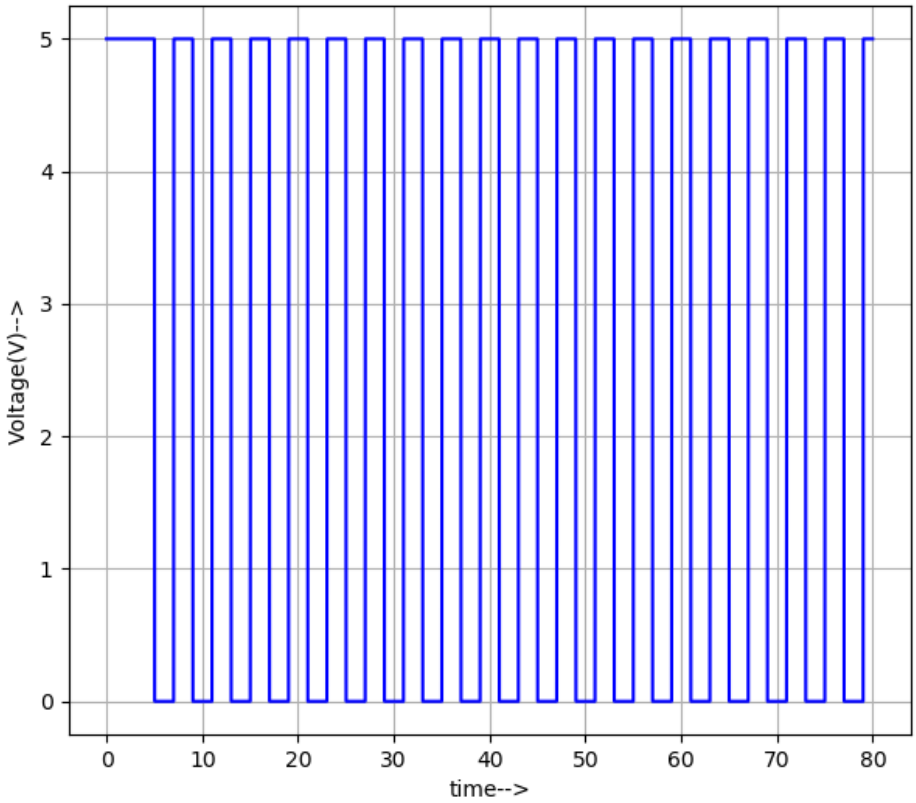
Python plot for the output Q1



Python plot for the output Q0



Python plot for the clear pulse



Python plot for the clock pulse

Conclusion:

Thus, the connection for the 4-bit Ripple Counter was made in eSim and its truth table was verified from the simulations.

References:

https://www.quora.com/How-do-I-draw-a-4-bit-binary-ripple-counter-using-a-D-flip-flop