Circuit Simulation Project

https://esim.fossee.in/circuit-simulation-project

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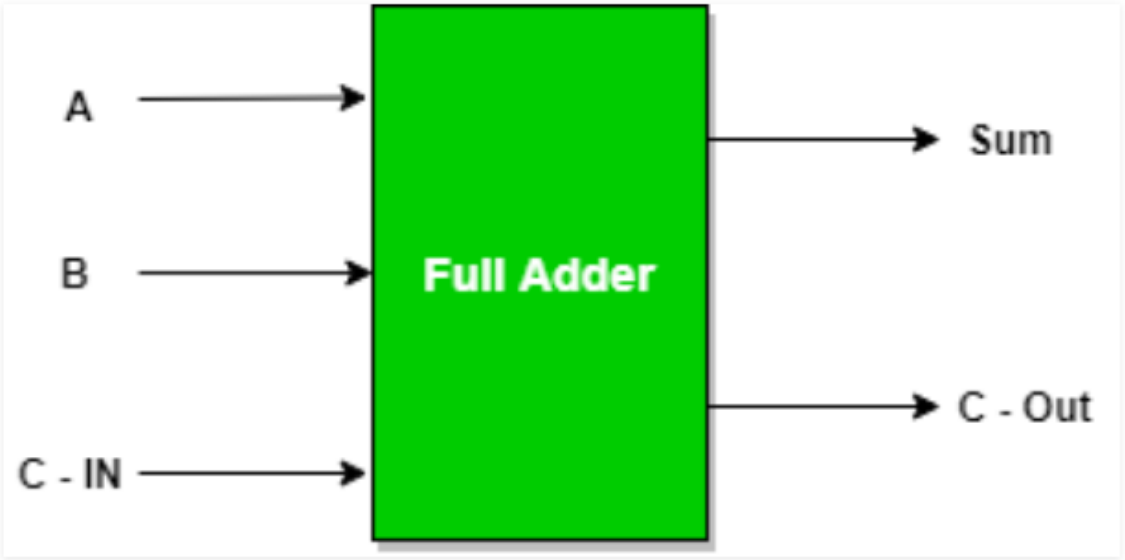
Project Name: Design a Full Adder using a 3 X 8 decoder

THEORY:

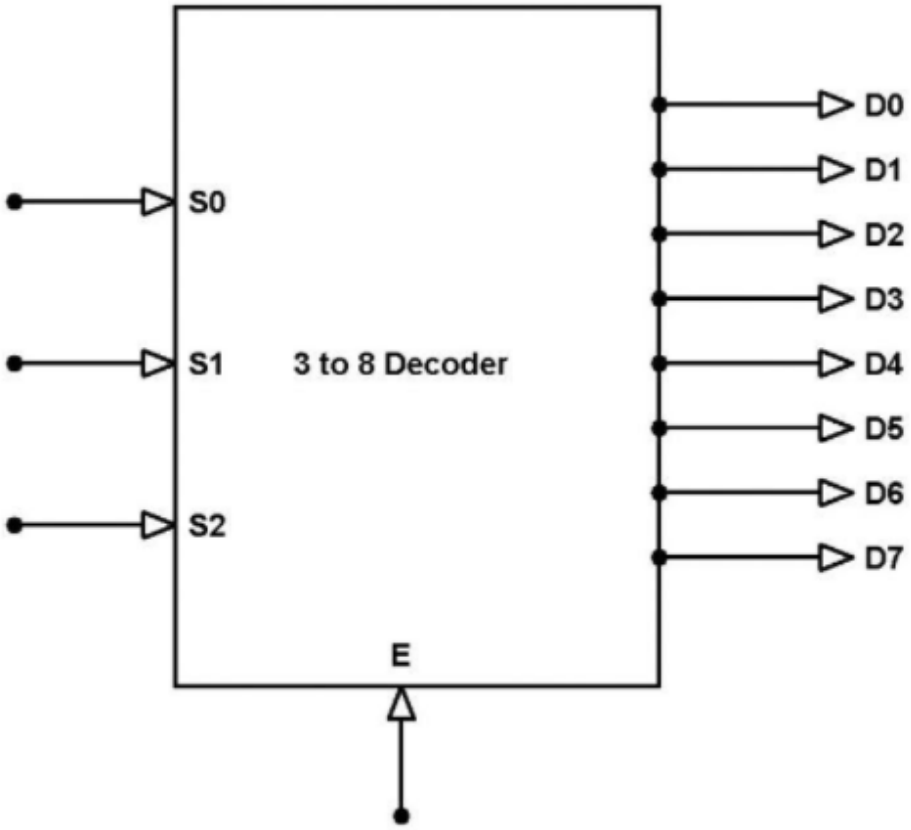
A full adder is a digital circuit that performs addition. Full adders are implemented with logical gates in hardware. A full adder adds three one-bit numbers, two operands and a carry bit. The adder outputs two numbers, a sum and a carry bit. The term is contrasted with a half adder, which adds two binary digits.



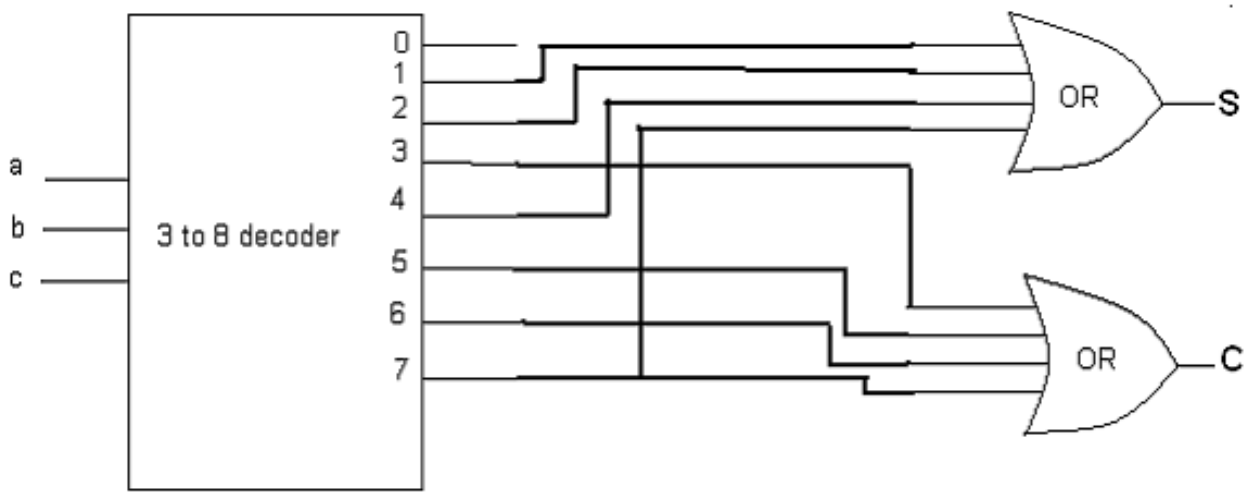
Full Adder Truth Table:

Inputs			Outputs	
A	B	C – IN	Sum	C - Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

3 Line to 8 Line Decoder - This decoder circuit gives 8 logic outputs for 3 inputs and has a enable pin. The circuit is designed with AND and NAND logic gates. It takes 3 binary inputs and activates one of the eight outputs. 3 to 8 line decoder circuit is also called as binary to an octal decoder.



A full adder can be implemented with a 3X8 decoder :



Equating Full Adder from 3 X 8 decoder:

Equation for sum S = ab'c' + a'b'c + a'bc' + abc = Σ(1,2,4,7)

Equation for carry out C = ab + ac + bc

= ab(c + c') + ac (b + b') + bc (a + a')

= abc + abc' + abc + ab'c + abc + a'bc

= abc +a'bc +ab'c+abc'= Σ (3, 5, 6, 7)

From the truth table also we can verify our calculations we can see that:

Sum = ∑m (1,2,4,7)

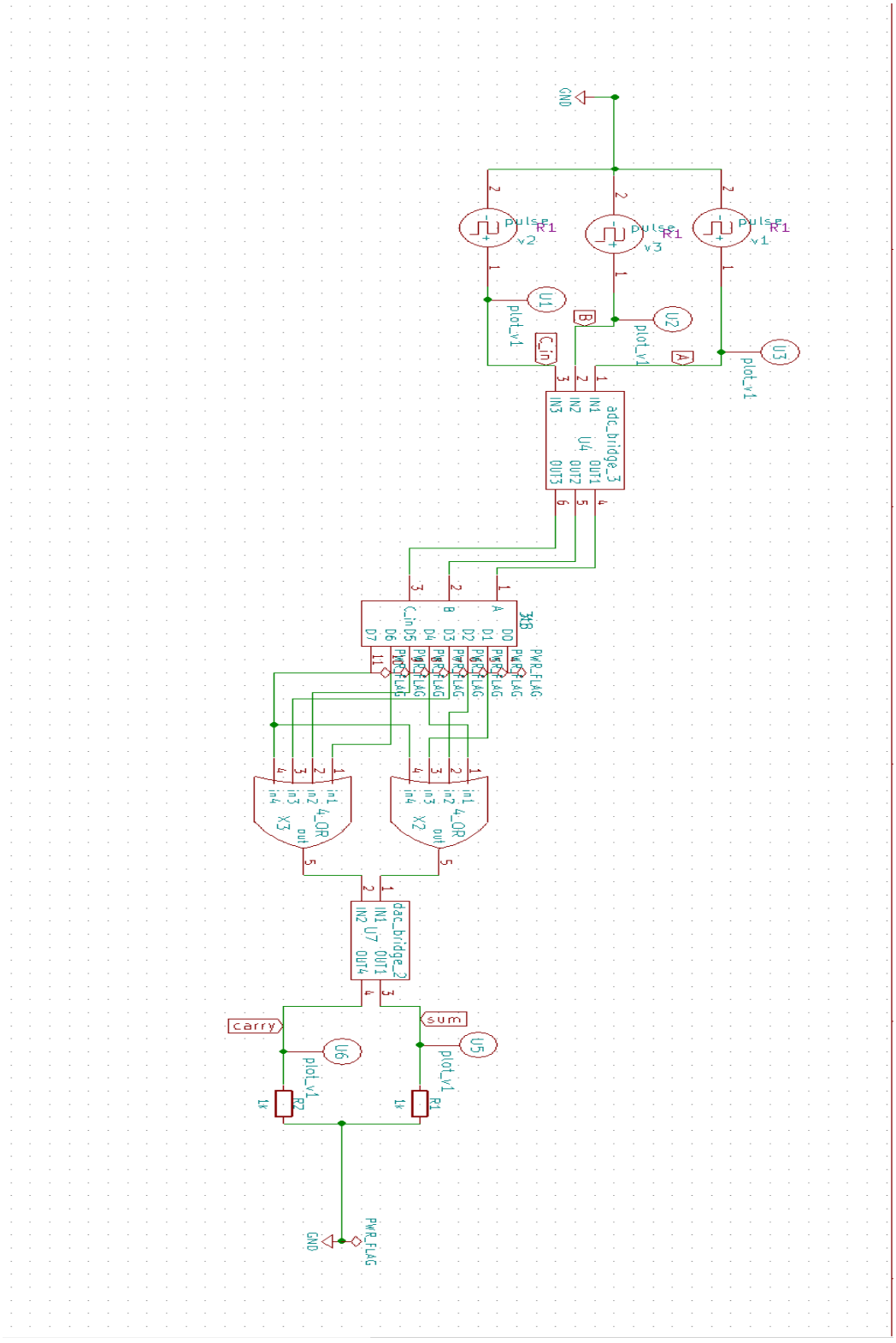
Carry = ∑m (3,5,6,7)

Equation for the input and output of Full Adders:

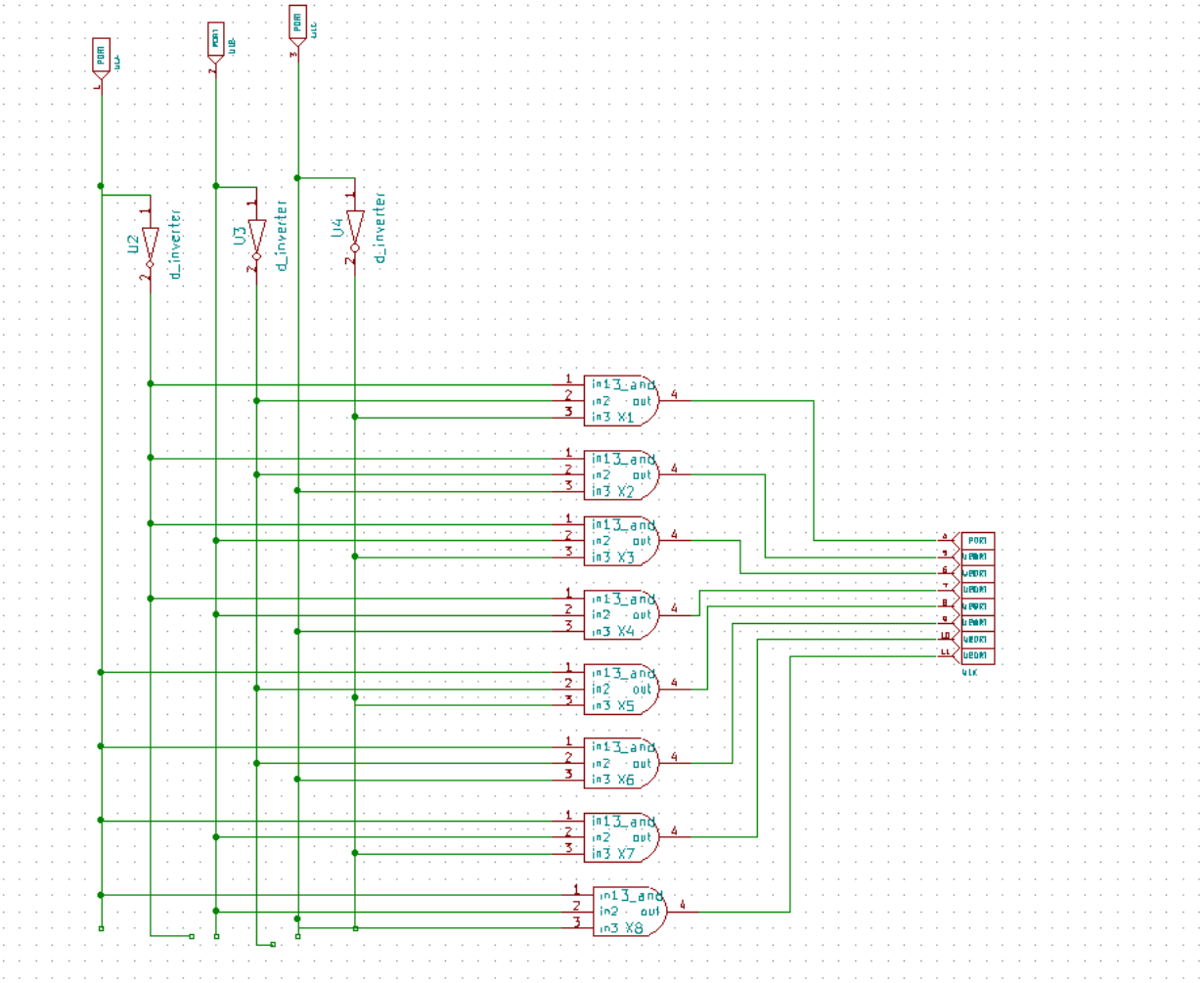
Logical Expression for C-OUT:
= A' B C-IN + A B' C-IN + A B C-IN' + A B C-IN
= A B + B C-IN + A C-IN
= (3,5,6,7)
Another form in which C-OUT can be implemented:
= A B + A C-IN + B C-IN (A + A')
= A B C-IN + A B + A C-IN + A' B C-IN
= A B (1 +C-IN) + A C-IN + A' B C-IN
= A B + A C-IN + A' B C-IN
= A B + A C-IN (B + B') + A' B C-IN
= A B C-IN + A B + A B' C-IN + A' B C-IN
= A B (C-IN + 1) + A B' C-IN + A' B C-IN
= A B + A B' C-IN + A' B C-IN
= AB + C-IN (A' B + A B')
Therefore COUT = AB + C-IN (A EX – OR B)

CIRCUIT DIAGRAM:

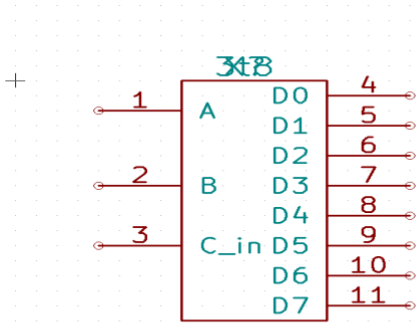
This` is the main functional circuit schematic for the full adder which uses a 3X8 decoder:



The structure of 3 X 8 decoder:



Symbol used for a 3 X 8 Decoder:

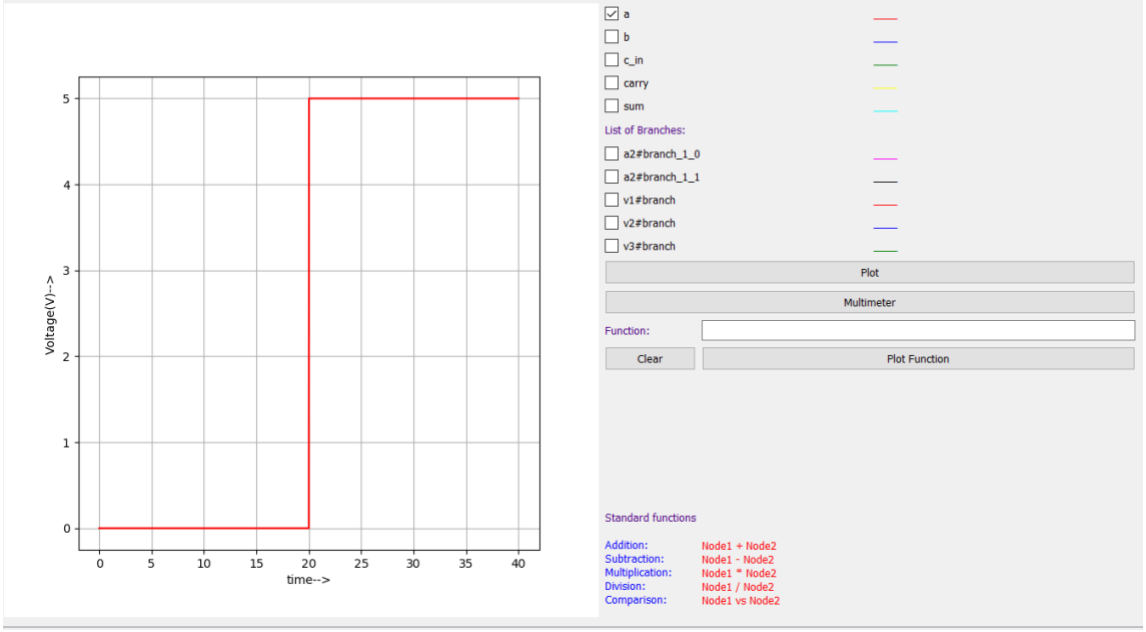


OUTPUTS:

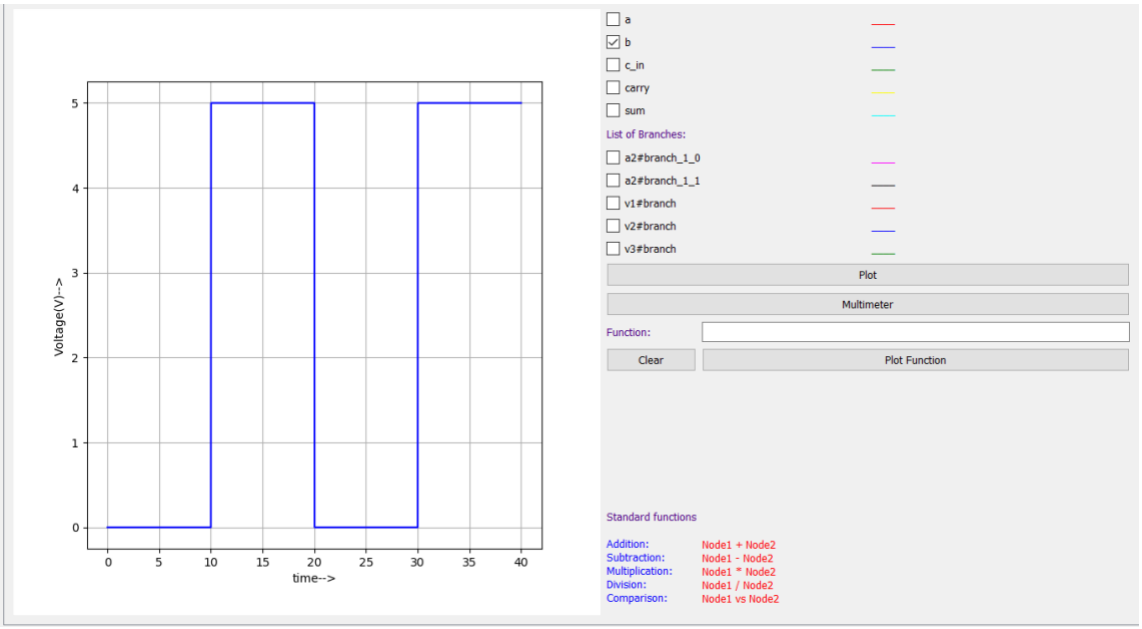
Python Plots:

Inputs:

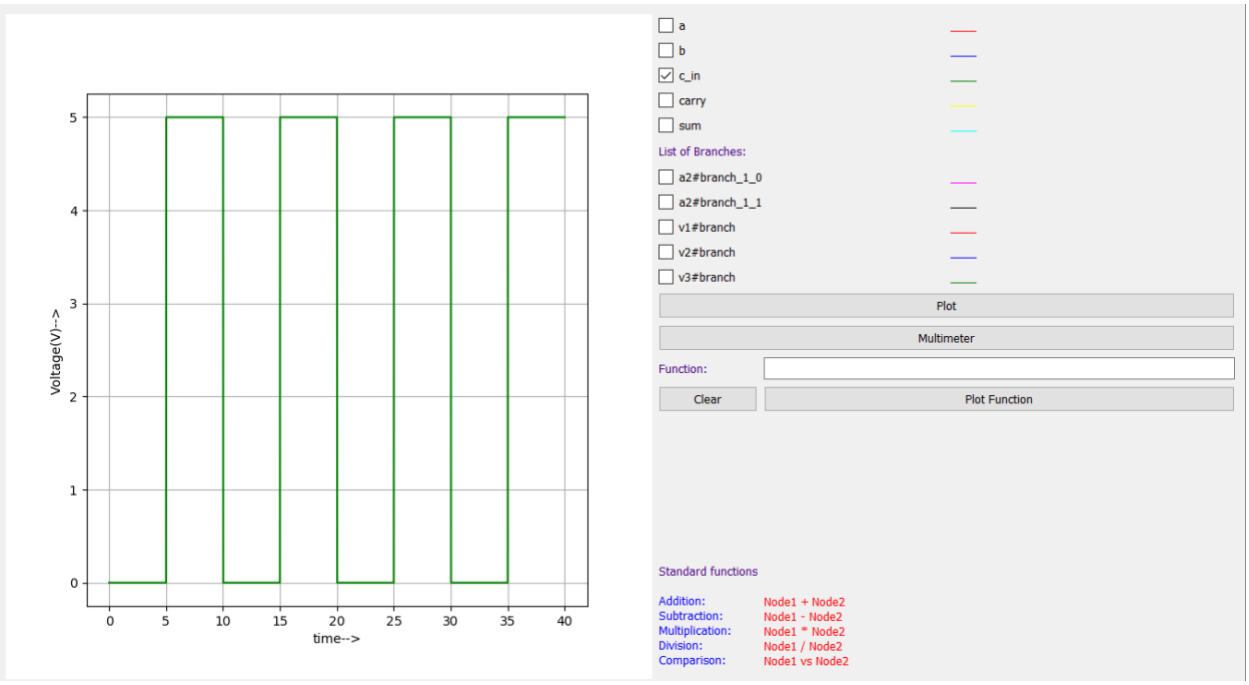
A



B

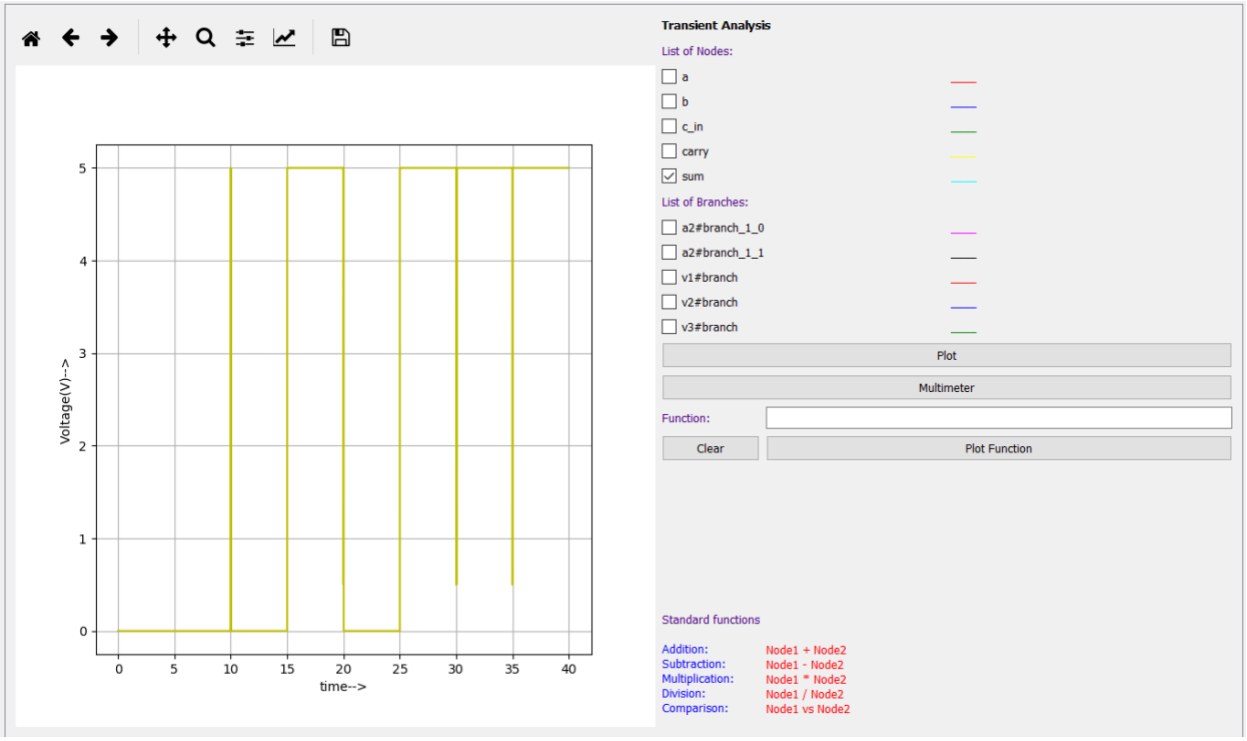


C_in

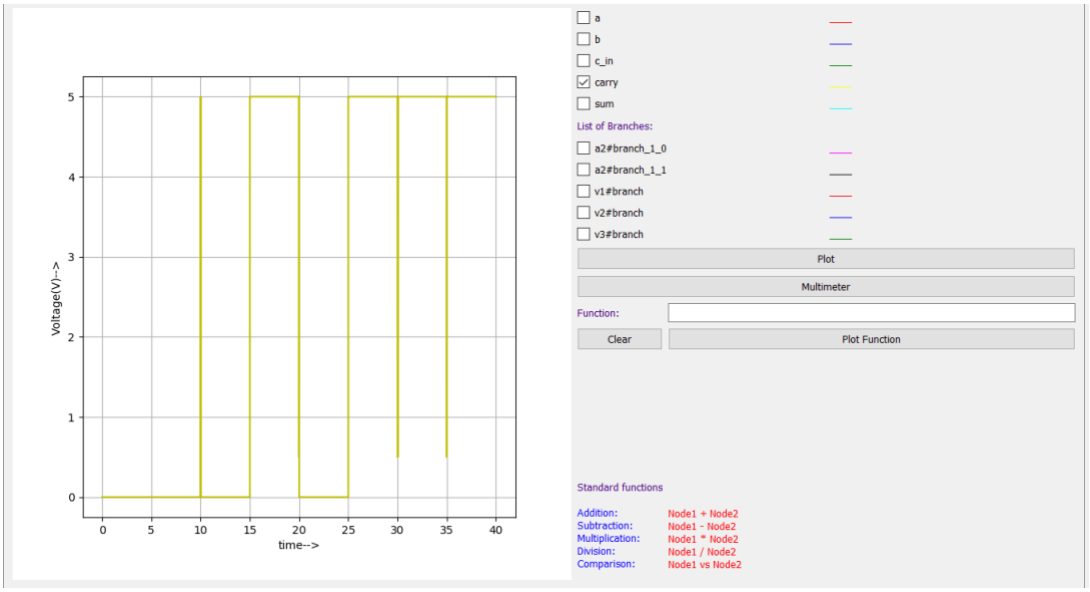


Outputs:

Sum:



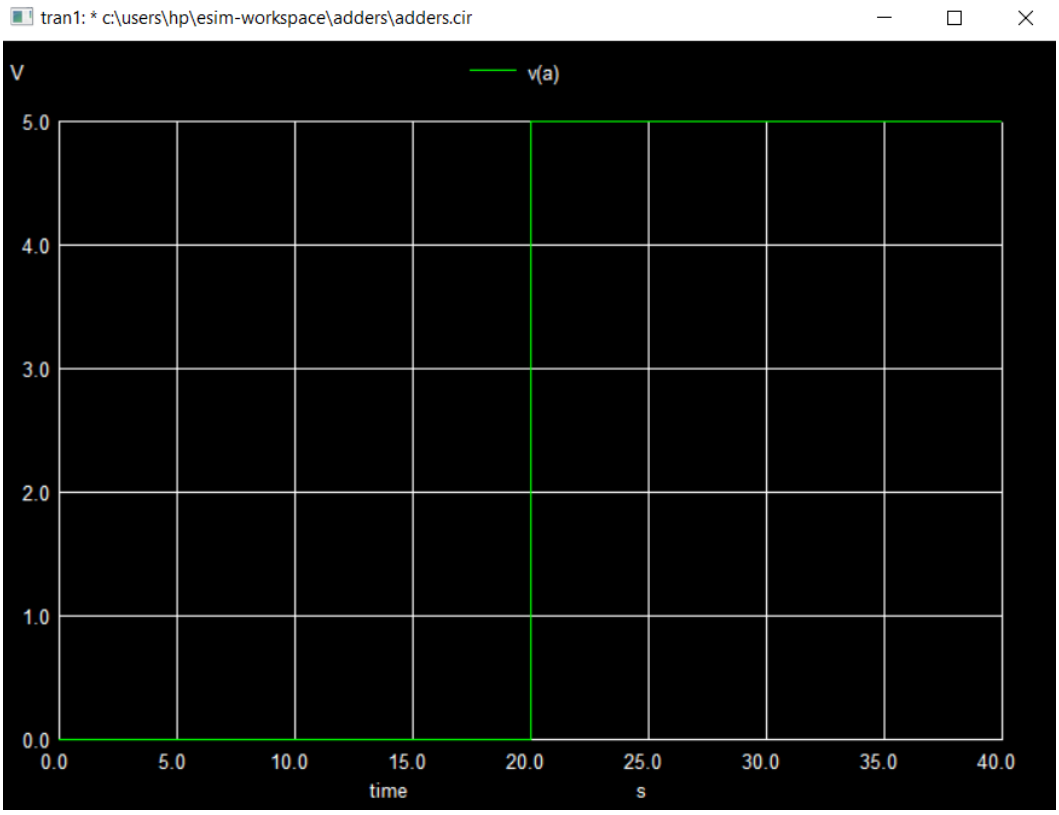
Carry:



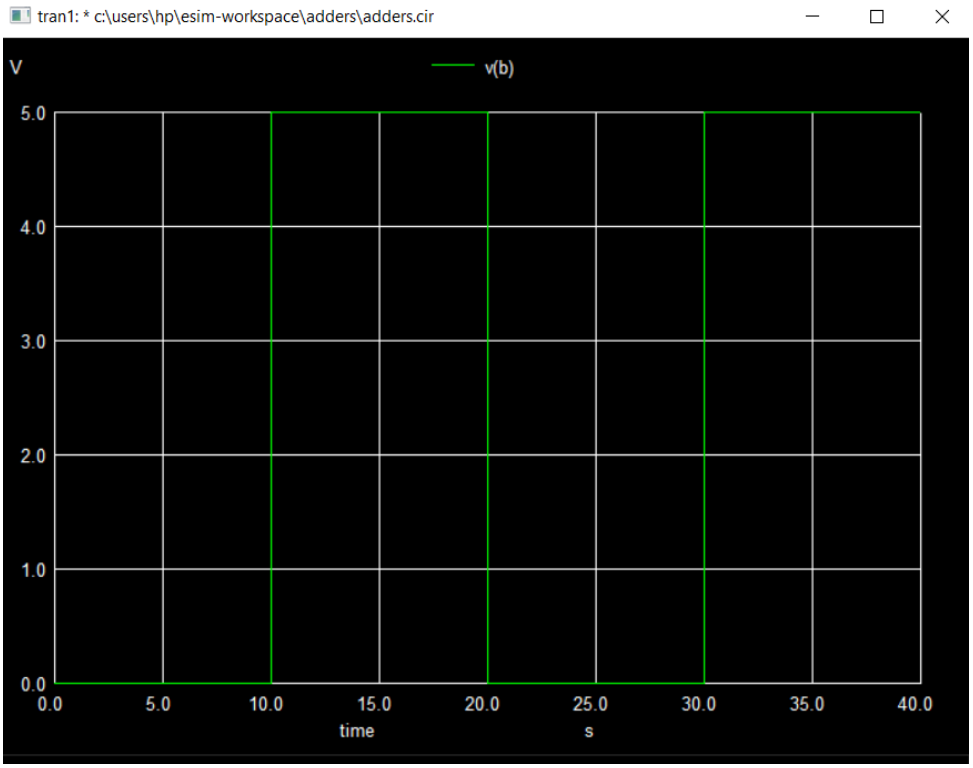
Ngspice Plots:

Inputs:

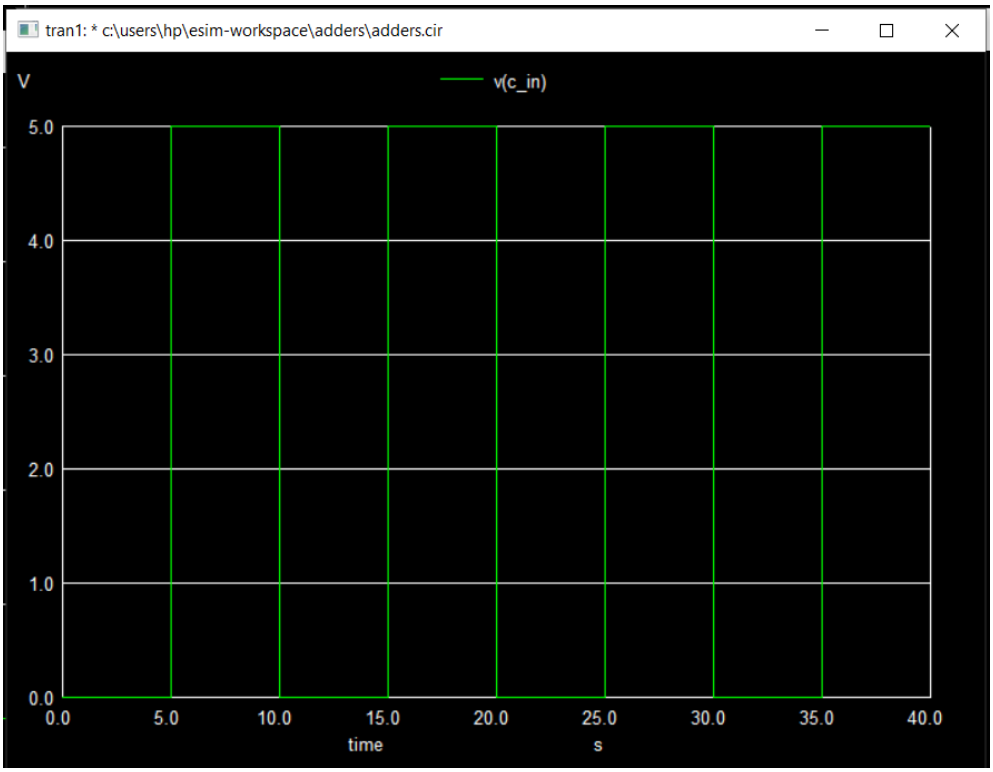
A



B

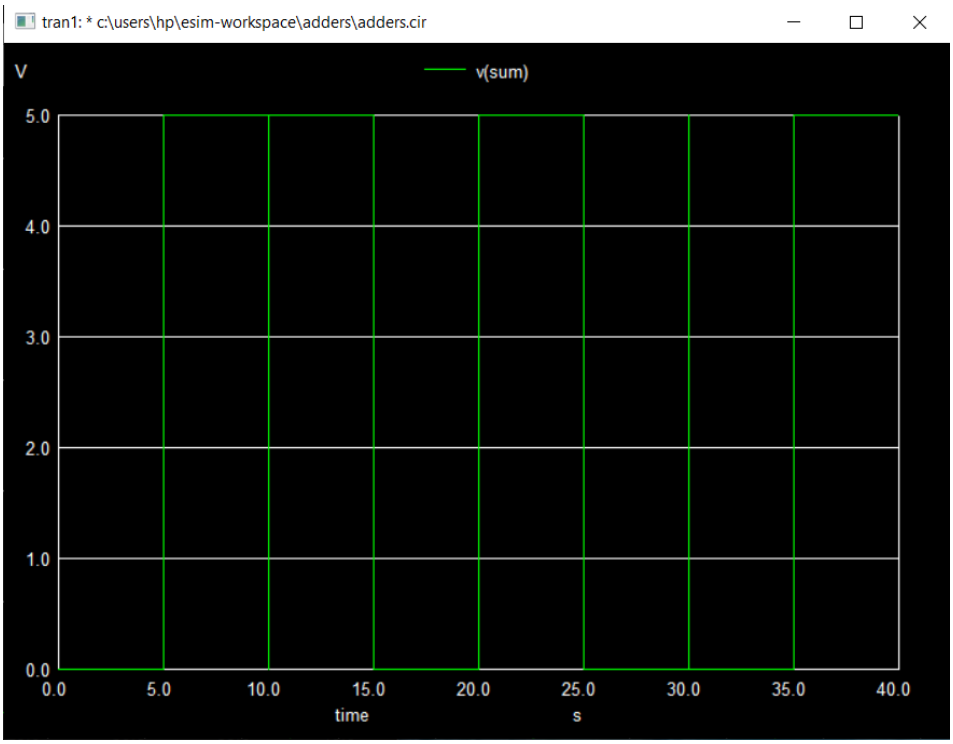

tran1: * c:\users\hp\esim-workspace\adders\adders.cir
V
v(b)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
5.0
10.0
15.0
20.0
25.0
30.0
35.0
40.0
time
s

C_in

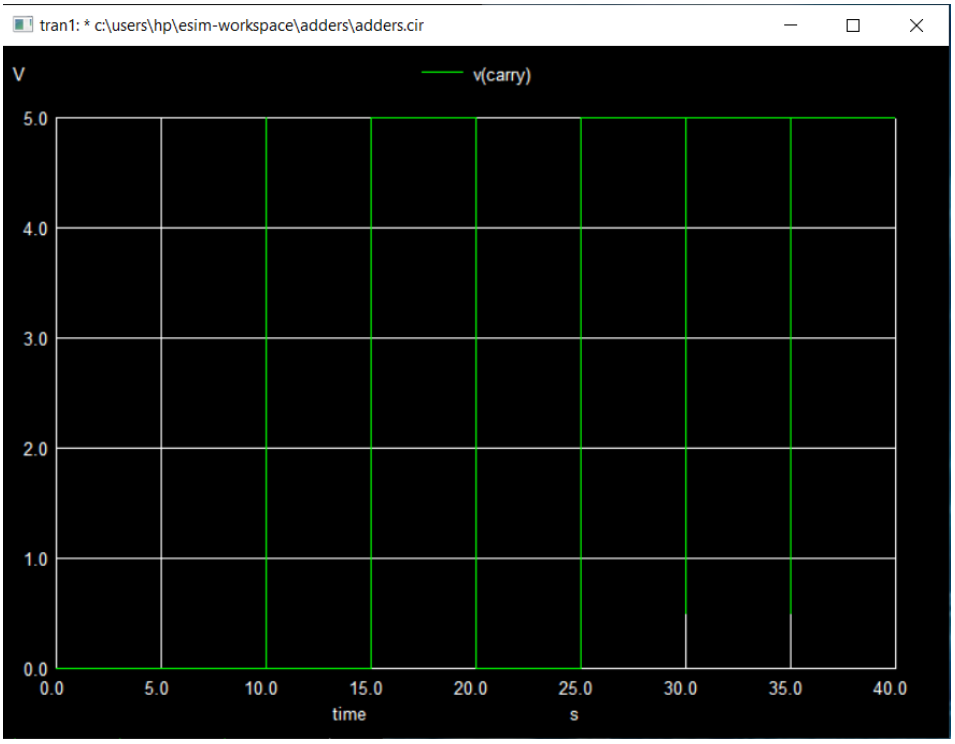

tran1: * c:\users\hp\esim-workspace\adders\adders.cir
V
v(c_in)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
5.0
10.0
15.0
20.0
25.0
30.0
35.0
40.0
time
s

Outputs:

Sum:



Carry:



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- https://www.youtube.com/watch?v=u863cwgdlnA