Circuit Simulation Project

https://esim.fossee.in/circuit-simulation-project

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Project Guide: Dr R. Maheshwari

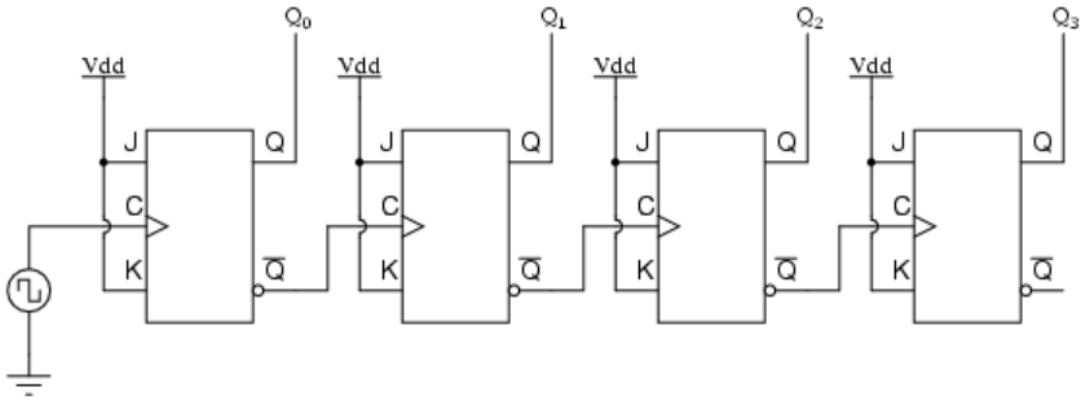
Title of the Circuit: 4-Bit Asynchronous Up Counter using JK Flip Flop

Description:

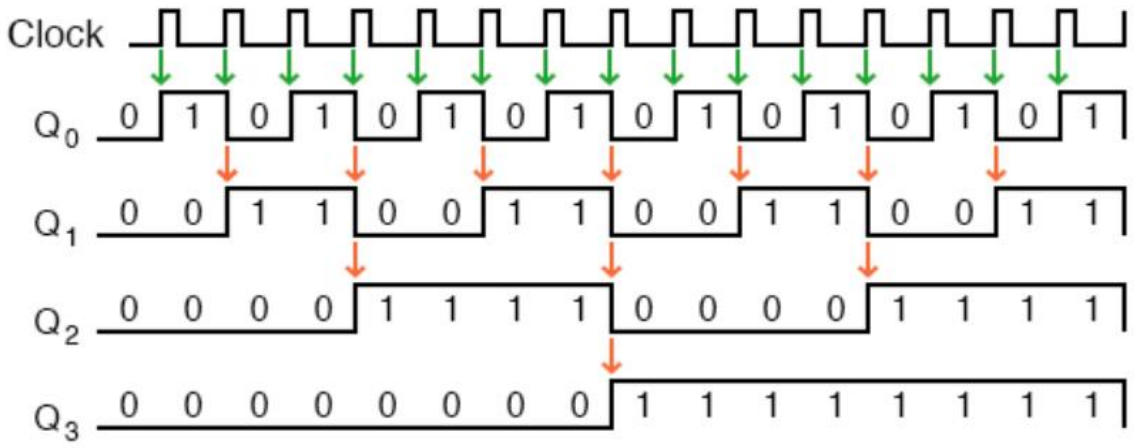
A counter is a device which can count any particular event on the basis of how many times the particular event(s) is occurred. In a digital logic system or computers, this counter can count and store the number of times any particular event or process have occurred, depending on a clock signal. Most common type of counter is sequential digital logic circuit with a single clock input and multiple outputs. The outputs represent binary or binary coded decimal numbers. Each clock pulse either increase the number or decrease the number.

Asynchronous counter can count using **Asynchronous clock input**. Counters can be easily made using flip-flops. As the count depends on the clock signal, in case of an Asynchronous counter, changing state bits are provided as the clock signal to the subsequent flip-flops. Those Flip-flops are serially connected together, and the clock pulse ripples through the counter. Due to the ripple clock pulse, it's often called a ripple counter. An Asynchronous counter can count $\mathbf{2^n - 1}$ possible counting states.

Circuit :

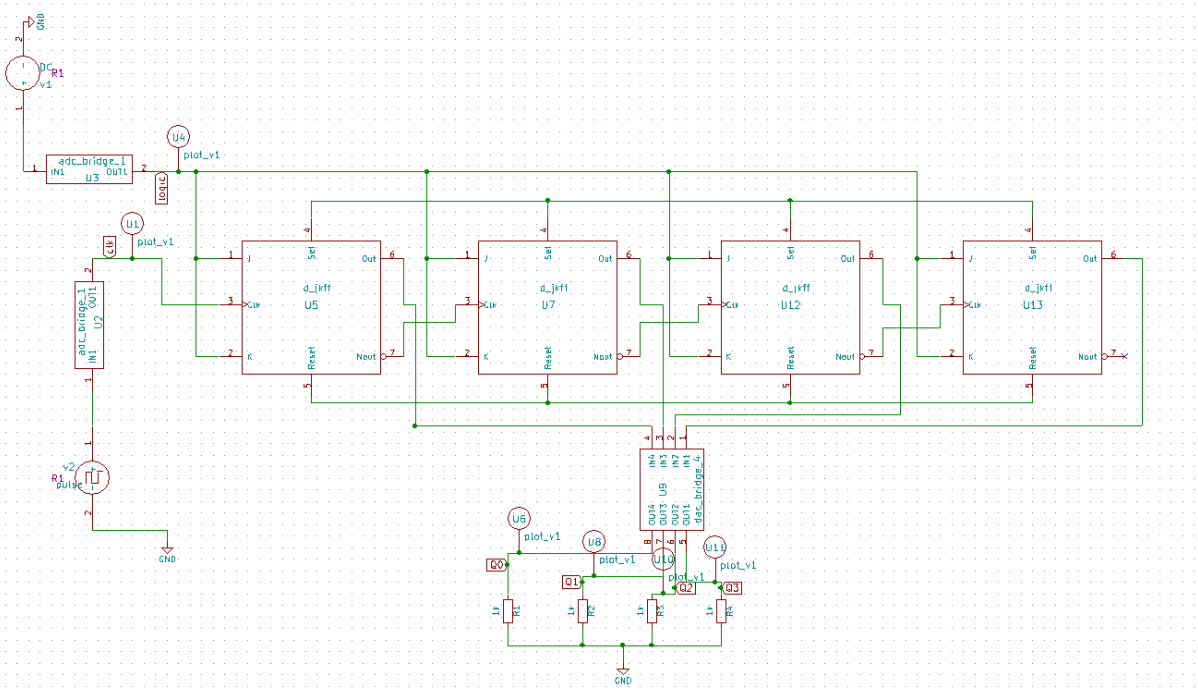


Output :



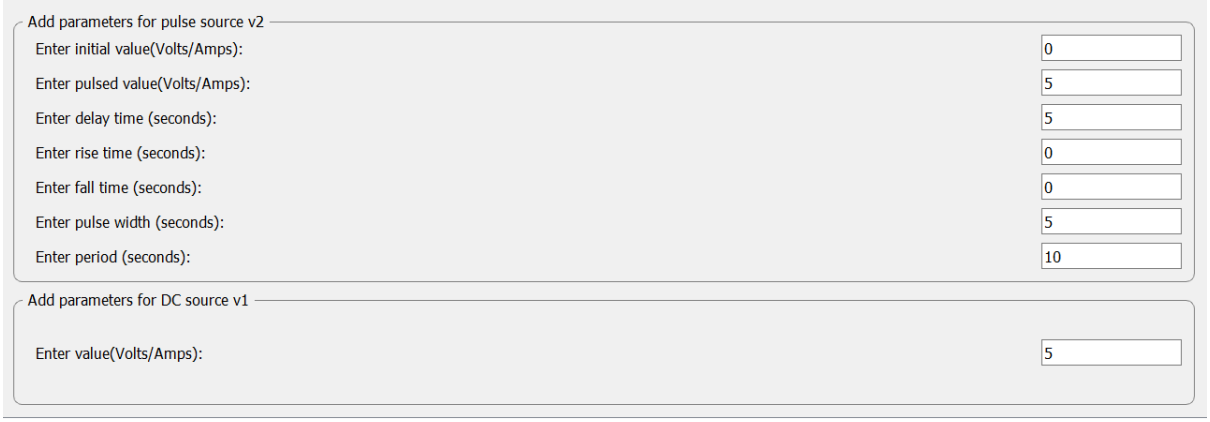
An “up” counter may be made by connecting the clock inputs of positive-edge triggered J-K flip-flops to the Q’ outputs of the preceding flip-flops. The J and K inputs of all flip-flops are connected to V_{cc} or V_{dd} so as to always be “high.” Counter circuits made from cascaded J-K flip-flops where each clock input receives its pulses from the output of the previous flip-flop invariably exhibit a ripple effect.

e-Sim Schematic :

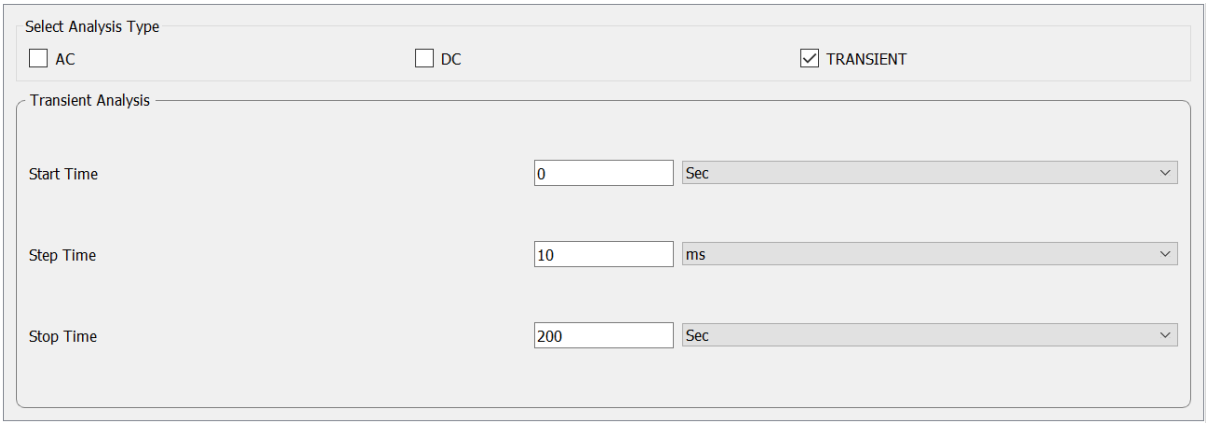


In this circuit Q0 represents LSB and Q3 represents MSB.

Source details :



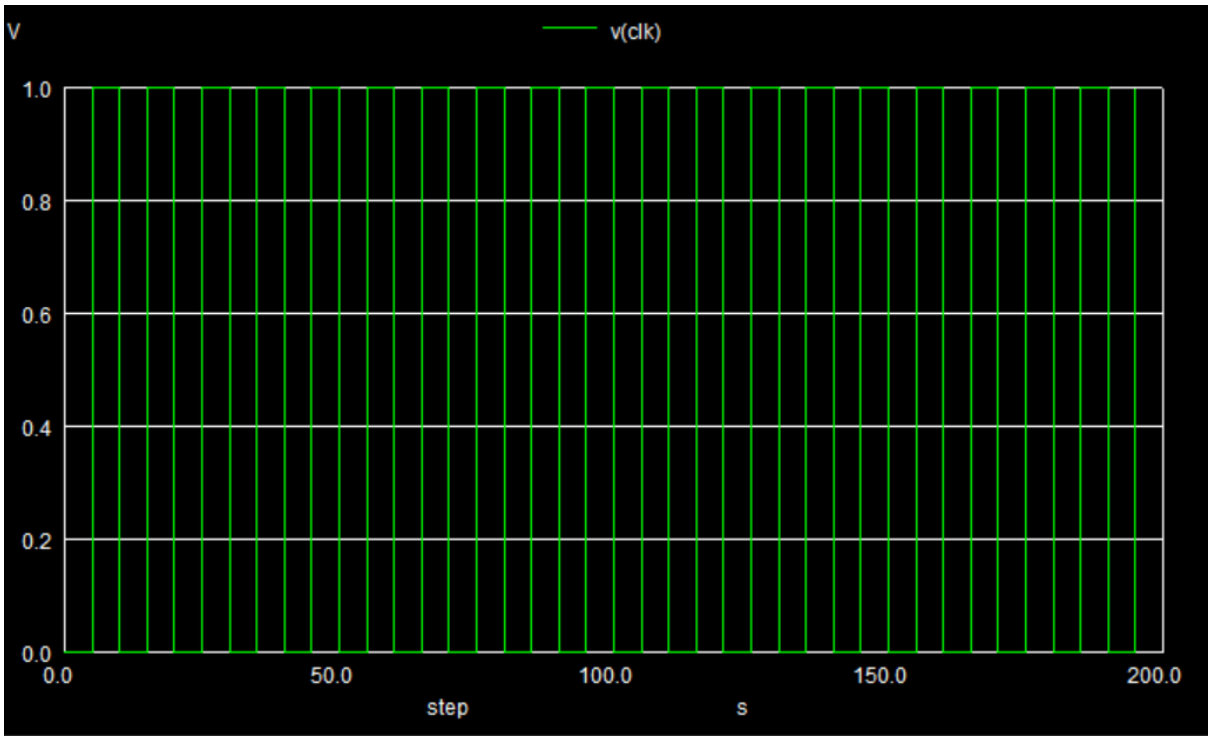
Transient details :



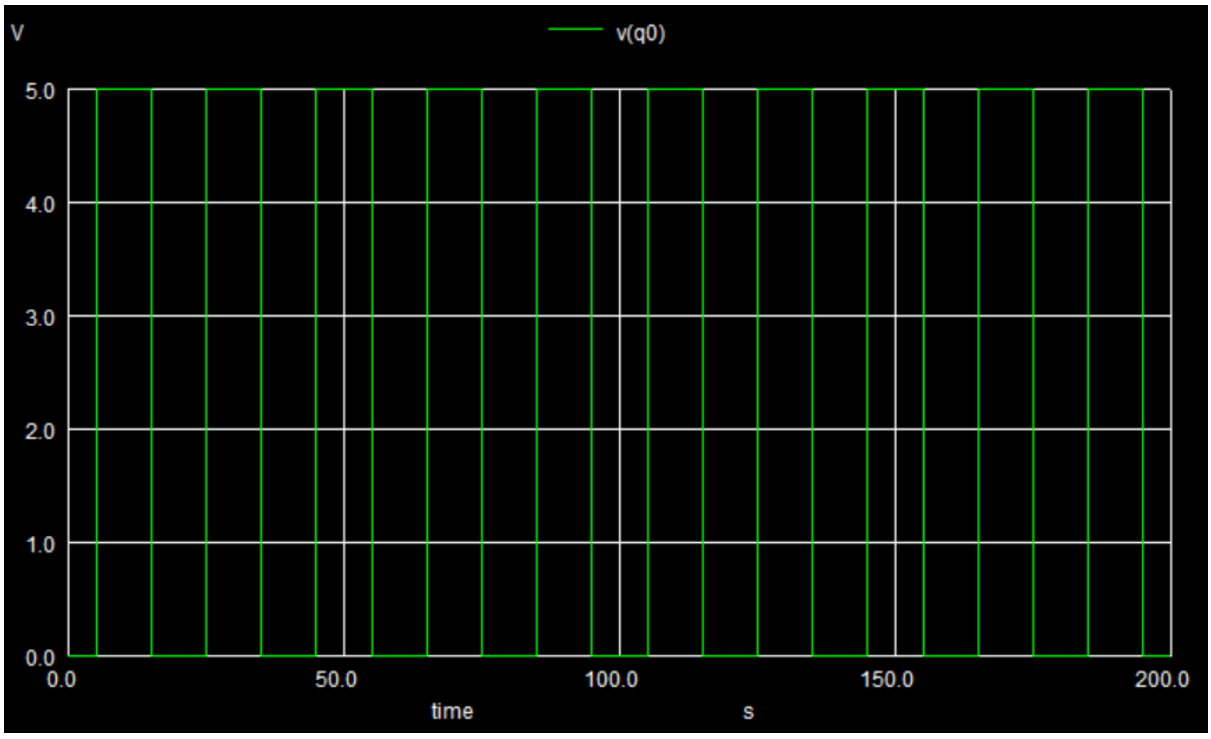
Simulation results :

1.NgSpice Waveforms

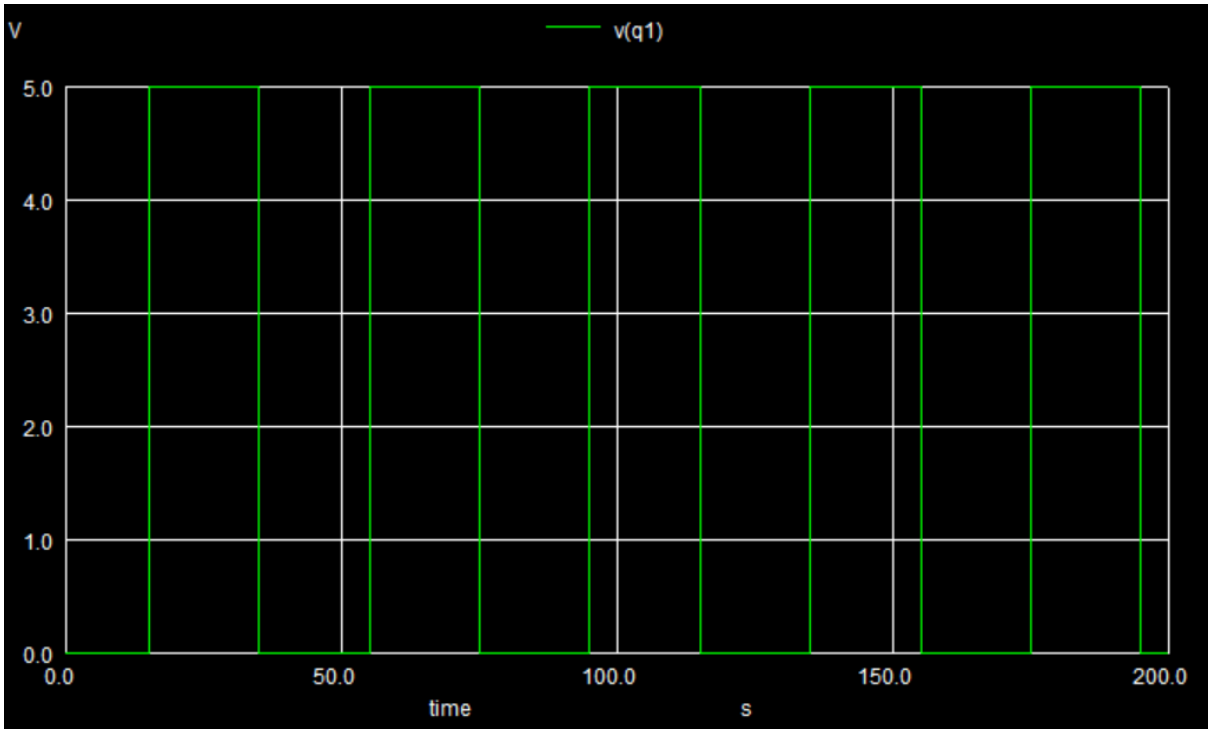
clk (Clock Pulse)



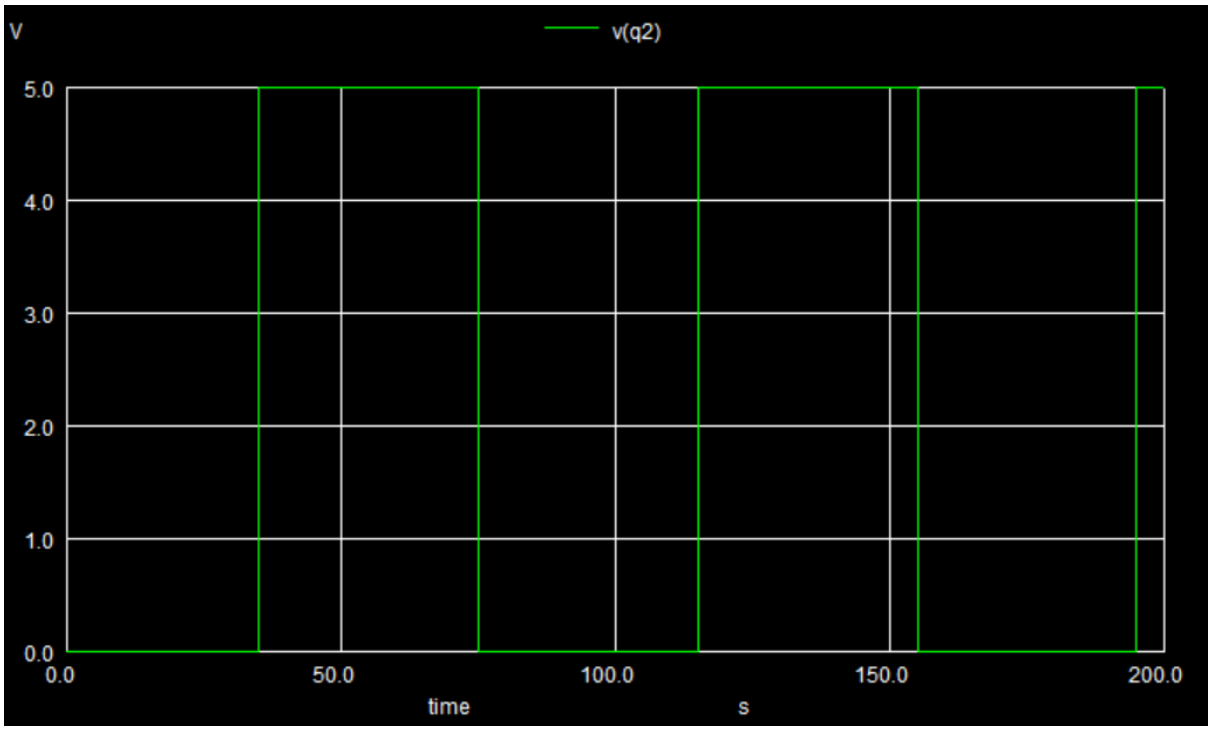
Q0 (LSB)



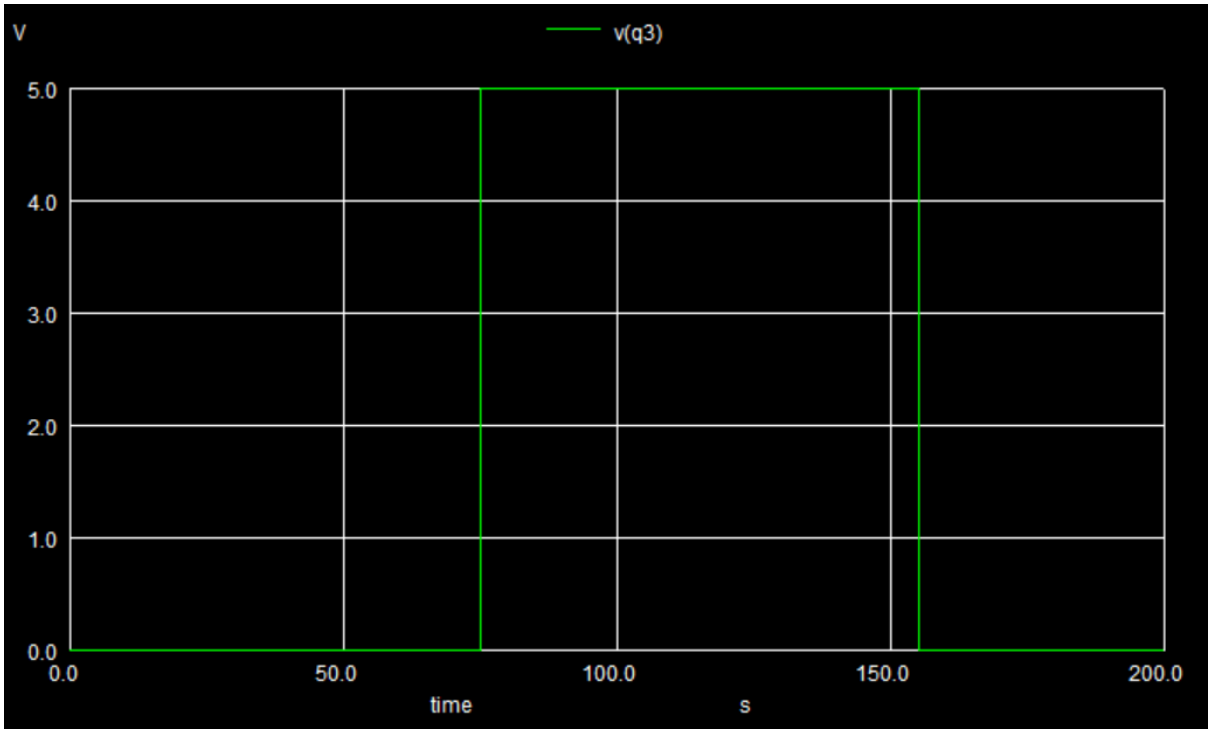
Q1


V
v(q1)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
50.0
100.0
150.0
200.0
time
s

Q2

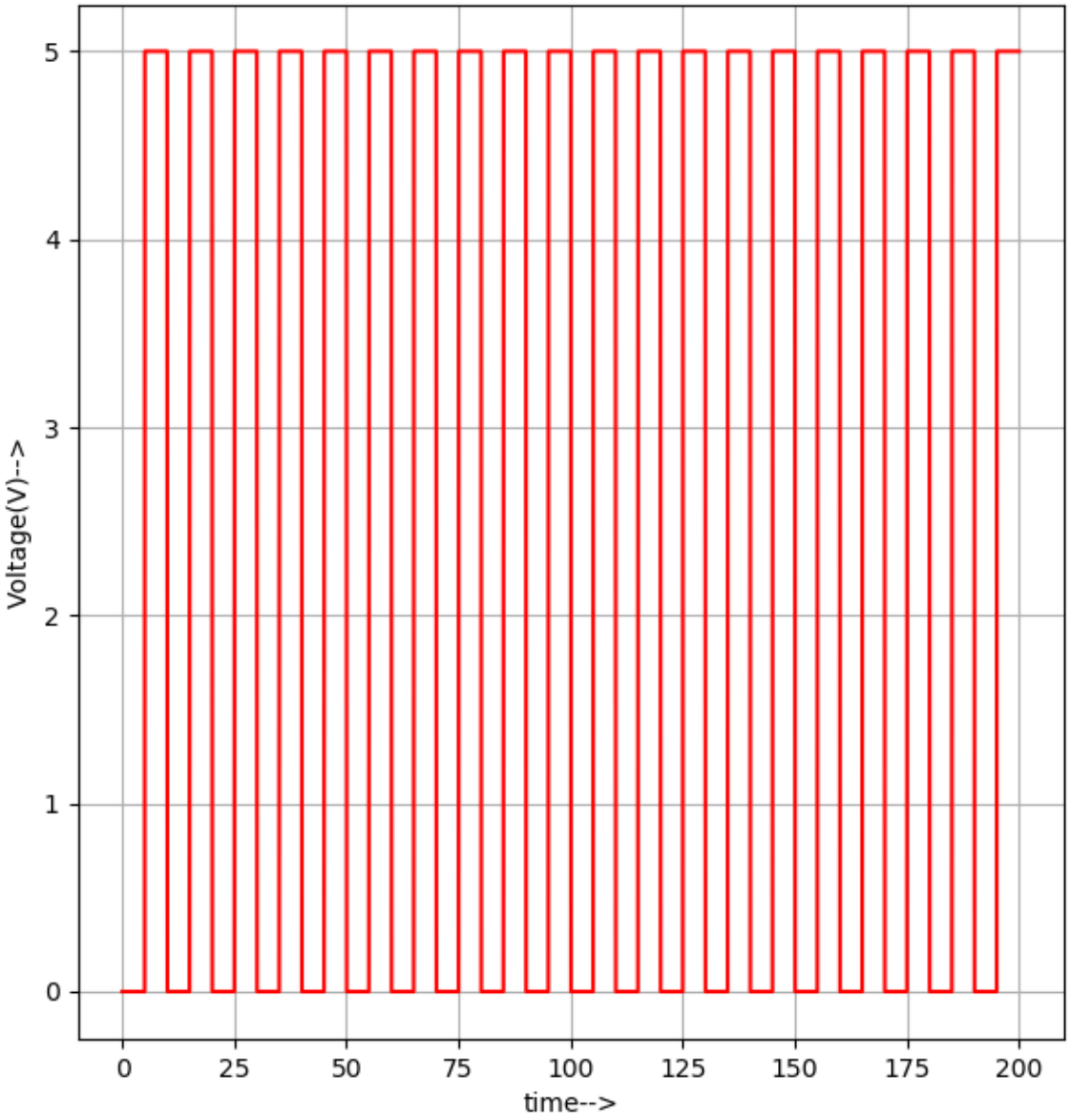

V
v(q2)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
50.0
100.0
150.0
200.0
time
s

Q3 (MSB)

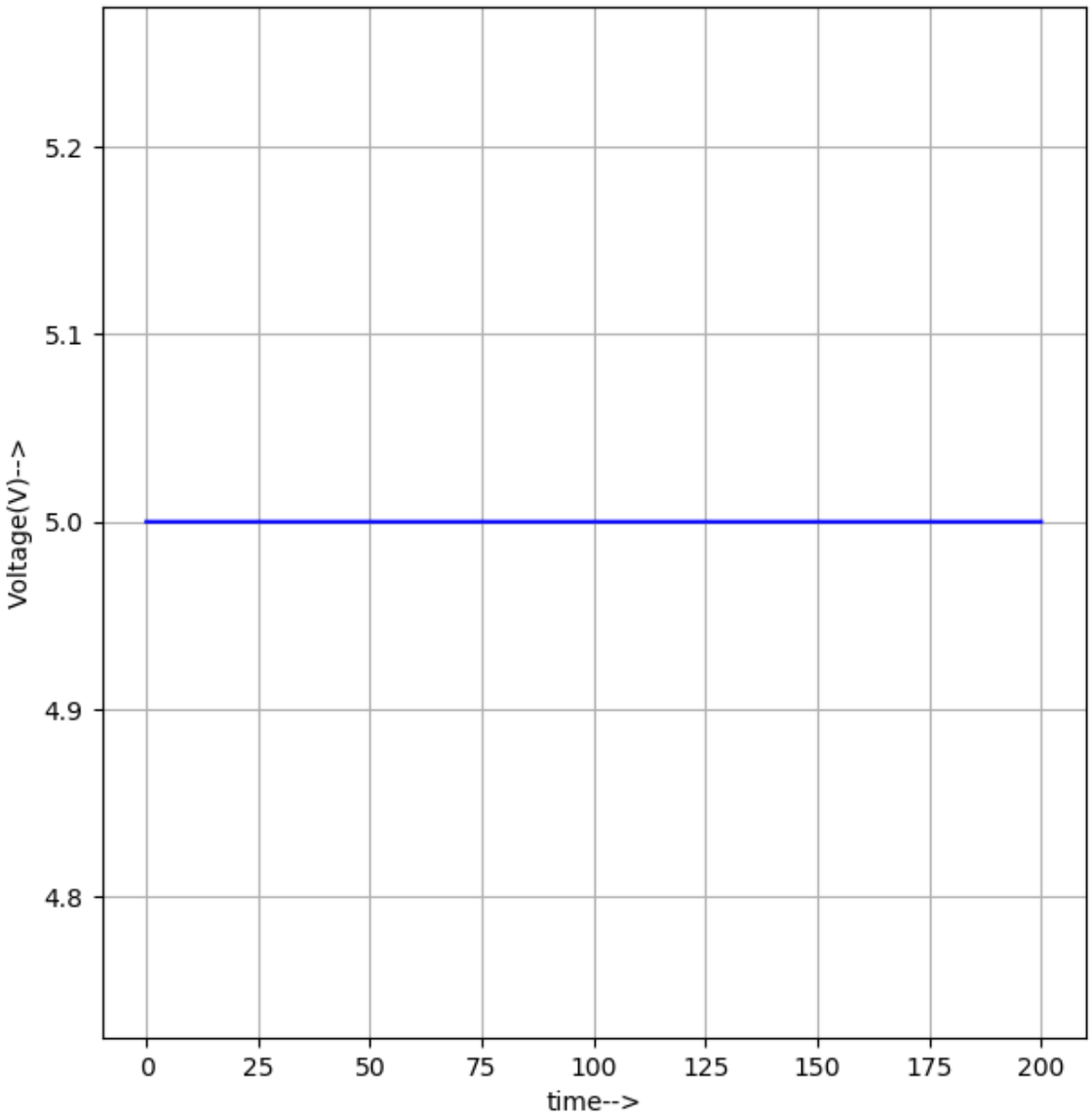


2.Python Waveform

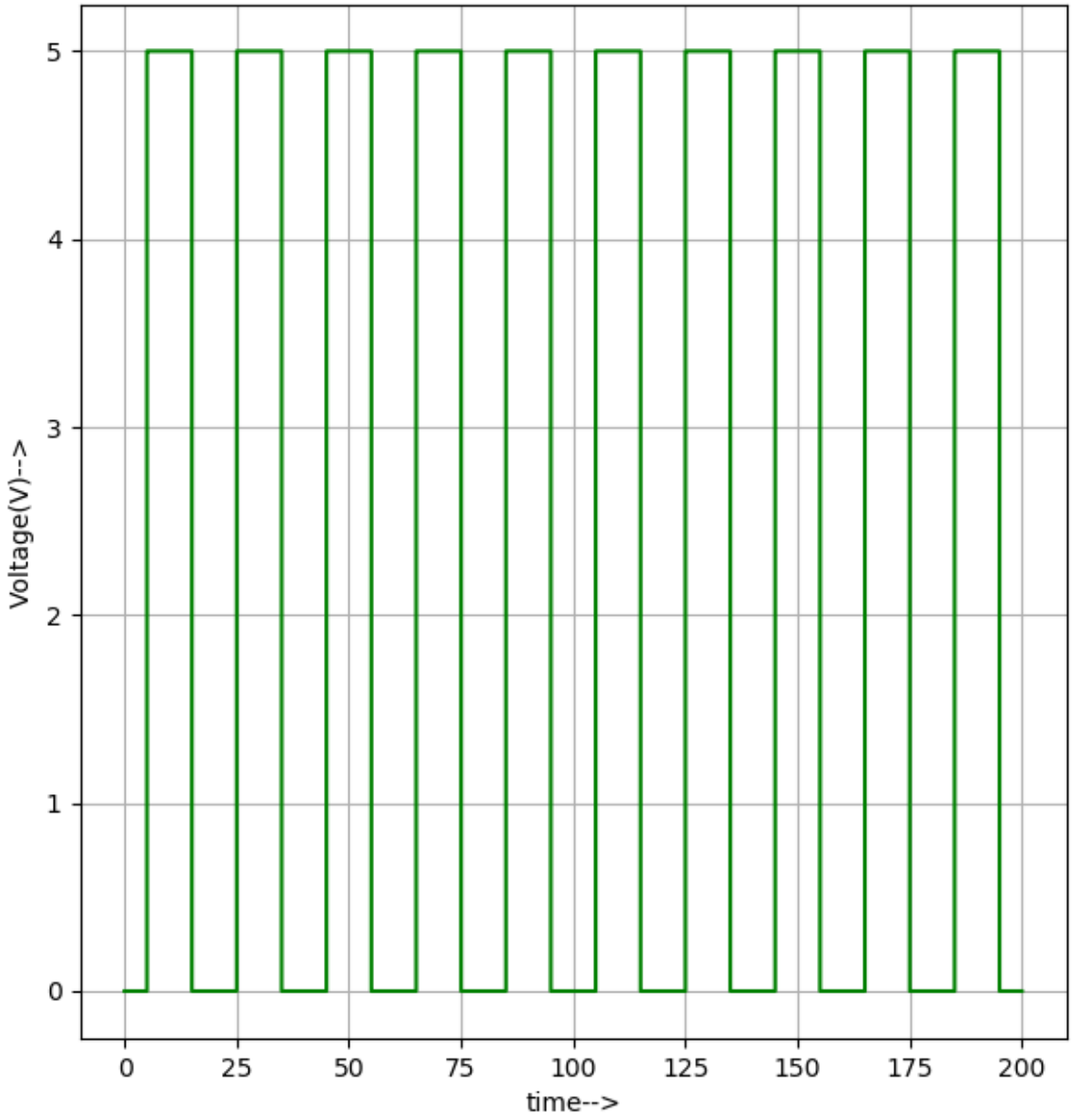
clk (Clock pulse)



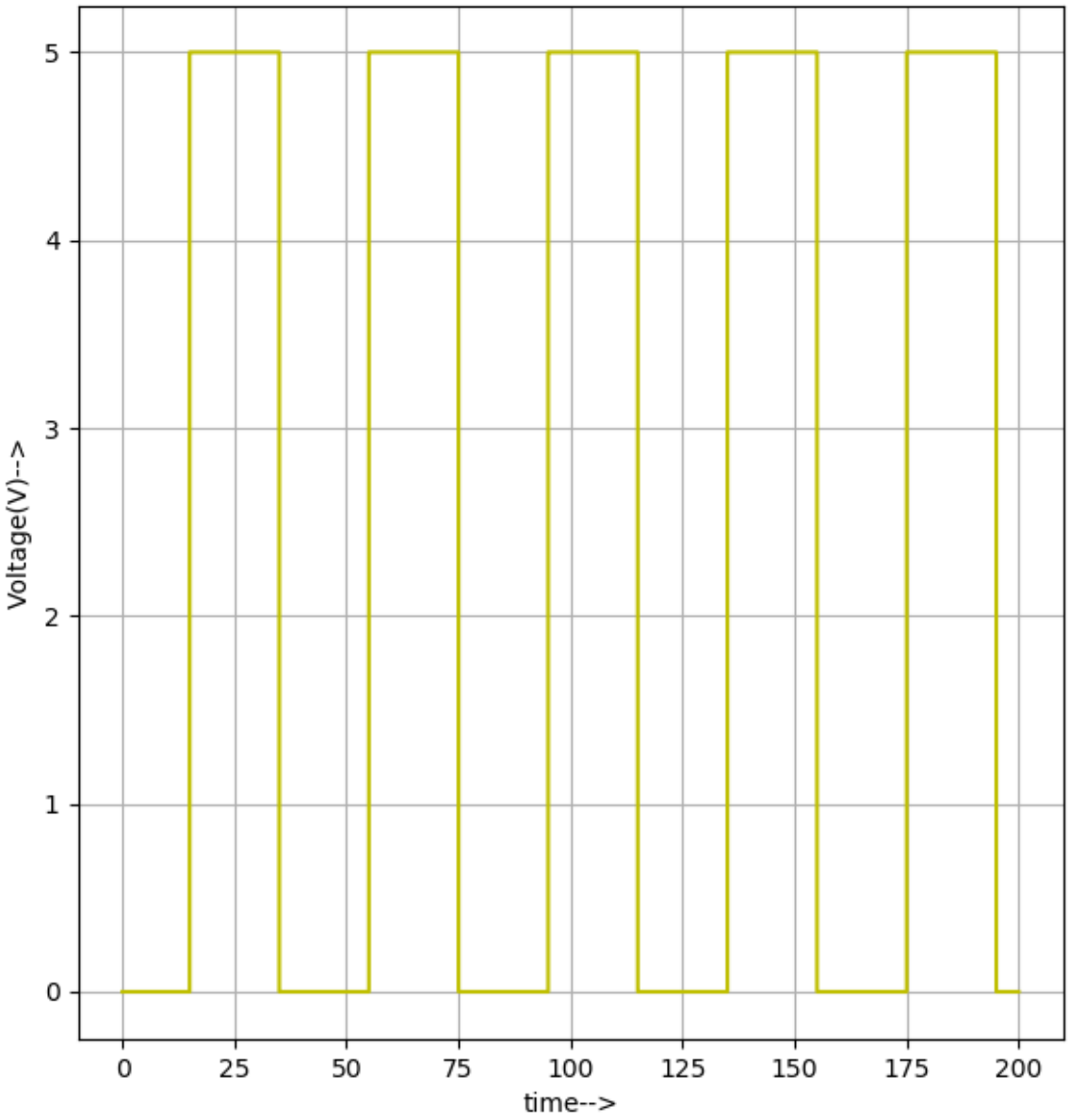
Logic



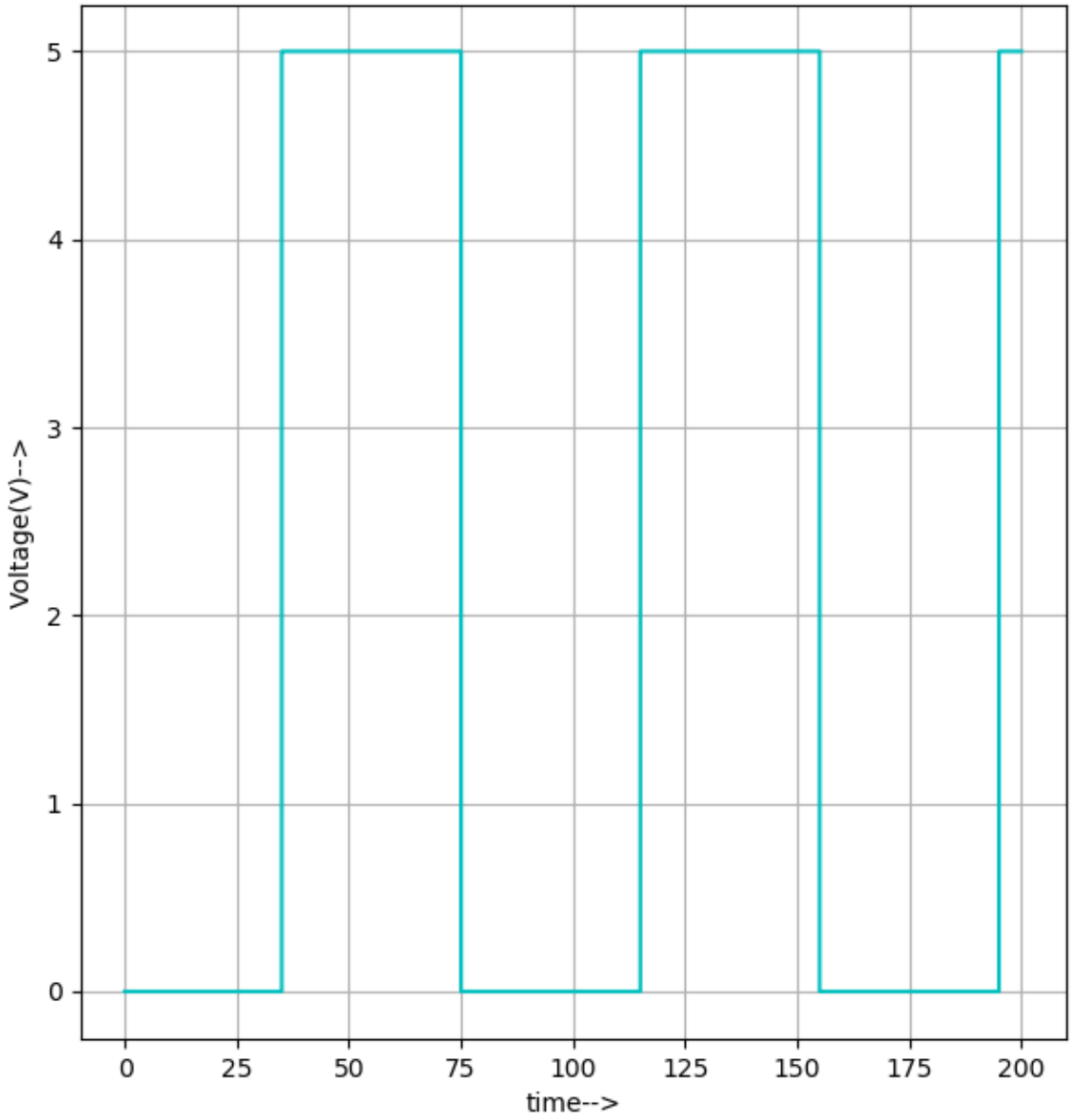
Q0 (LSB)



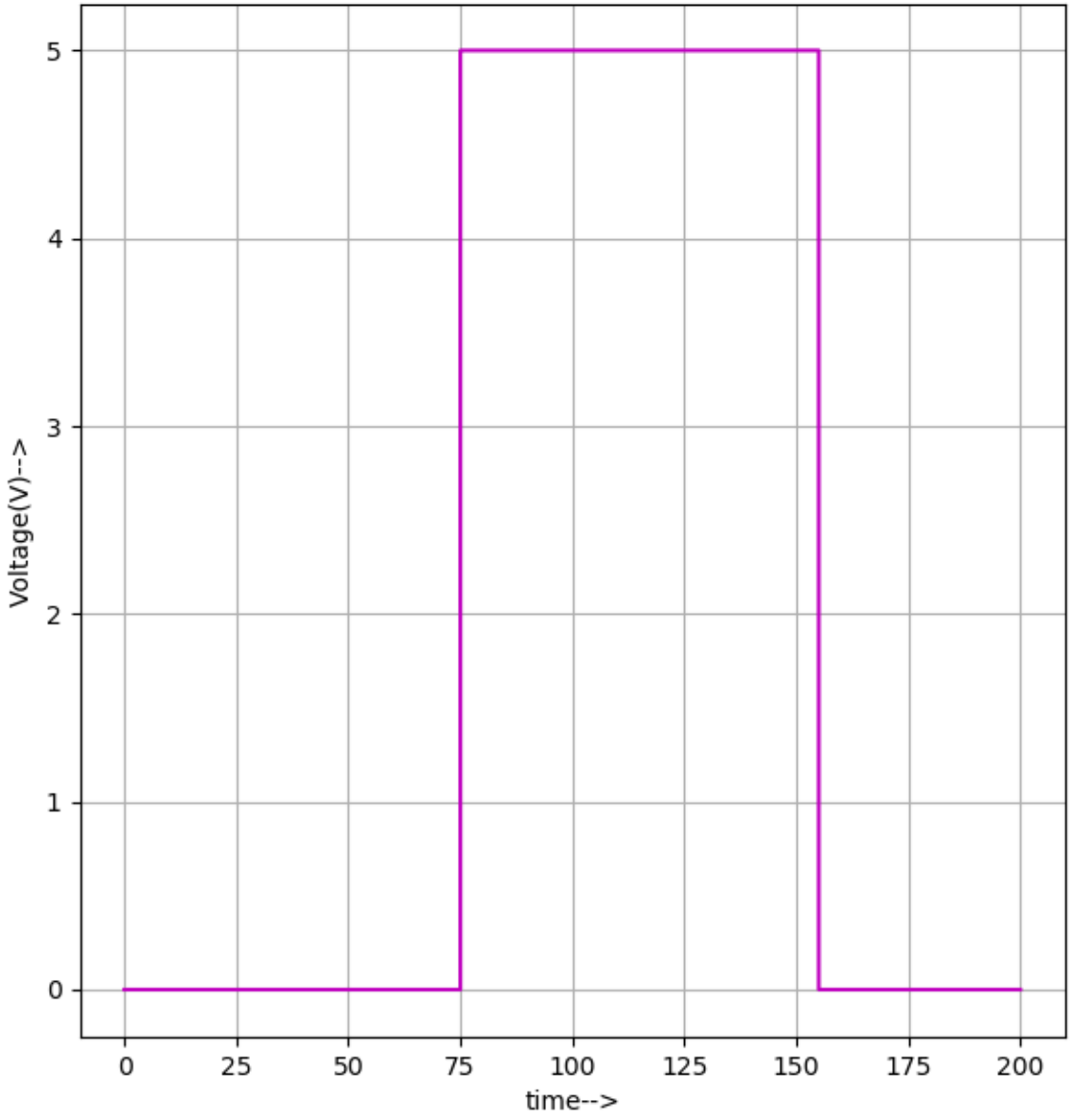
Q1



Q2



Q3 (MSB)



Reference:

https://www.allaboutcircuits.com/textbook/digital/chpt-11/asynchronous-counters/

https://circuitdigest.com/tutorial/asynchronous-counter