





CIRCUIT SIMULATON PROJECT

https://esim.fossee.in/circuit-simulation-project

Name of Participant: Vinay Karnati

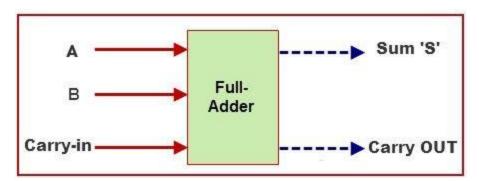
Project Guide: Dr. Maheswari. R

Full Adder using 3 to 8 decoders

Theory:

FULL ADDER - This adder is difficult to implement than a half-adder. The difference between a half-adder and a full-adder is that the full-adder has three inputs and two outputs, whereas half adder has only two inputs and two outputs. The first two inputs are A and B and the third input is an input carry as C-IN.

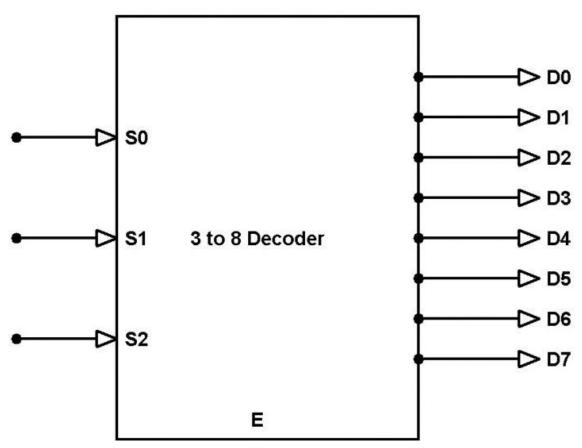
A full adder is a digital circuit that performs addition. Full adders are implemented with logic gates in hardware. A full adder adds three one-bit binary numbers, two operands and a carry bit. The adder outputs two numbers, a sum and a carry bit.



Then the full adder is a logical circuit that performs an addition operation on three binary digits and just like the half adder, it also generates a carry out to the next addition column. Then a Carry-in is a possible carry from a less significant digit, while a Carry-out represents a carry to a more significant digit.

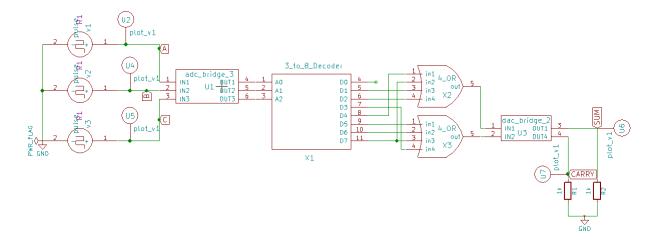
Decoder - A decoder is a combinational logic circuit which is used to change the code into a set of signals. It is the reverse process of an encoder. A decoder circuit takes multiple inputs and gives multiple outputs. A decoder circuit takes binary data of 'n' inputs into '2" unique output

3 Line to 8 Line Decoder - This decoder circuit gives 8 logic outputs for 3 inputs. The circuit is designed with AND and OR logic gates. It takes 3 binary inputs and activates one of the eight outputs. 3 to 8 line decoder circuit is also called as binary to an octal decoder.

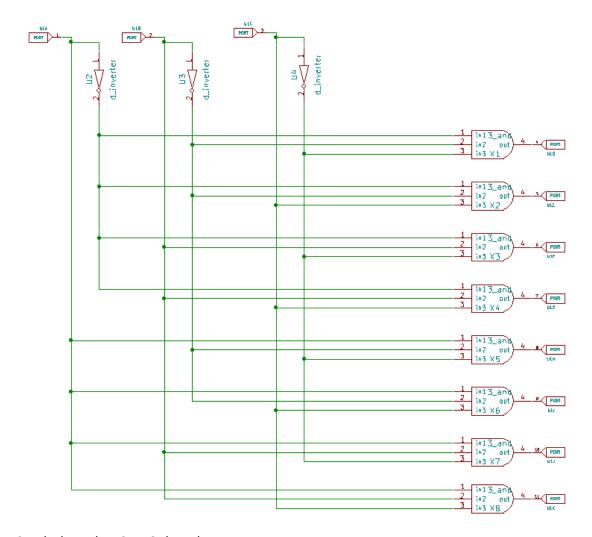


Circuit Diagram:

This is the main functional circuit schematic for the full adder which uses a 3:8 decoder.



This is the circuit schematic for the 3 to 8 decoder used in the main schematic.



Symbol used as 3 to 8 decoder:

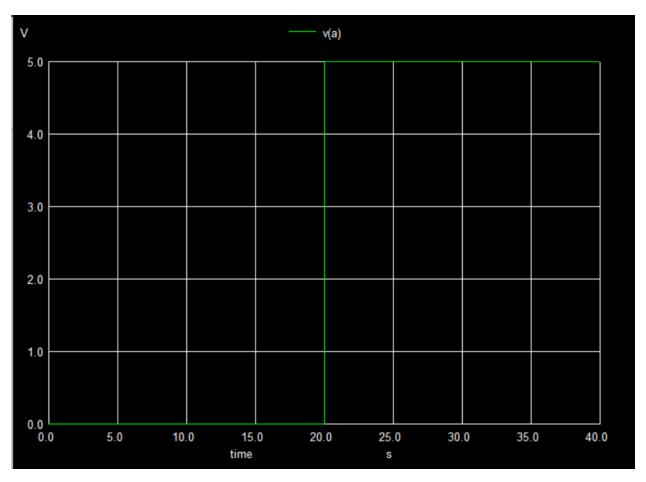
	3_to_8	Decoder	
2	A0 A1 A2	D0 D1 D2 D3	5 6 7 8
		D5 D6 D7	10 11 0
		?	

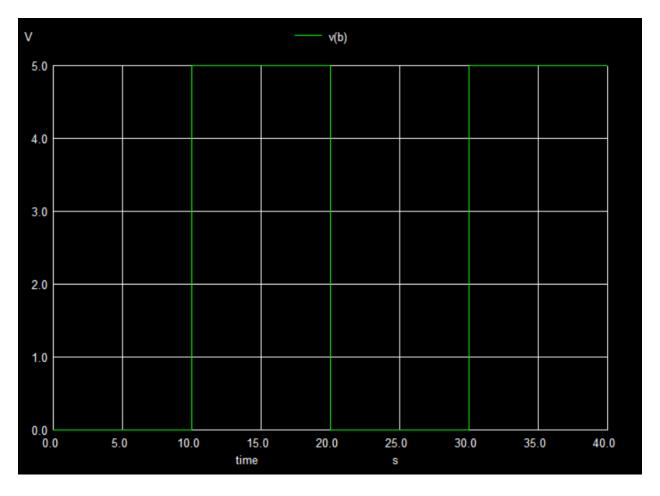
Simulation Results:

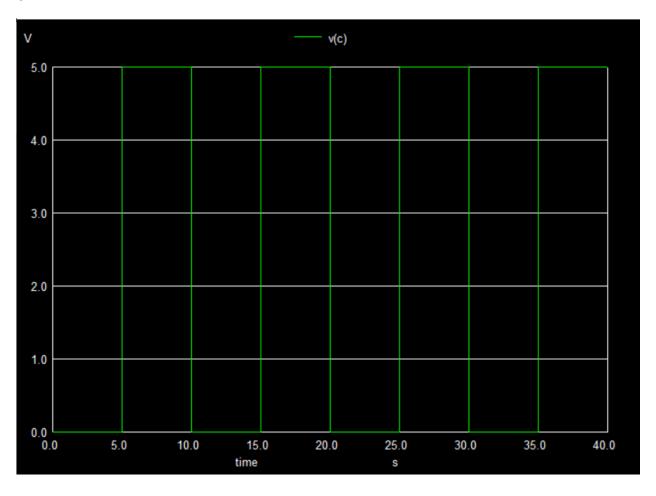
Ngspice plots:

Input waveforms:

A:

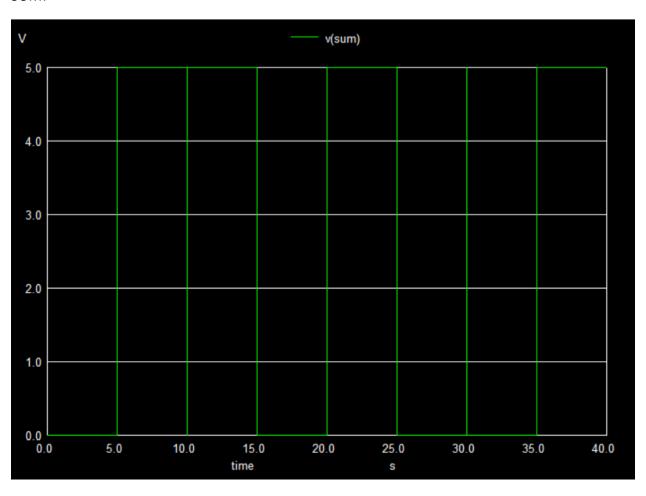




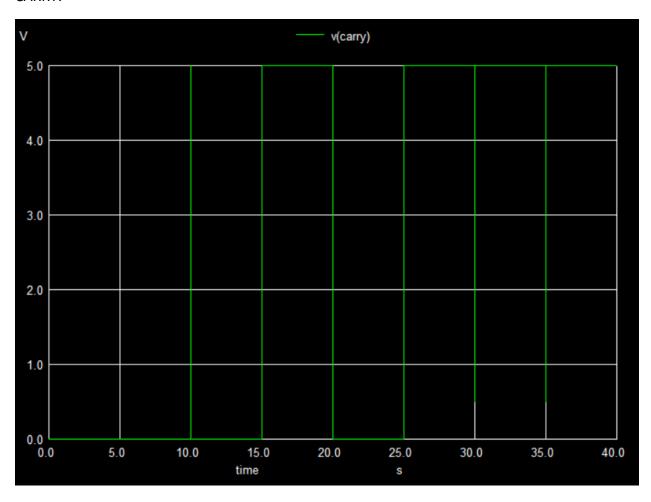


OUTPUT:

SUM:



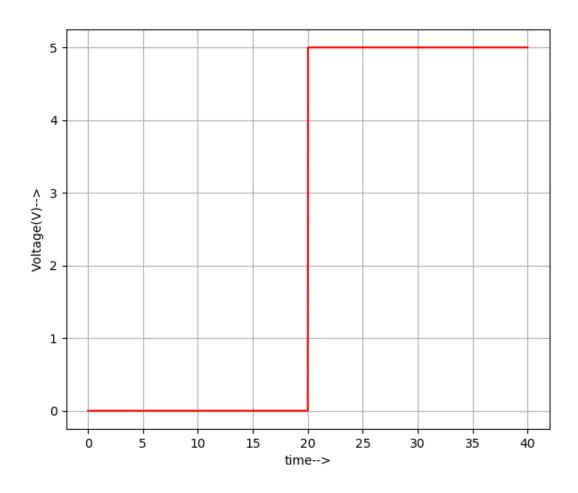
CARRY:

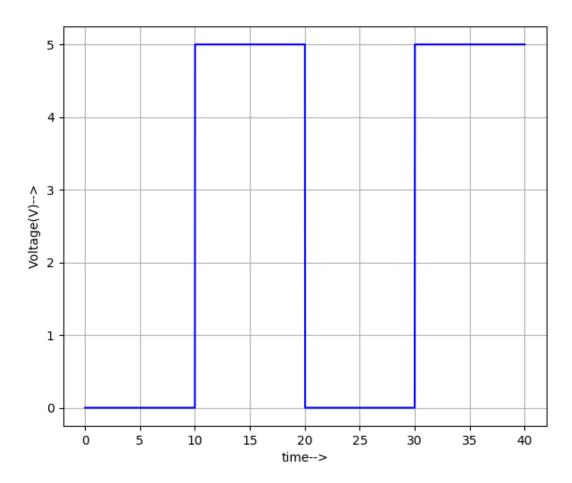


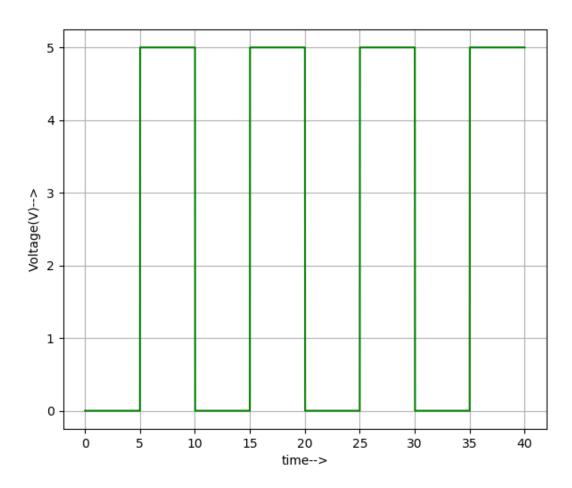
Python plots:

INPUT:

A:

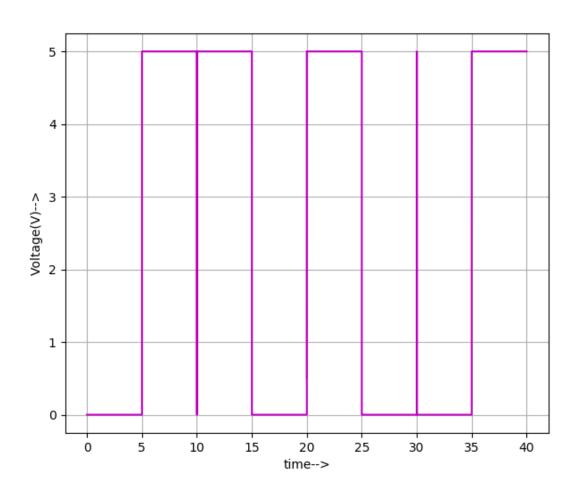




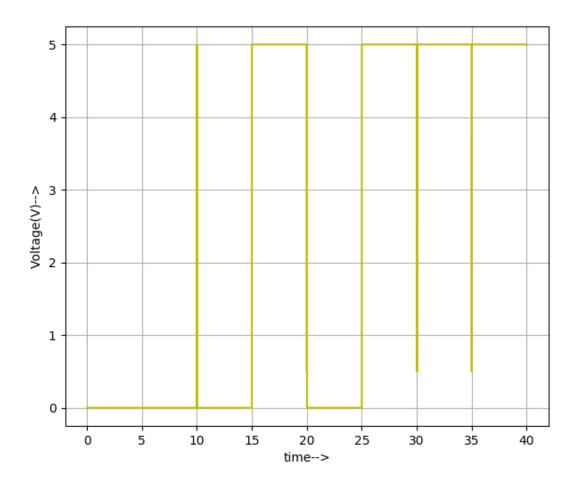


OUTPUT:

SUM:



CARRY:



References:

http://www.exploreroots.com/dc22.html

https://www.electroniclinic.com/decoder-3-to-8-decoder-block-diagram-truth-table-and-logic-diagram/https://www.deldsim.com/study/material/51/full-adder-function-using-38-decoder/