Circuit Simulation Project

https://esim.fossee.in/circuit-simulation-project

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Project Guide : Dr. Maheswari. R

Title of the project :

4-Bit Odd-Even Parity Generator and Checker

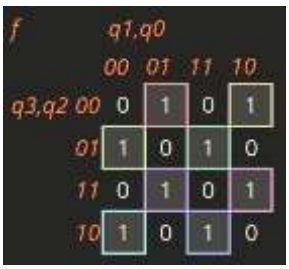
Theory/Description :

- 4-bit odd-even parity generator, appends the parity bit to the given data-word based on type of parity, odd parity means the codeword to be sent should have odd number of 1's and even parity means the codeword should have even number of 1's. The logical circuit can be formed using truth table and K-maps. Let the data-word be q3q2q1q0.

q3	q2	q1	q0	Even parity bit	Odd parity bit
0	0	0	0	0	1
0	0	0	1	1	0
0	0	1	0	1	0
0	0	1	1	0	1
0	1	0	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	1	0
1	0	0	0	1	0
1	0	0	1	0	1
1	0	1	0	0	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	1	1	0
1	1	1	0	1	0
1	1	1	1	0	1

K-maps :

Even parity bit –

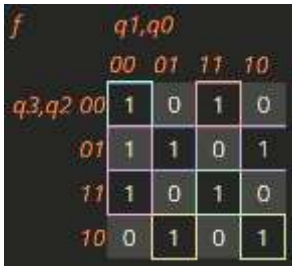


The formula generated is :

f(q3,q2,q1,q0) =

q3⊕q2⊕q1⊕q0

Odd parity bit –



The formula generated is :

f(q3,q2,q1,q0) =

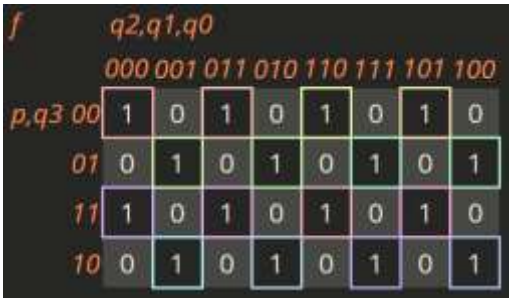
q3⊙q2⊙q1⊙q0

- 5-bit odd-even parity checker checks if the received codeword is correct or corrupted. The check value 0 means received data has error and value 1 means data is correct and can be accepted.

q3	q2	q1	q0	p (parity bit)	Even parity check	Odd parity check
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	1	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	0	1	0
0	1	1	1	0	0	1
1	0	0	0	0	0	1
1	0	0	1	0	1	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	0	1	0
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0
0	0	0	0	1	0	1
0	0	0	1	1	1	0
0	0	1	0	1	1	0
0	0	1	1	1	0	1
0	1	0	0	1	1	0
0	1	0	1	1	0	1
0	1	1	0	1	0	1
0	1	1	1	1	1	0
1	0	0	0	1	1	0
1	0	0	1	1	0	1
1	0	1	0	1	0	1
1	0	1	1	1	1	0
1	1	0	0	1	0	1
1	1	0	1	1	1	0
1	1	1	0	1	1	0
1	1	1	1	1	0	1

K-Maps :

Even parity check :

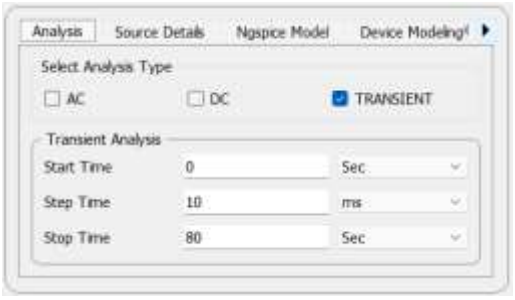


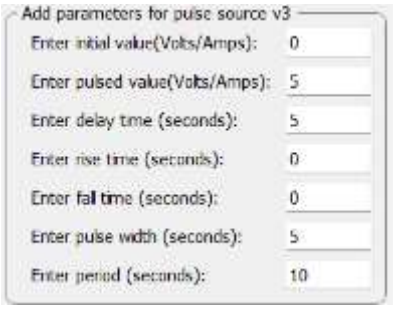
f(p,q3,q2,q1,q0) = p⊕q3⊕q2⊕q1⊕q0

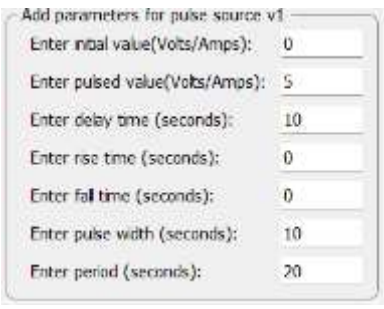
Odd parity check :

f(p,q3,q2,q1,q0) = (p⊕q3)⊙(q2⊕q1⊕q0)

4-Bit Odd/Even Parity Generator :







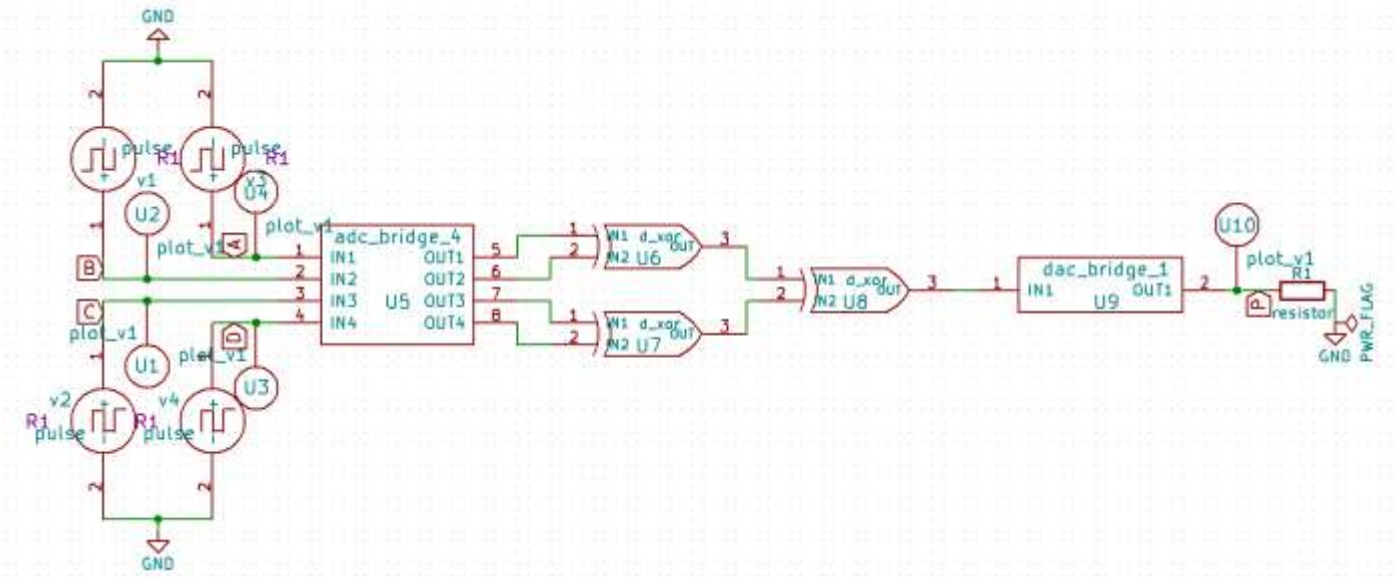
Add parameters for pulse source v4

Enter initial value(Volts/Amps):	0
Enter pulsed value(Volts/Amps):	5
Enter delay time (seconds):	40
Enter rise time (seconds):	0
Enter fall time (seconds):	0
Enter pulse width (seconds):	40
Enter period (seconds):	80

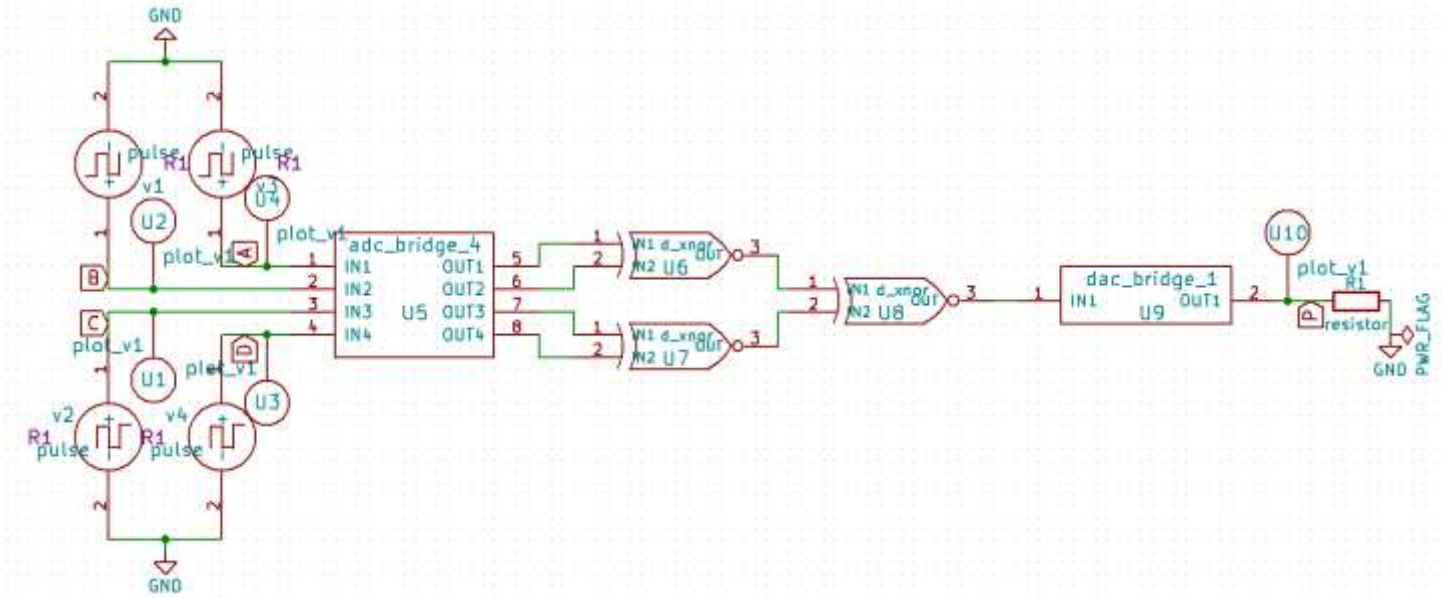
Add parameters for pulse source v2

Enter initial value(Volts/Amps):	0
Enter pulsed value(Volts/Amps):	5
Enter delay time (seconds):	20
Enter rise time (seconds):	0
Enter fall time (seconds):	0
Enter pulse width (seconds):	20
Enter period (seconds):	40

Even parity generator circuit :

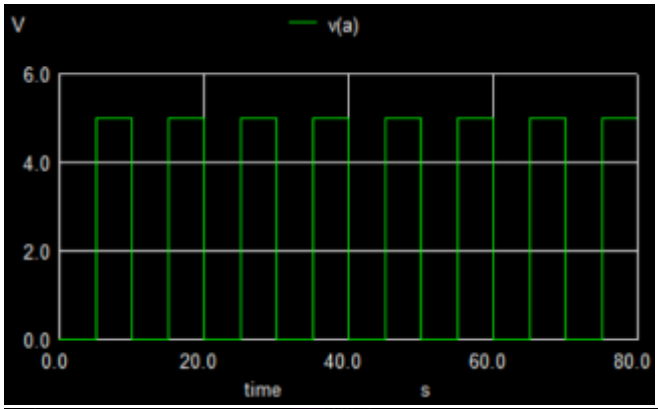


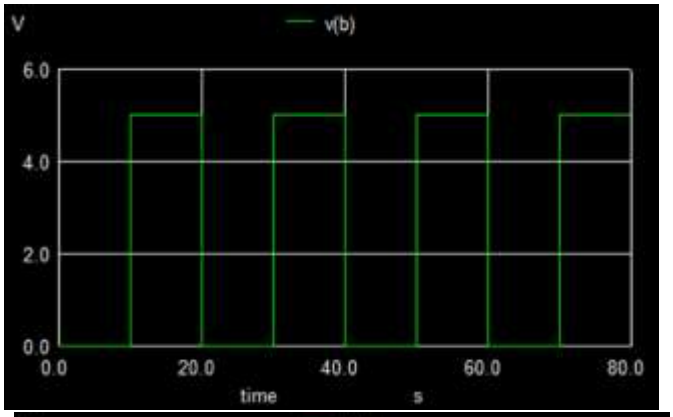
Even parity generator circuit :

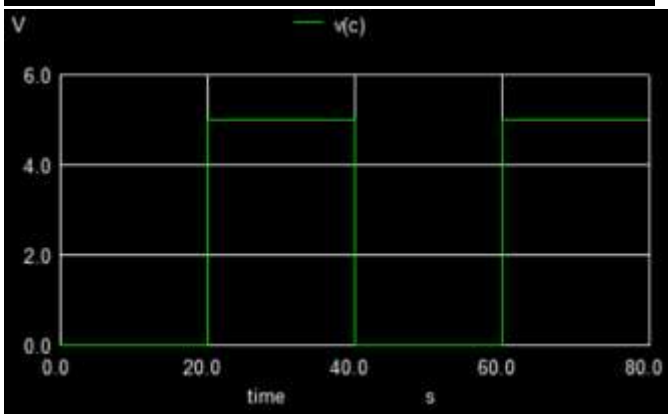


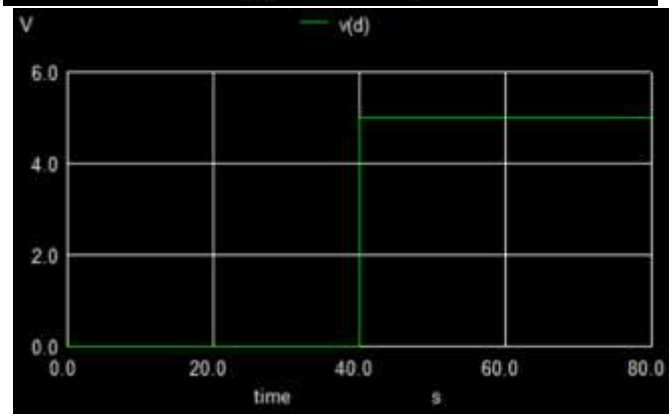
Input Waveforms :

Ngspice Plots :

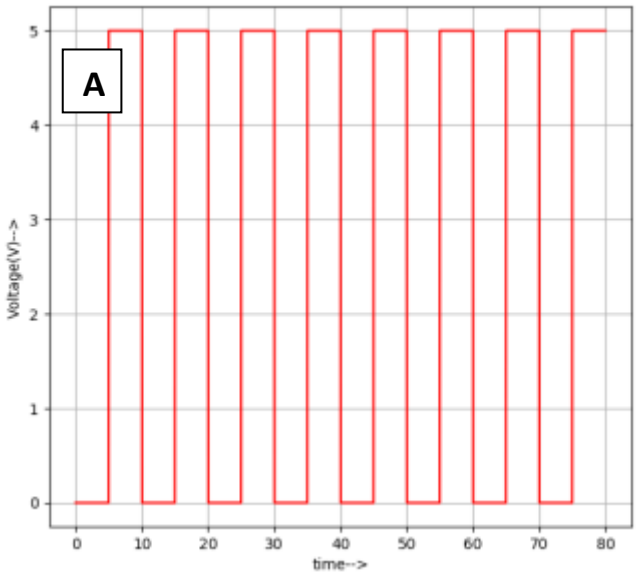


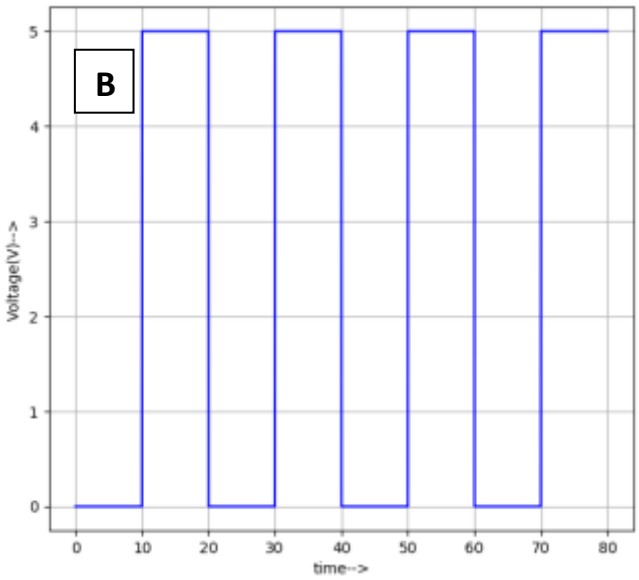


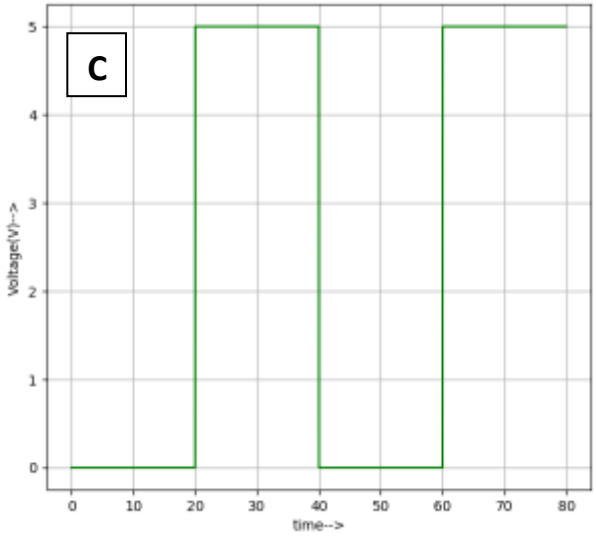


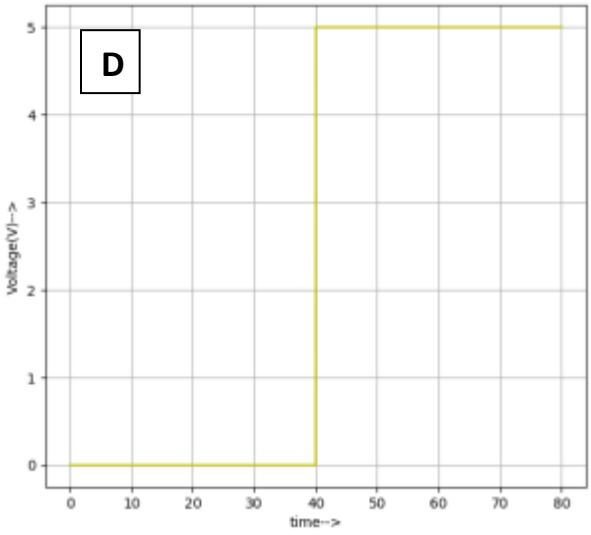


Python Plots :



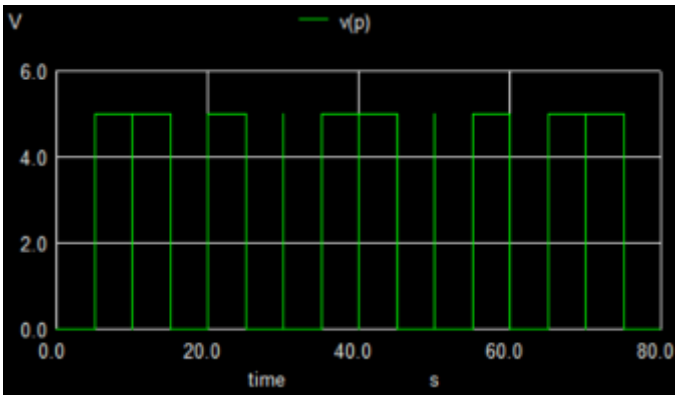


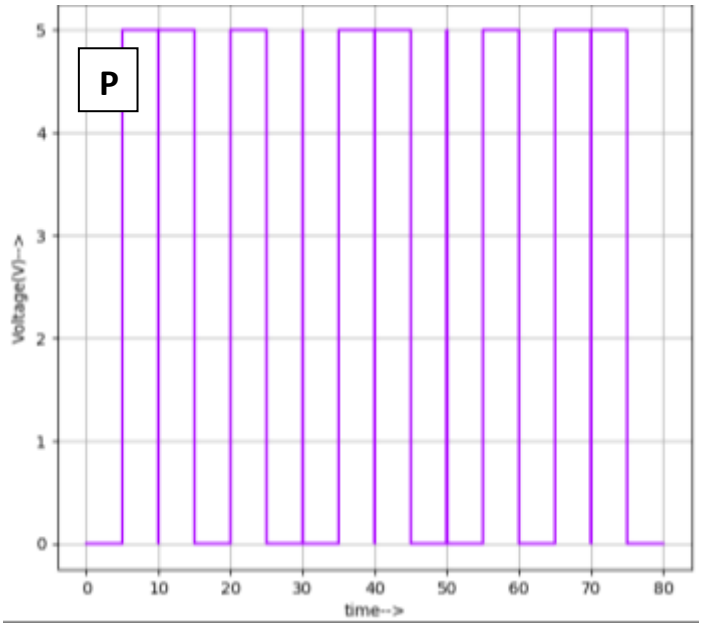




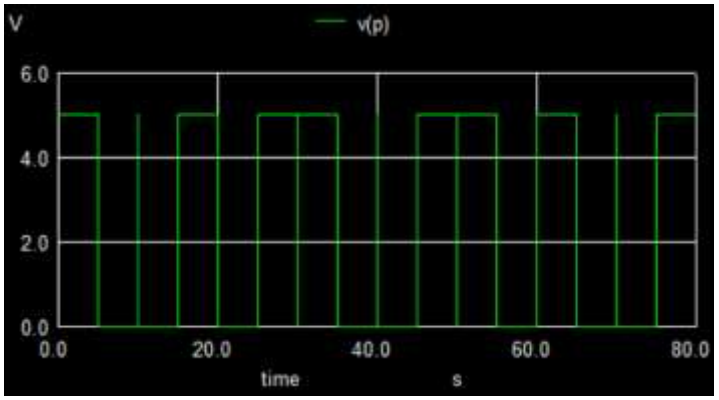
Output Waveforms :

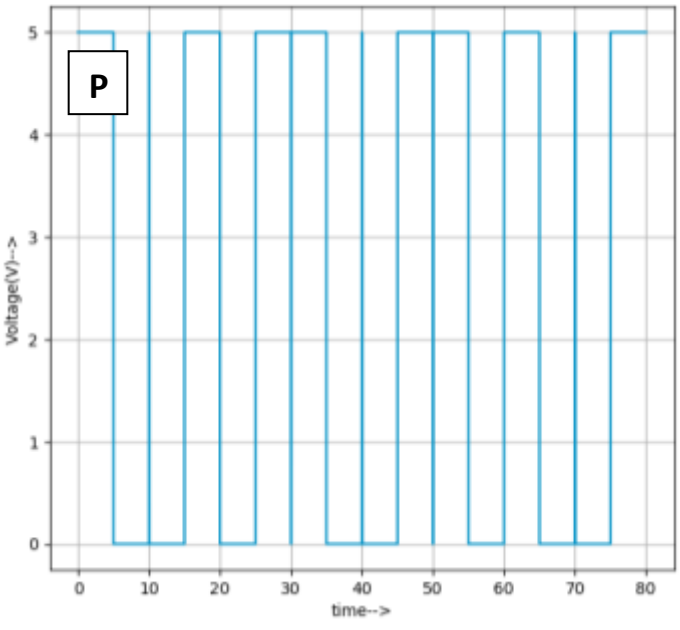
1) 4-bit Even parity :



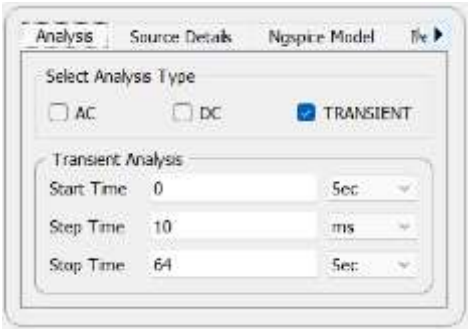


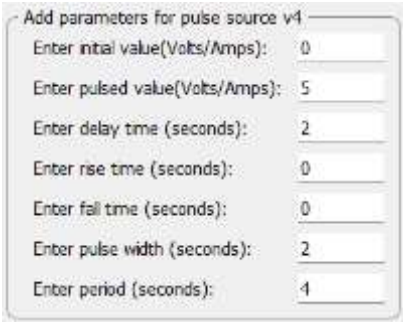
2) 4-bit Odd parity :

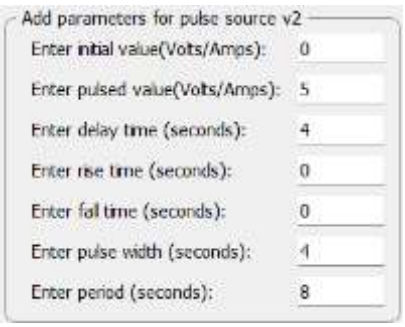


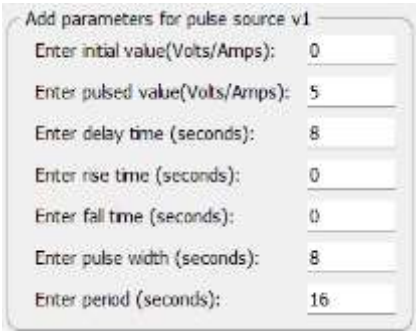


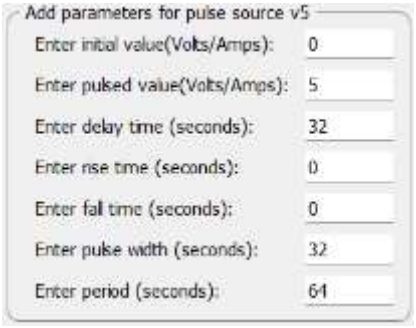
5-Bit Odd/Even Parity Checker :

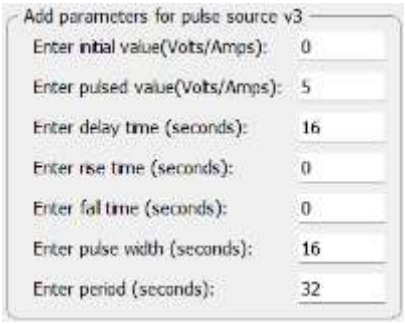




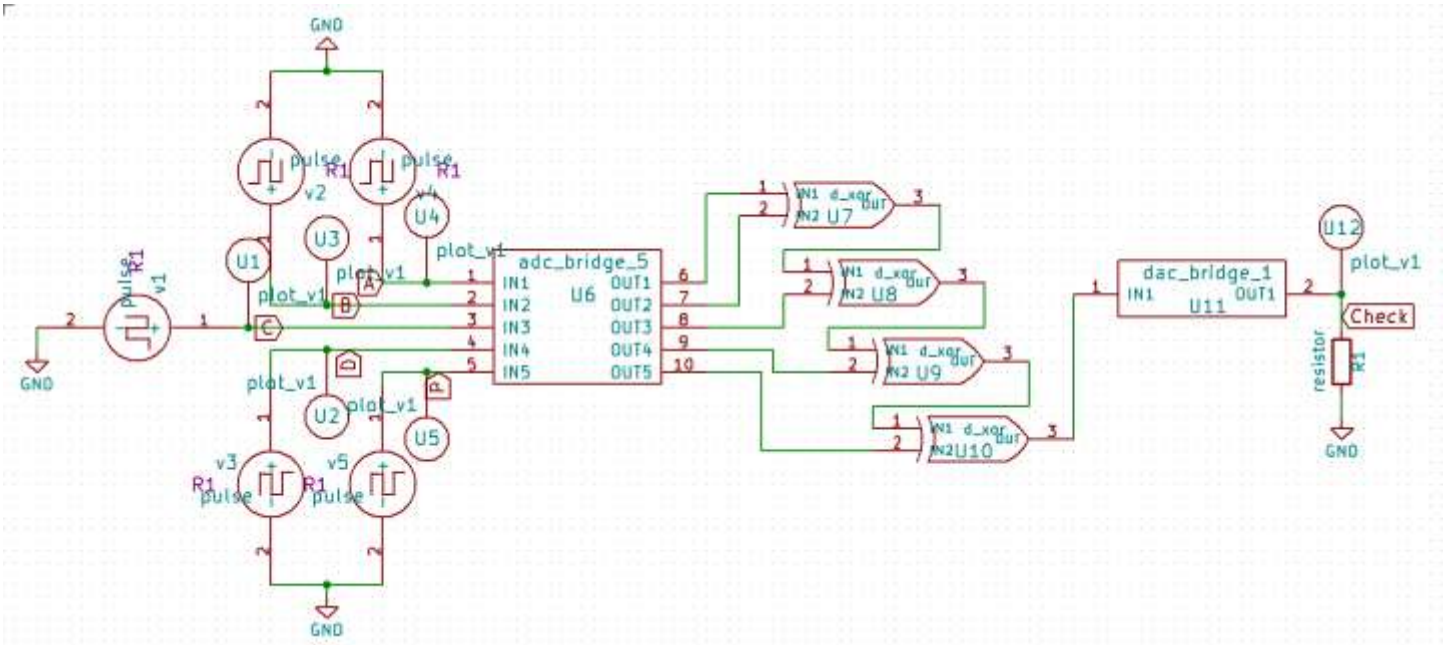




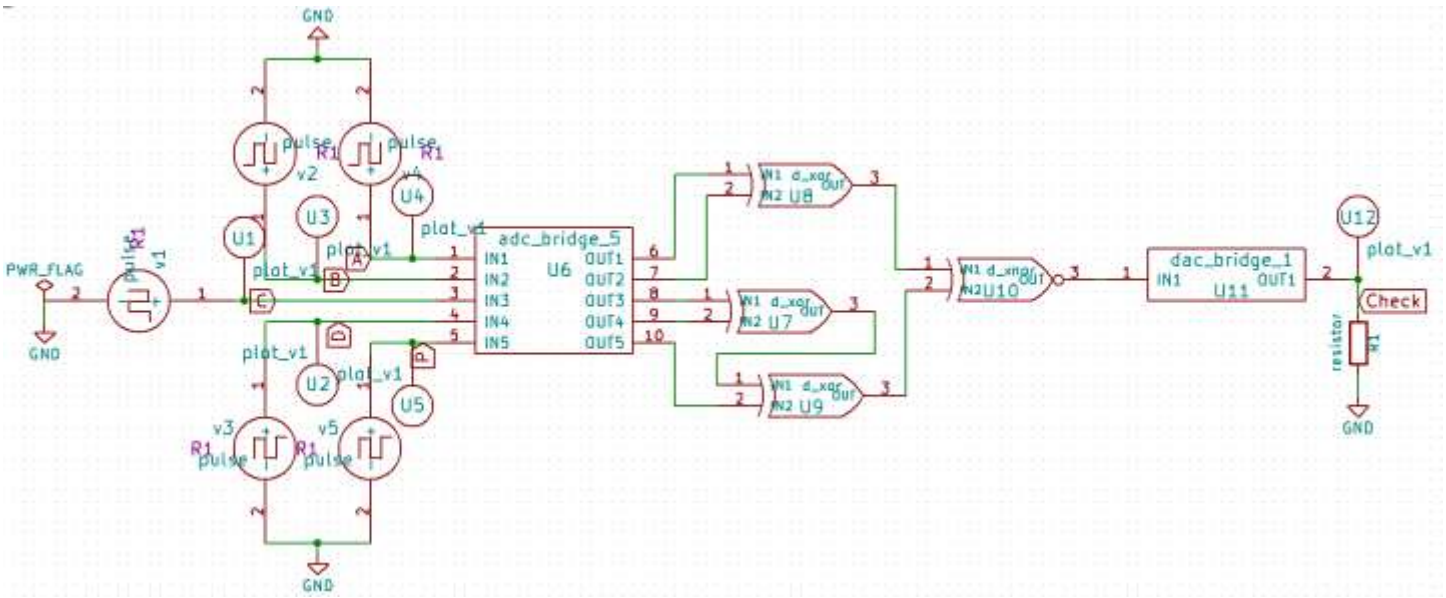




Even parity checker circuit :

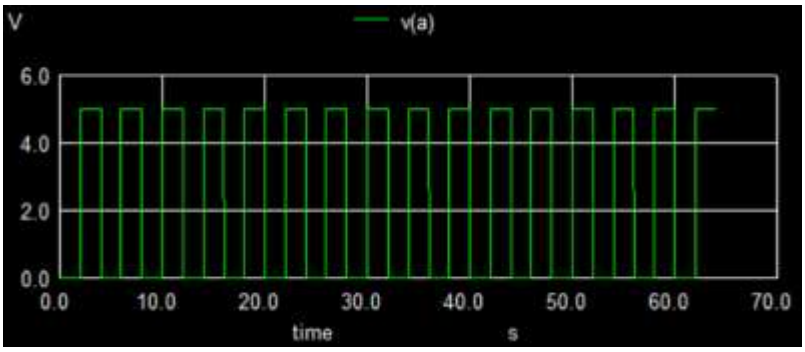


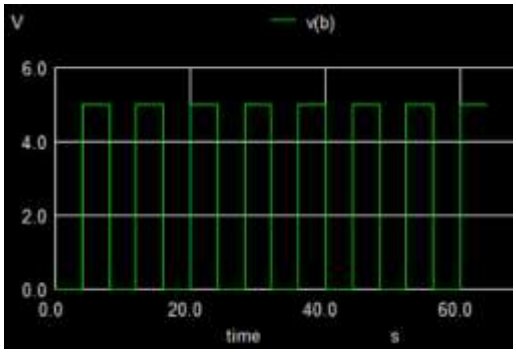
Odd parity checker circuit :

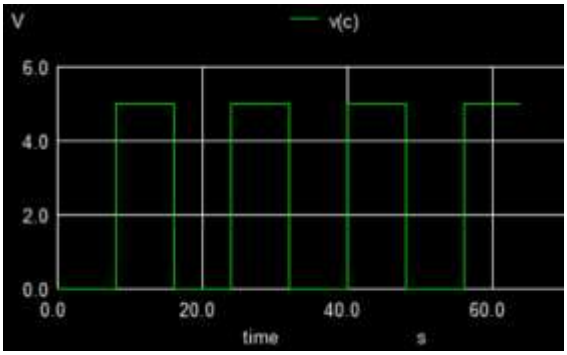


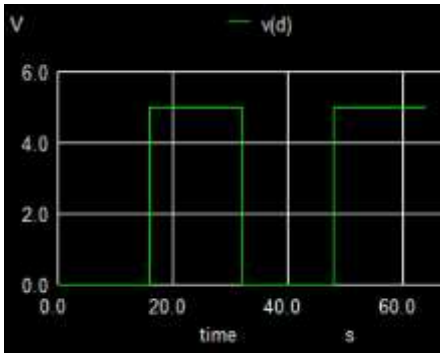
Input Waveforms :

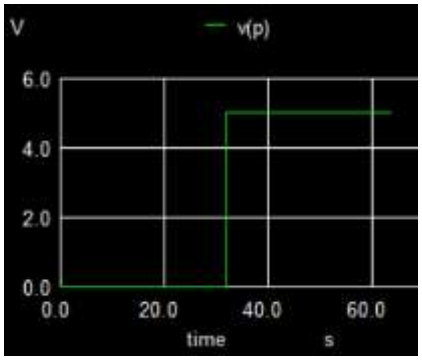
Ngspice Plots :



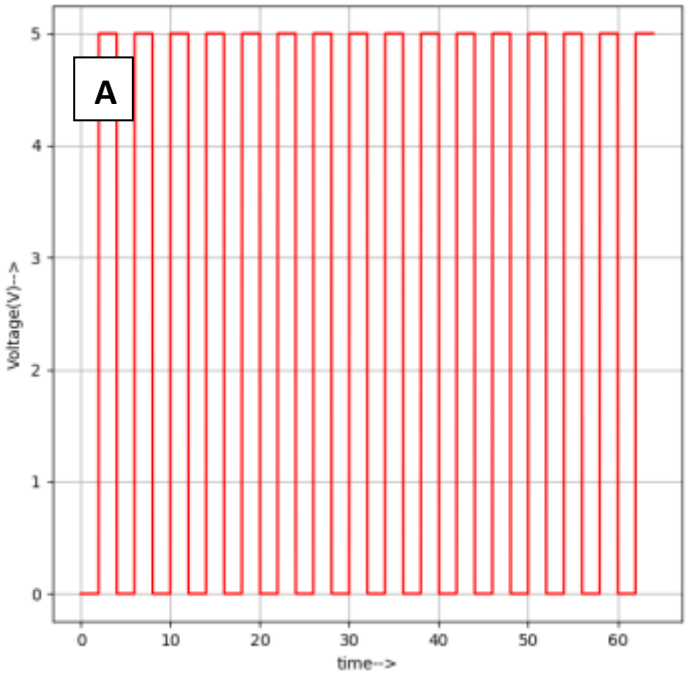


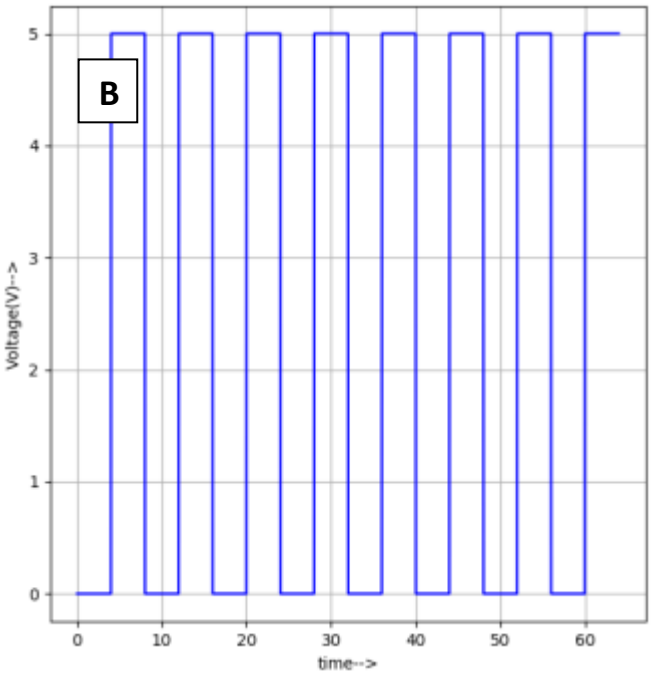


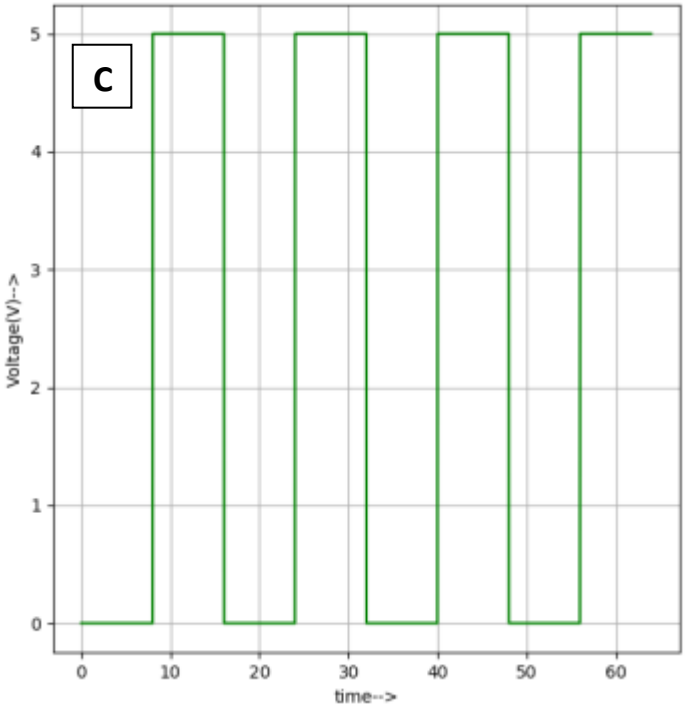


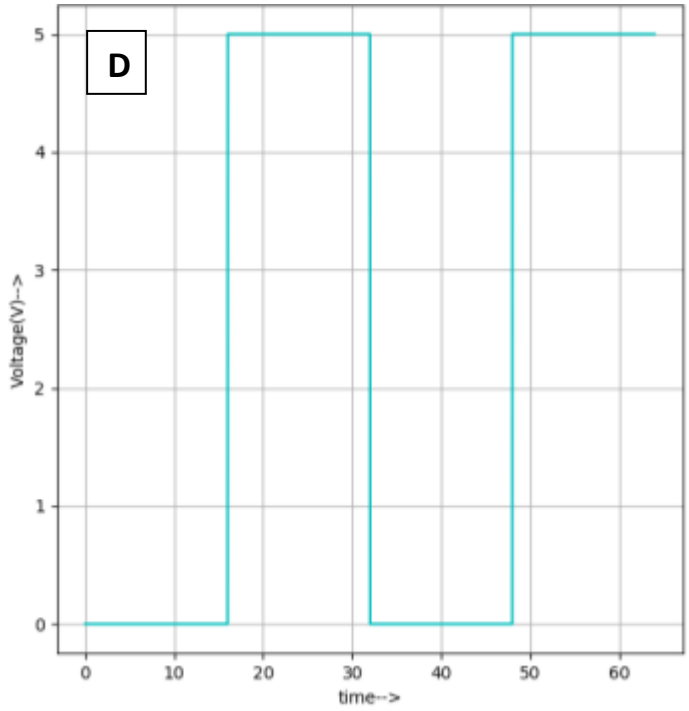


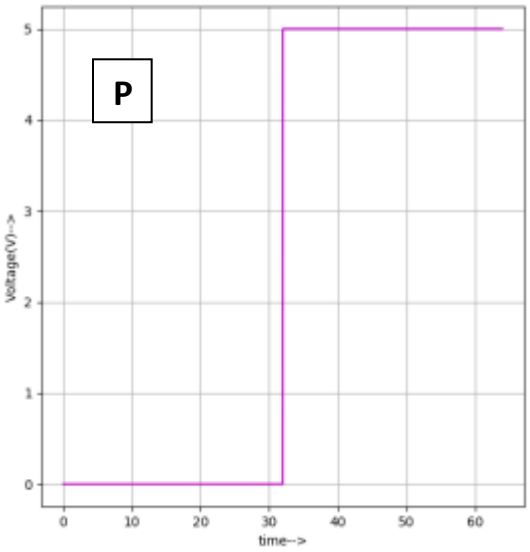
Python Plots :





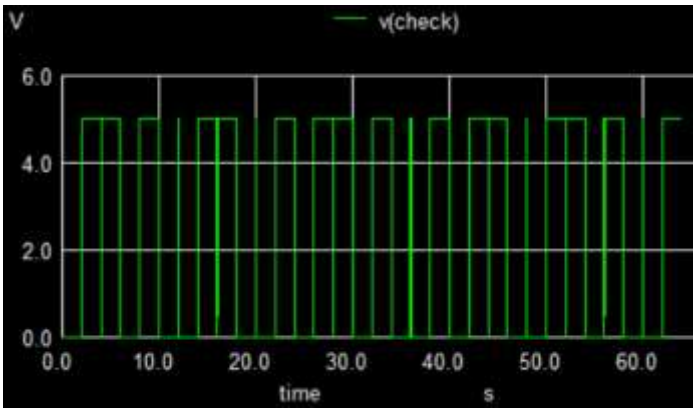


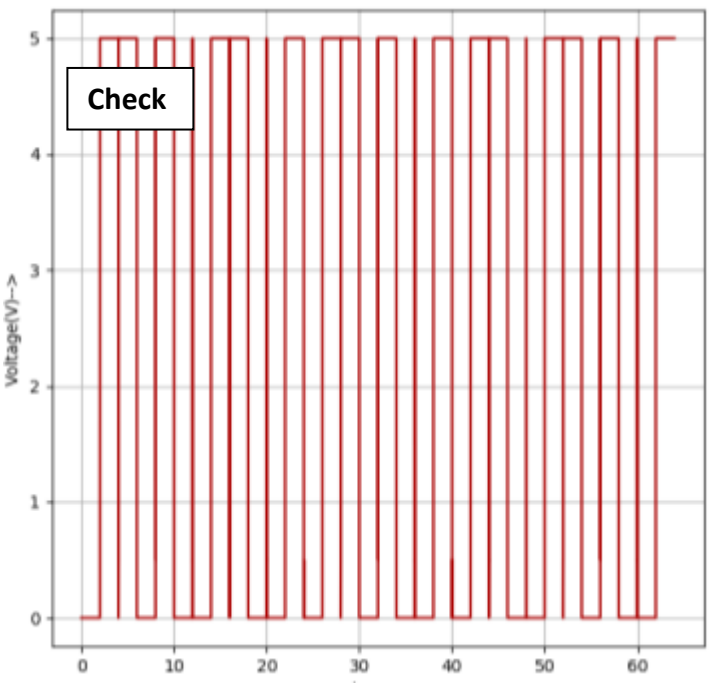




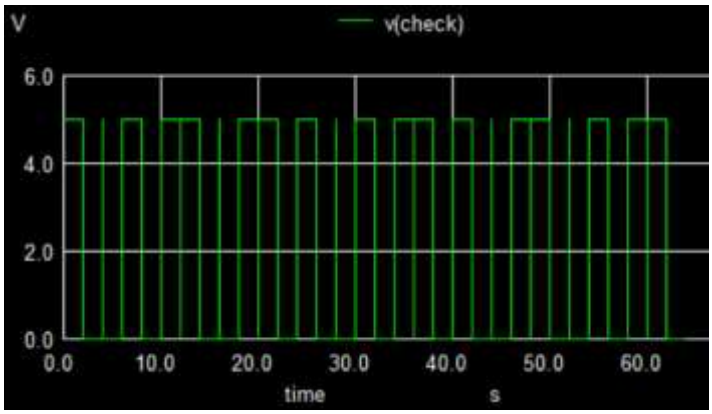
Output Waveforms :

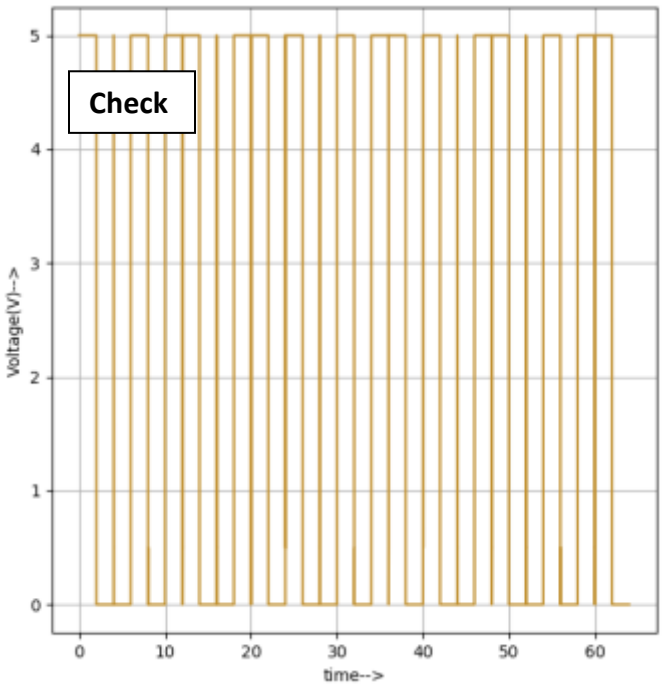
1) 5-bit Even parity checker :





2) 5-bit Odd parity checker :





Conclusion :

Therefore, the 4-bit parity generator and 5-bit parity checker are simulated and the results are verified successfully.

Sources / References :

4-bit parity generator circuit : https://technobyte.org/parity-generator-parity-checker/

5-bit checker parity circuit : https://www.coursehero.com/file/p9lchf/Table-6201-Five-bit-even-parity-checker-5-bit-Message-Parity-Error-A-B-C-D-P-PE/

K-map solver : https://www.charlie-coleman.com/experiments/kmap/