Circuit Simulation Project

https://esim.fossee.in/circuit-simulation-project

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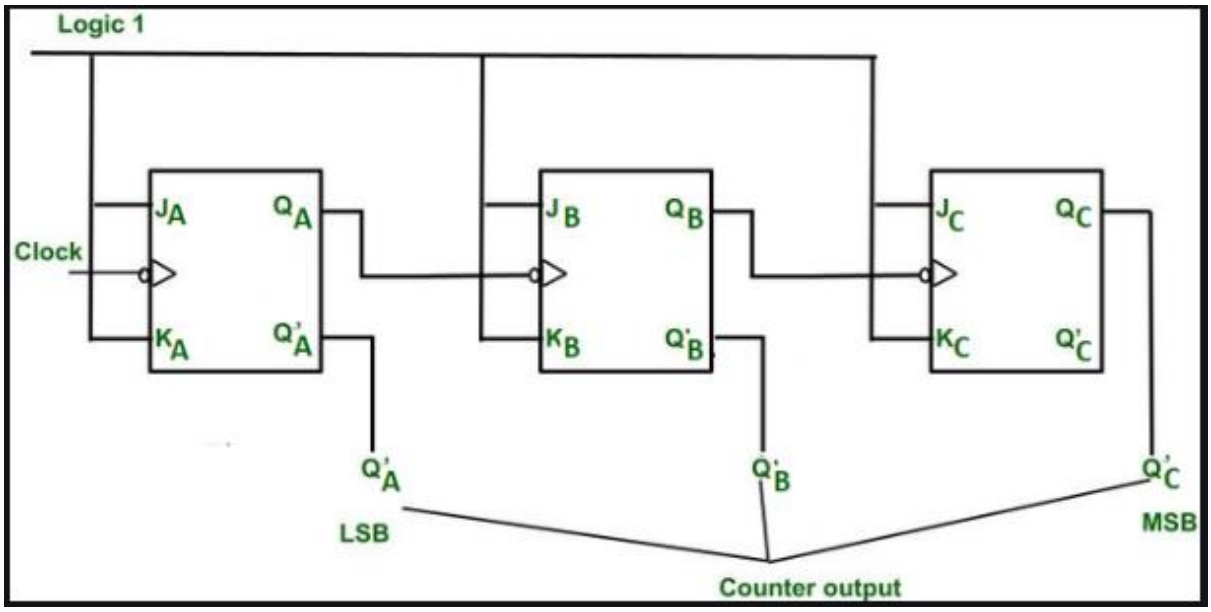
Project Guide: Dr R. Maheshwari

Title of the Circuit: 3-Bit Asynchronous Down Counter

Description:

Counters are used to count the clock pulses. The clock pulses occur at regular intervals. They are used to measure the time and frequency.
In an asynchronous counter, an external clock is provided only for the first flip flop, therefore output of the first flip flop acts as a clock pulse for the second flip flop and so on.
Asynchronous counters are also known as ripple counters and are formed by the successive combination of trailing edge-triggered flip-flops.
Asynchronous counters are those whose output is free from the clock signal. Because the flip flops in asynchronous counters are supplied with different clock signals, there may be delay in producing output.
These are used in applications where low power consumption is required. And are also used in frequency divider circuits, ring and Johnson counters.

CIRCUIT DIAGRAM:



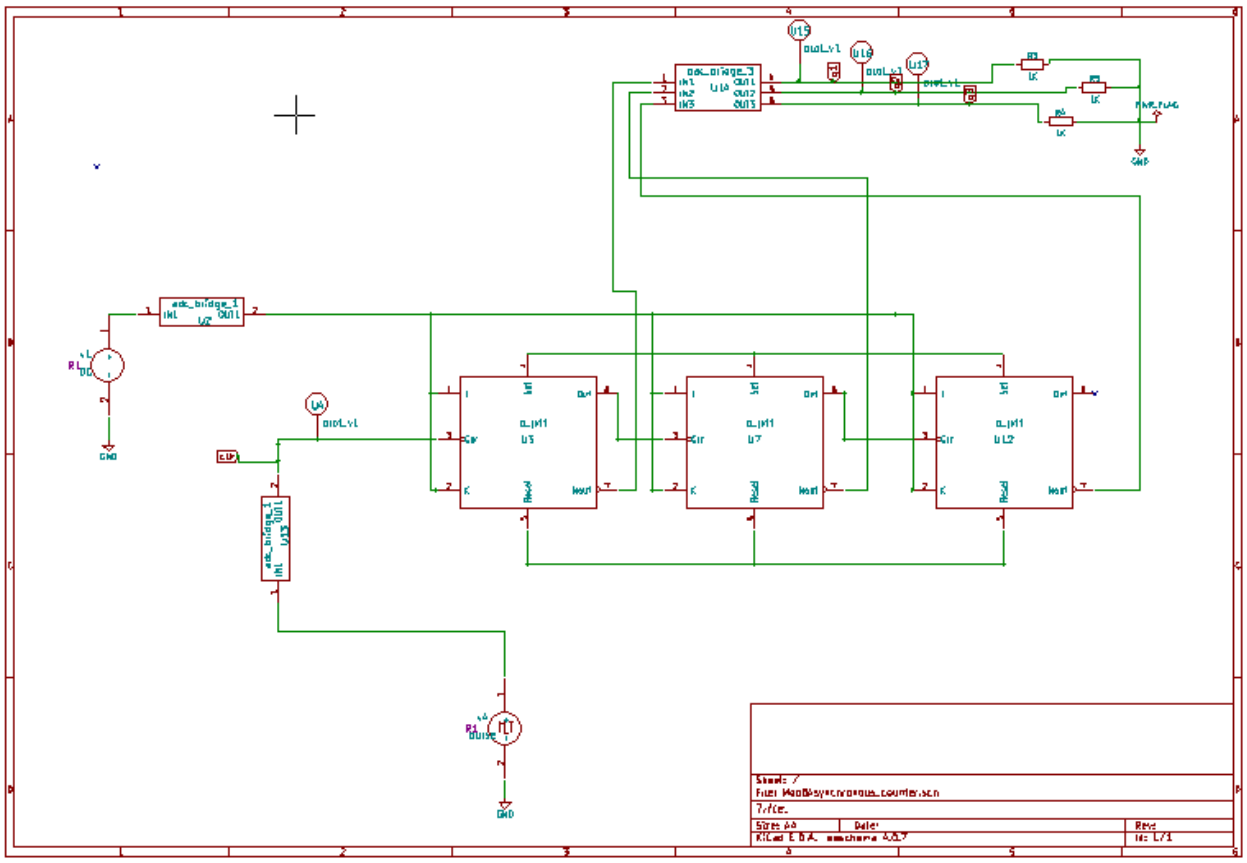
For a 3 bit asynchronous counter, 3 flip flops are required and 2^3=8 states can be generated.

In this implementation, the clock pulse is given to only the first flip flop. Therefore, the output of the first flip flop is fed as a clock to the second flip flop and the output of the second flip flop is fed as the clock for the third flip flop. But the complemented output is taken from each flip flop (i.e same as Up counter but output states are complemented). Here Q_a is LSB and Q_c is MSB.

TRUTH TABLE:

Clock	Q_C	Q_B	Q_A	Q'_C	Q'_B	Q'_A
Initially	0	0	0	1	1	1
1st	0	0	1	1	1	0
2nd	0	1	0	1	0	1
3rd	0	1	1	1	0	0
4th	1	0	0	0	1	1
5th	1	0	1	0	1	0
6th	1	1	0	0	0	1
7th	1	1	1	0	0	0

e-Sim Schematic

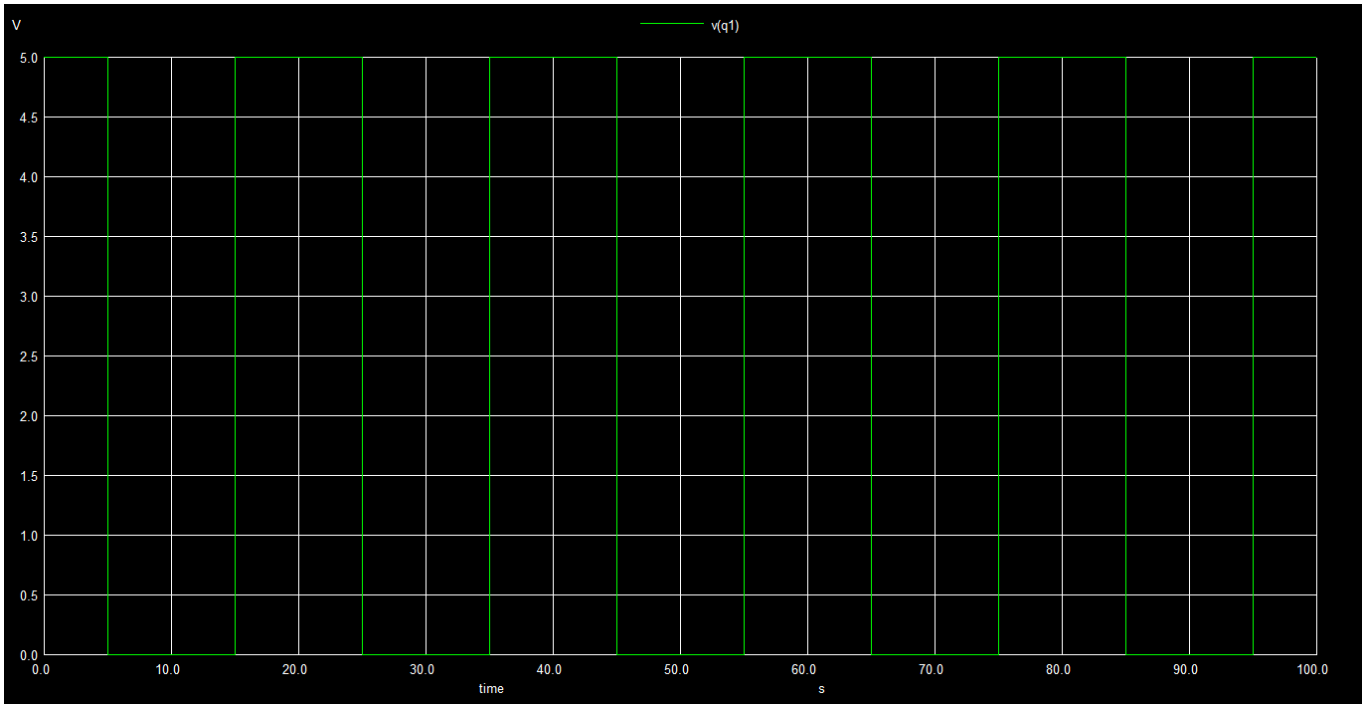


In this circuit, Q_1 represents LSB and Q_3 represents MSB.

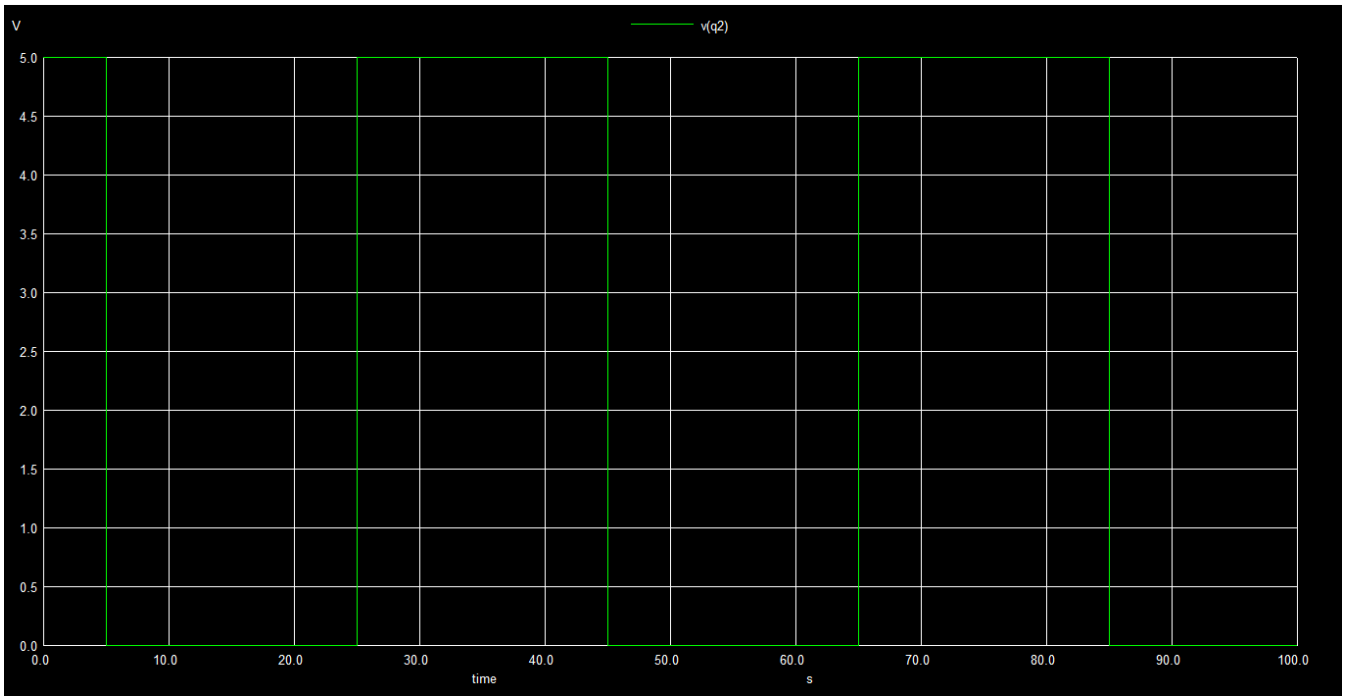
Simulation Results:

1. NG Spice Waveforms:

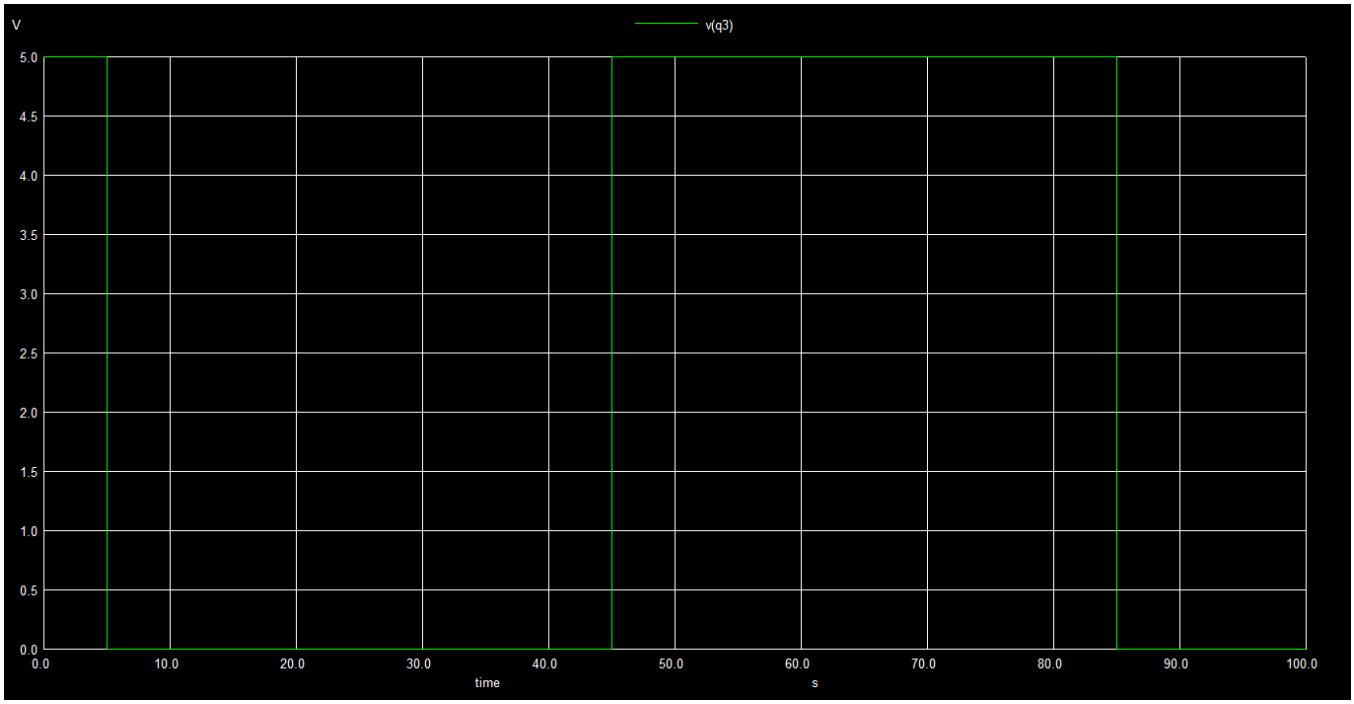
Q_1' (LSB):


V
v(q1)
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
time
s

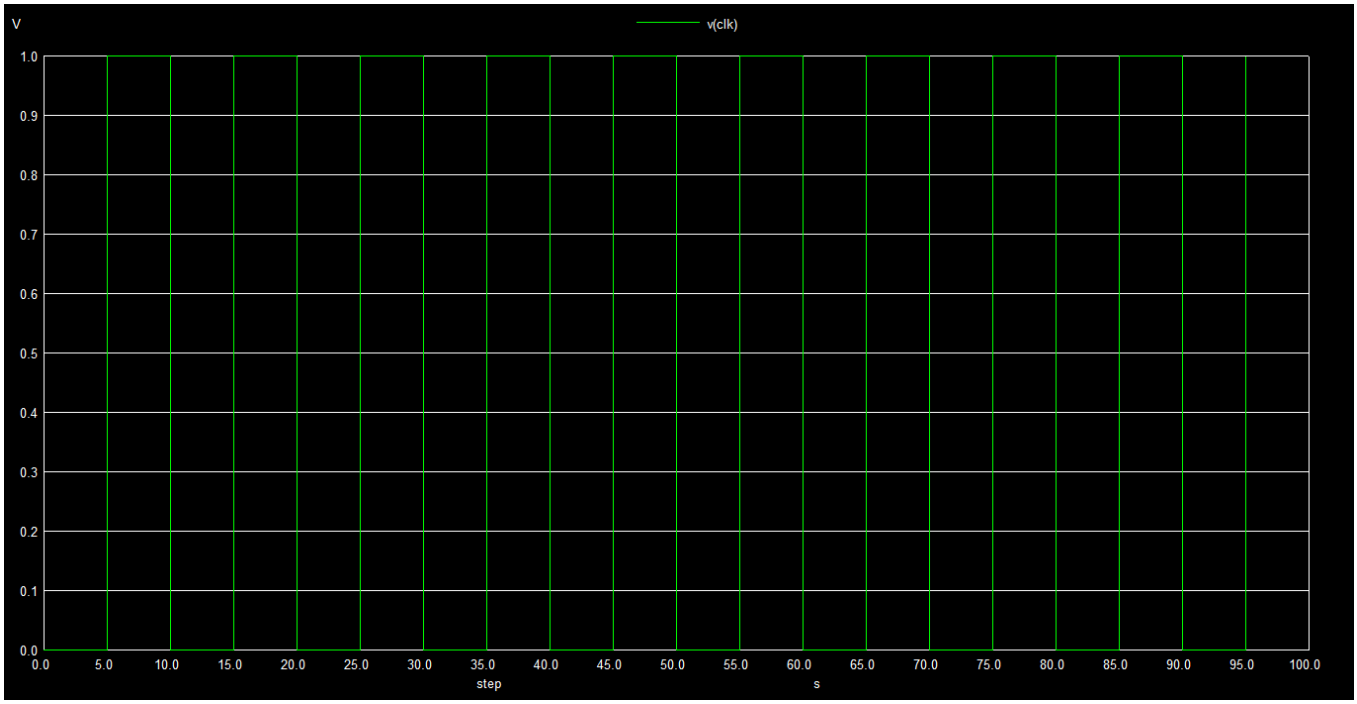
Q_2':


V
v(q2)
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
time
s

Q_3' (MSB)

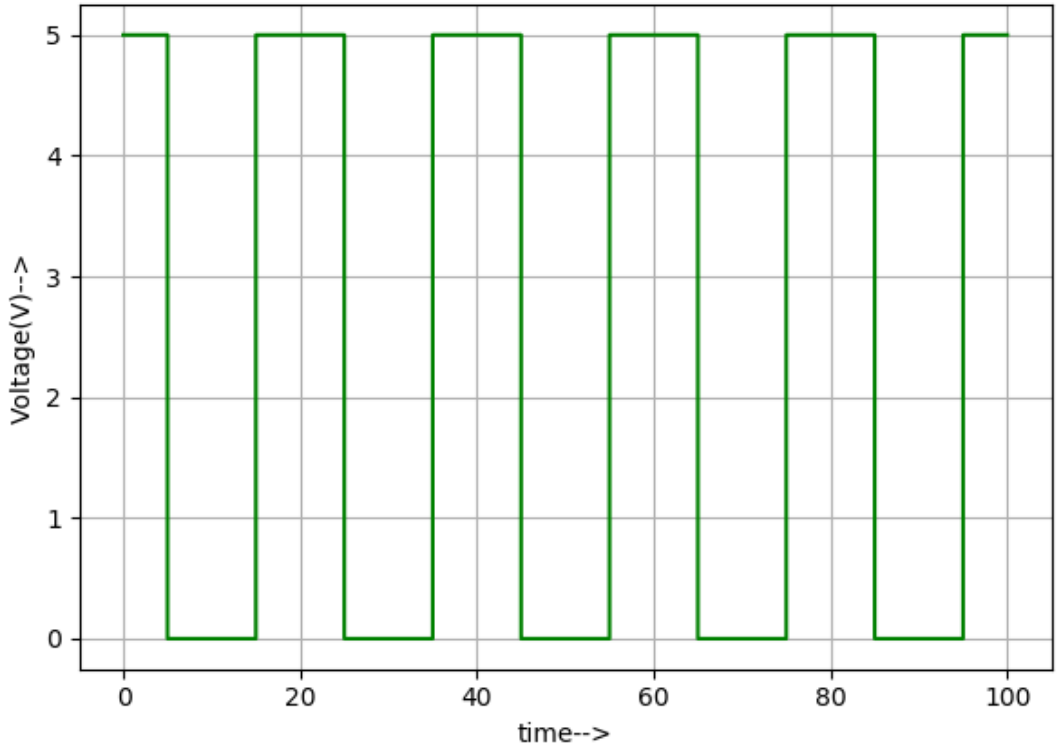


Clk (Clock pulse):

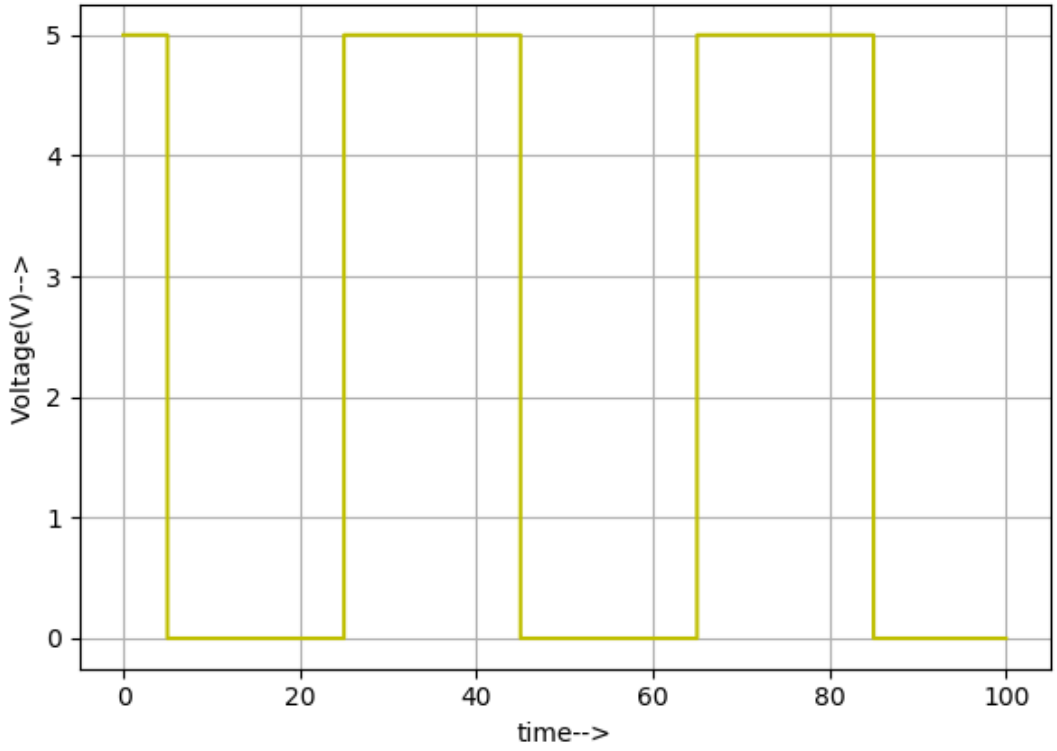


2. Python Waveforms:

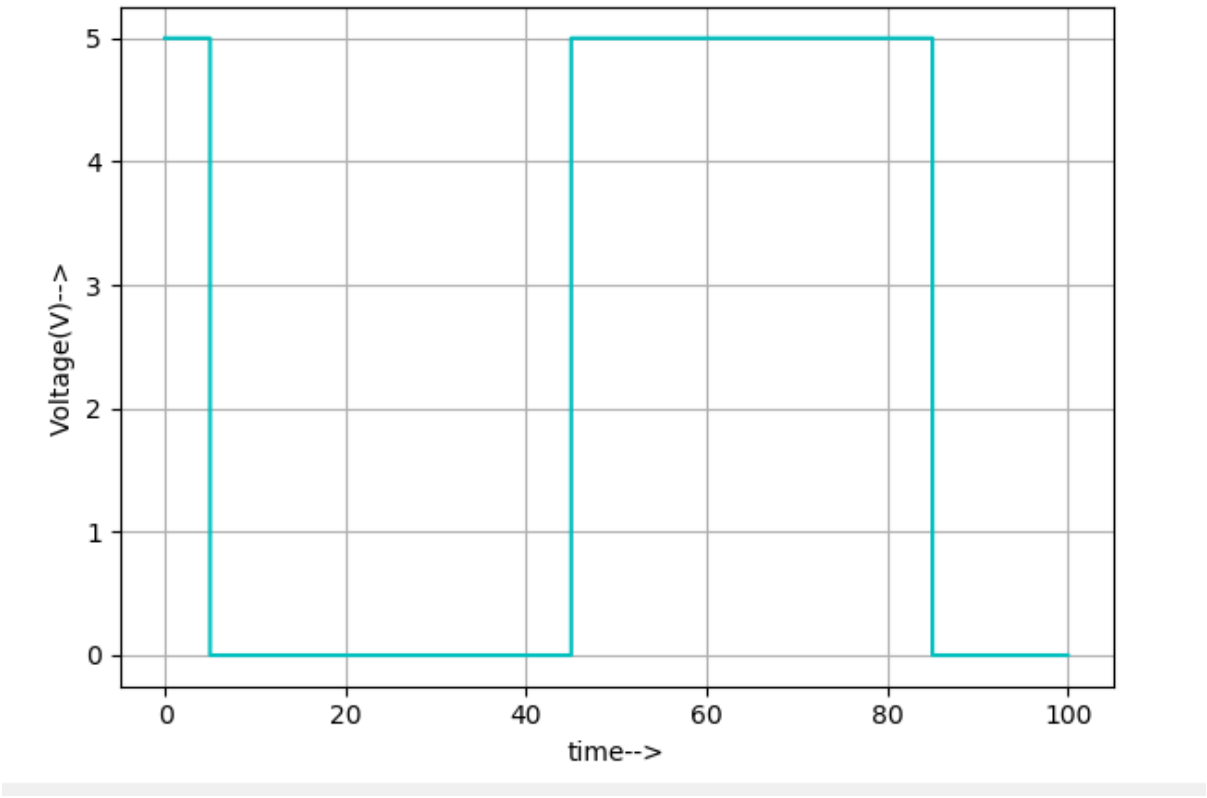
Q_1' (LSB):



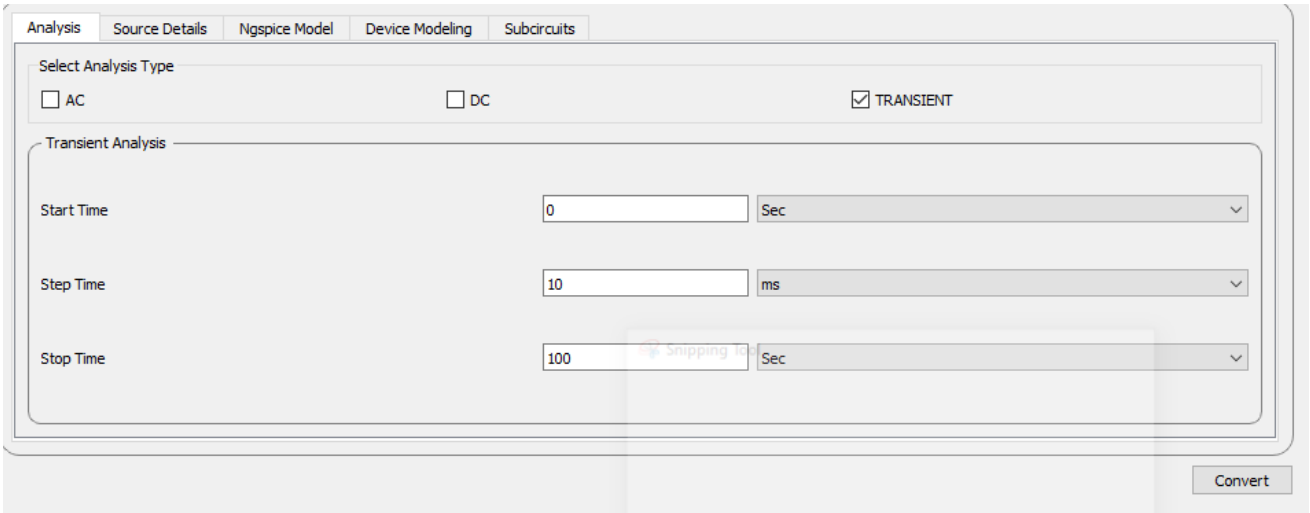
Q_2':



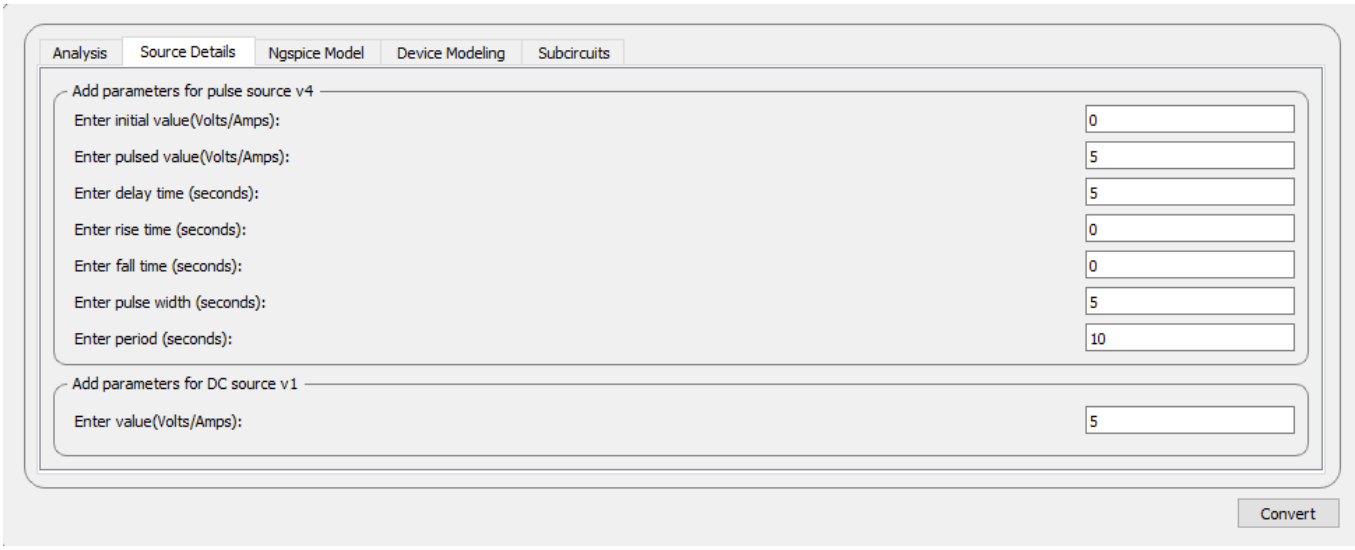
Q_3' (MSB):



Transient Analysis:



Source Details:



Conclusion:

Thus, 3-bit asynchronous down counter was designed and verified using JK flipflops on esim.

References:

https://www.geeksforgeeks.org/asynchronous-down-counter/

https://www.electronicshub.org/asynchronous-counter/

https://electronicscoach.com/asynchronous-counter.html