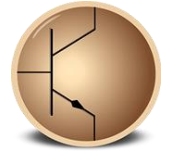




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Circuit Simulation Project

<https://esim.fossee.in/circuit-simulation-project>

Name of the participant: Rishi Nair

Project guide: Dr. Maheswari. R

Title of the circuit: 3 Bit Synchronous UP Counter Using JK Flip Flops

Theory/Description:

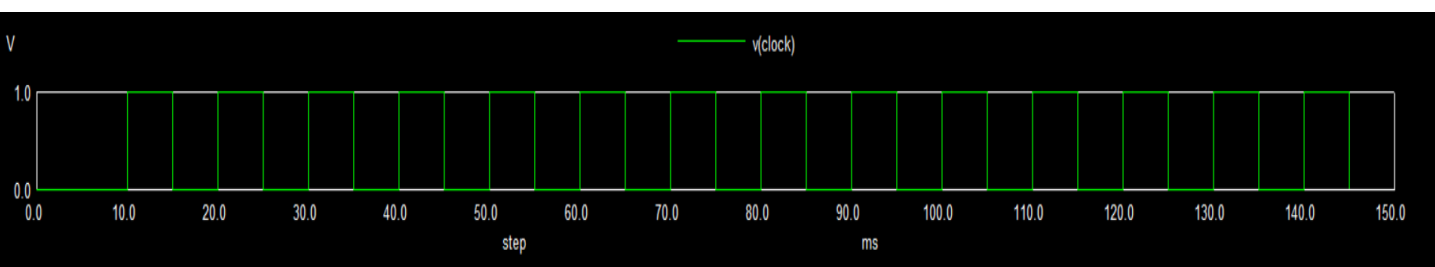
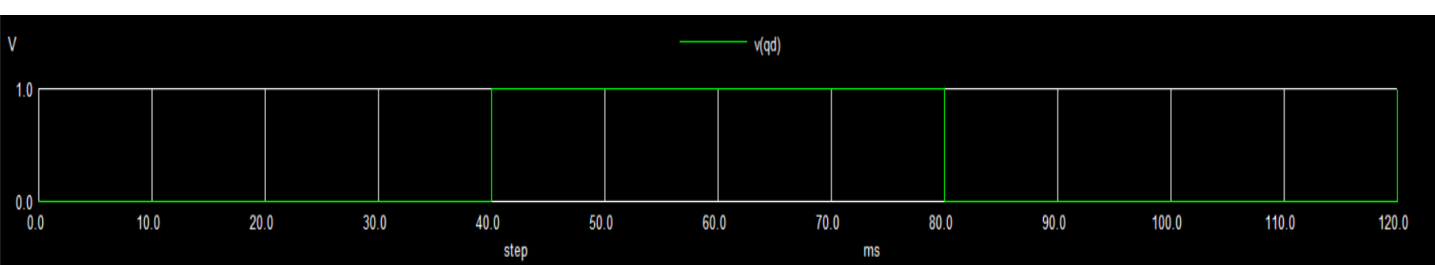
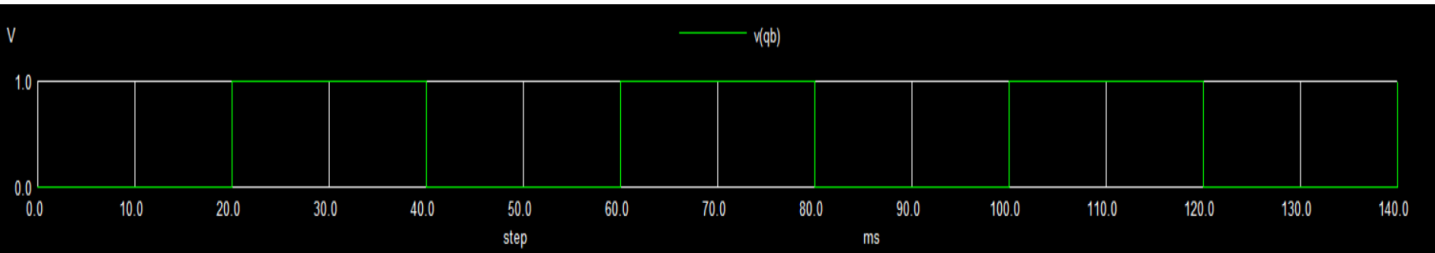
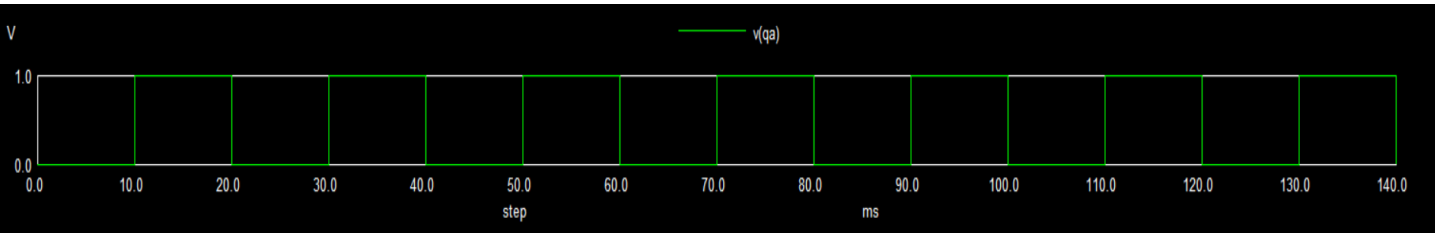
A counter is a sequential circuit that goes through a prescribed sequence of states upon the application of input pulses. The input pulses called count pulses, may be clock pulses, or they may originate from an external source and may occur at prescribed intervals of time or at random.

Synchronous counters are designed in such a way that the clock pulses are applied to the CP inputs of all the flip-flops. The common pulse triggers all the flip-flops simultaneously, rather than one at a time in succession.

In the 3-bit synchronous counter, we have used three j-k flip-flops. As in the diagram

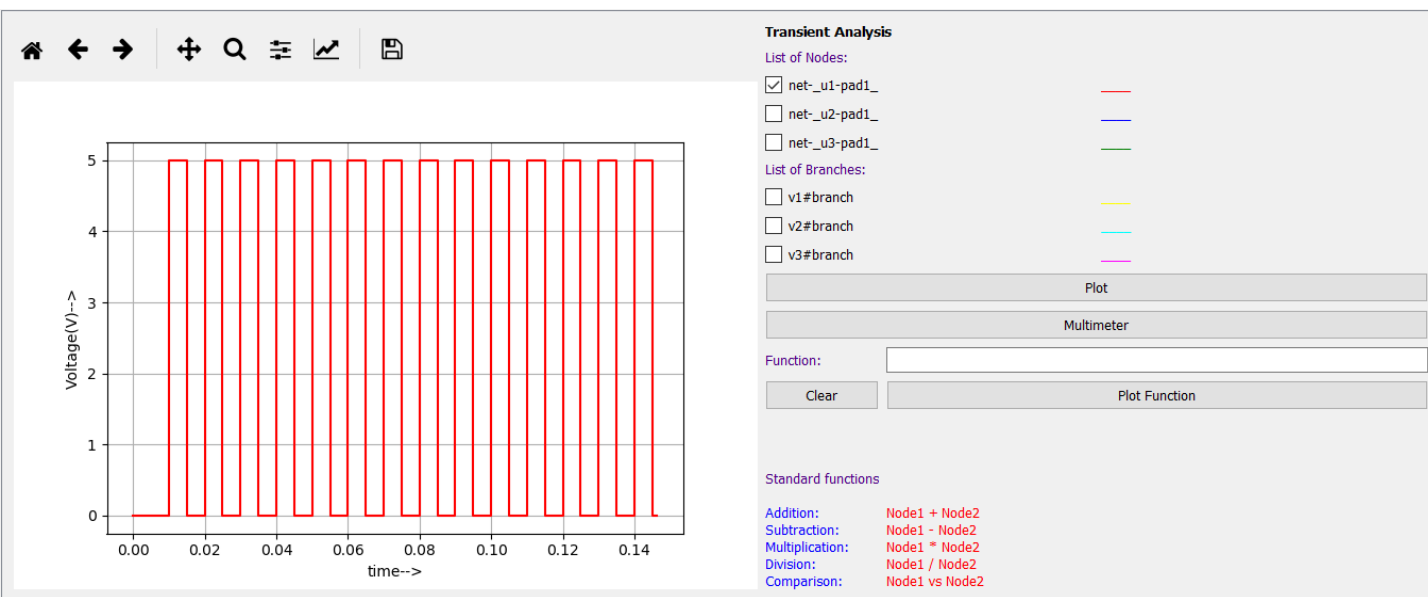
Circuit Diagram:

Output (Ngspice):



Clock

Output (Python):



Clock Signal

References:

https://www.iitg.ac.in/cseweb/vlab/Digital-System-Lab/up_counter.php?id=13