Circuit Simulation Project

https://esim.fossee.in/circuit-simulation-project

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Project Guide: Dr. Maheswari. R

Title of the project:

Design of a 4 to 16 Decoder using 3 to 8 Decoders

Theory/Description:

A **binary decoder** is a combinational logic circuit that converts binary information from the n coded inputs to a maximum of 2^n unique outputs. They are used in a wide variety of applications, including instruction decoding, data multiplexing and data demultiplexing, seven segment displays etc.

A 3 to 8 decoder consists of 3 inputs, an enable and 8 outputs each of which represents a minterm. If the enable is high, then the decoder is enabled. Otherwise, the decoder is disabled.

If A, B, C are the inputs then the equations of the outputs of a 3 to 8 decoder are:

D0 = A'B'C'

D1 = A'B'C

D2 = A'BC'

D3 = A'BC

D4 = AB'C'

D5 = AB'C

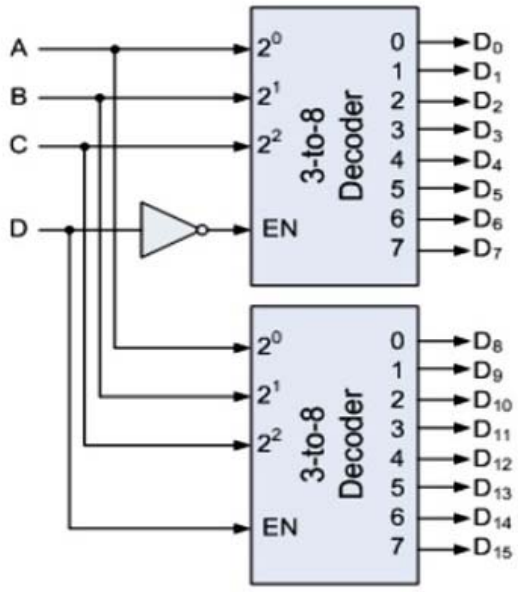
D6 = ABC'

D7 = ABC

where A', B' and C' represents the complement of A, B and C respectively.

Two 3 to 8 decoders can be used to implement a 4 to 16 decoder (4 inputs and 16 outputs).

Circuit diagram of a 4 to 16 decoder using 3 to 8 decoders is as follows:



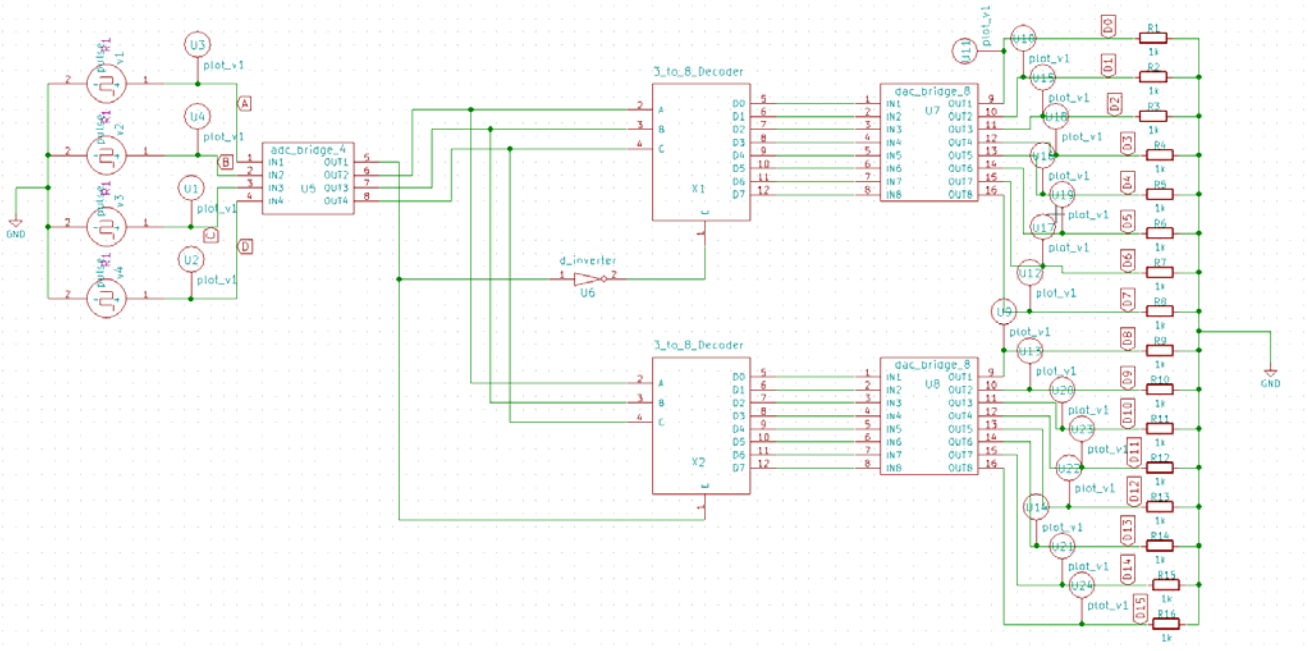
Here A, B, C and D are the inputs and D0-D15 are the outputs.

Truth table of a 4 to 16 Decoder:

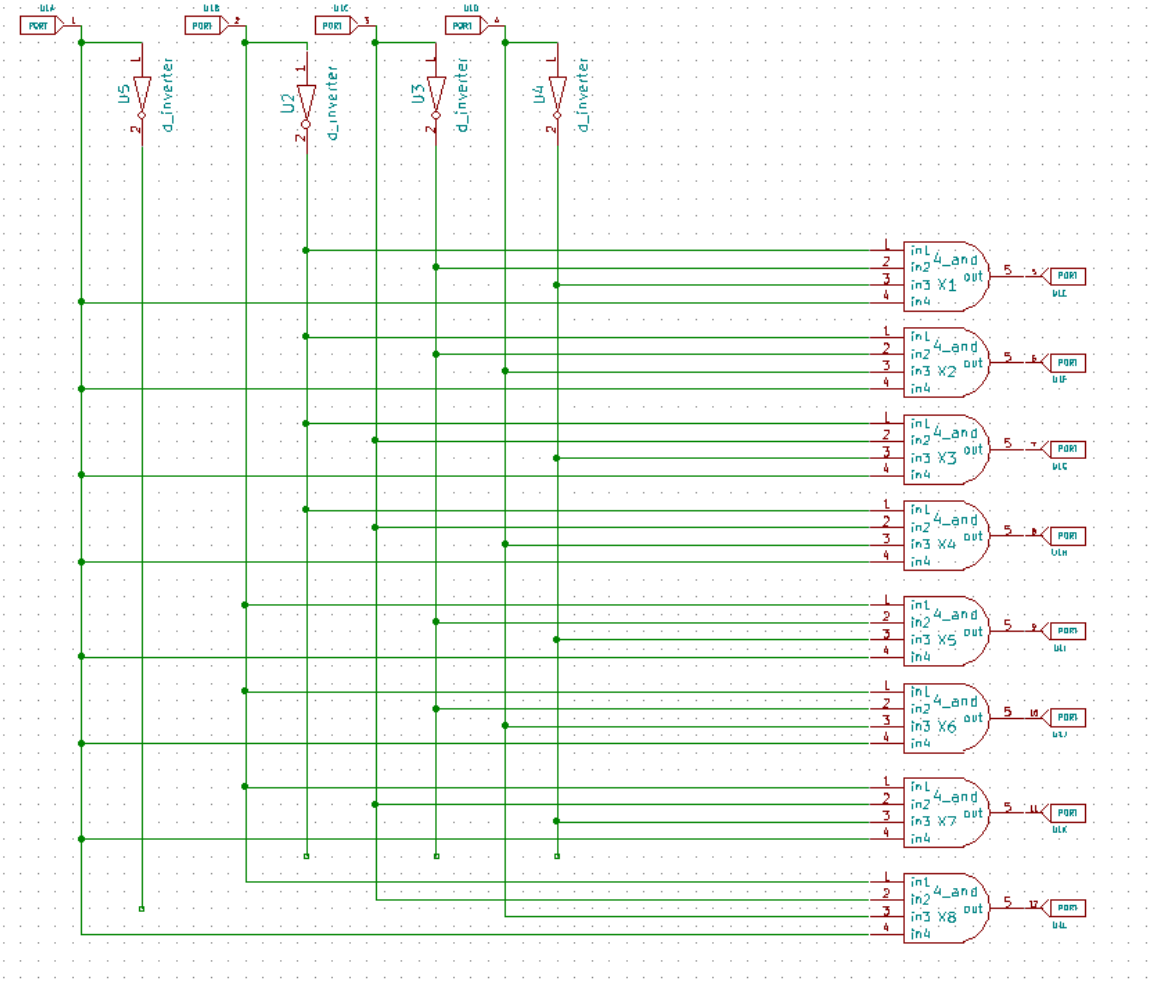
A	B	C	D	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Circuit Diagrams using eSim:

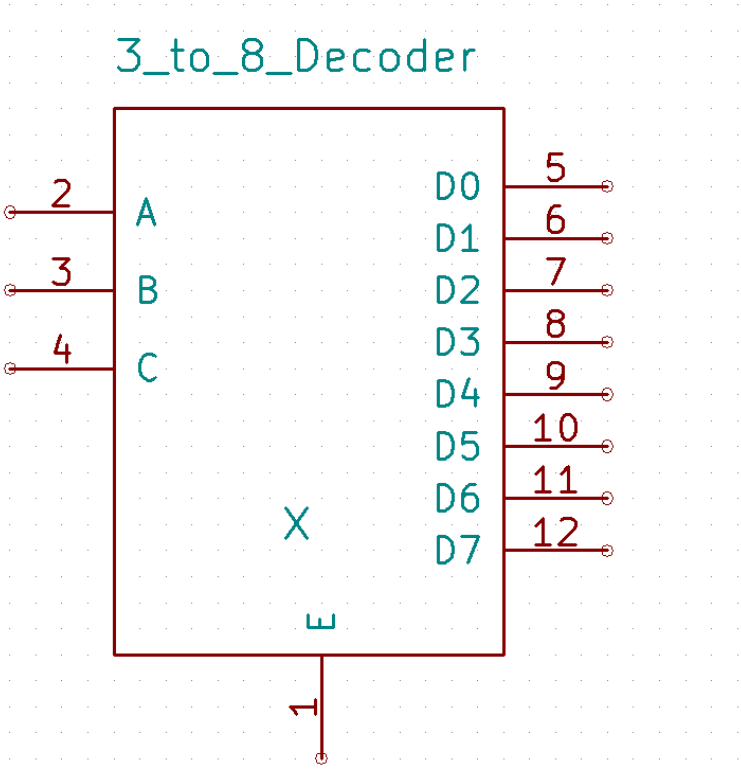
- Main functional circuit diagram of a 4 to 16 decoder which uses 3 to 8 decoders:



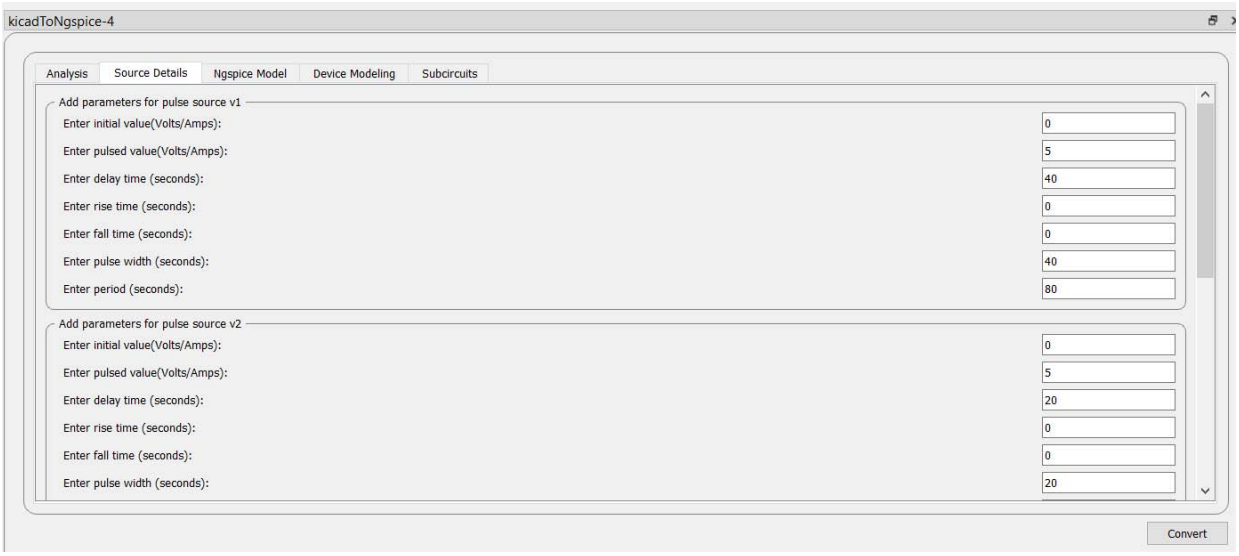
- The circuit diagram of a 3 to 8 decoder which is used as a subcircuit:

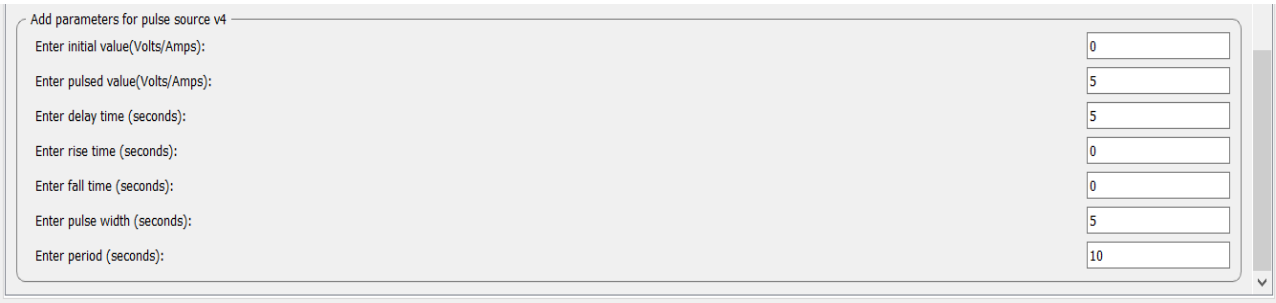


- Symbol designed to represent 3 to 8 decoder:

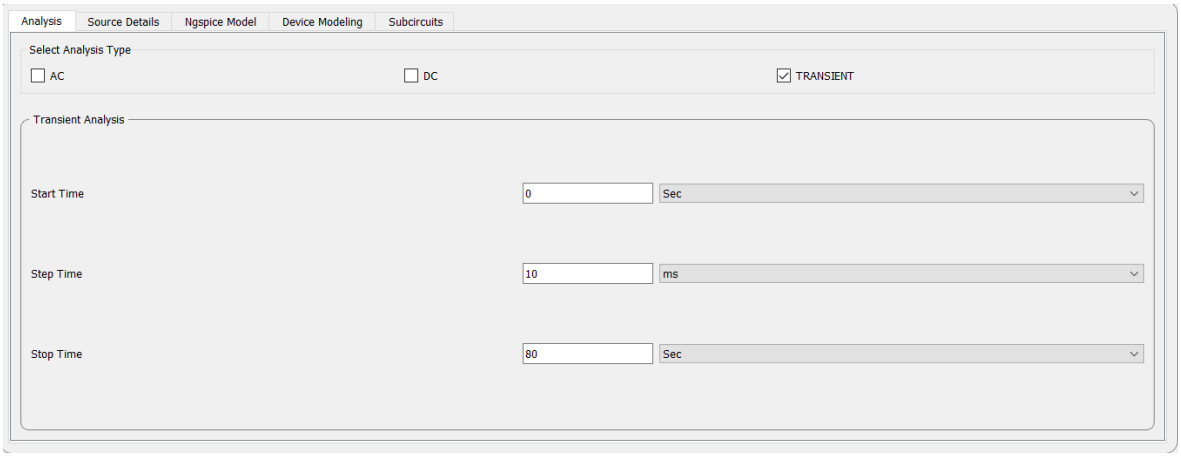


Source details:





Analysis:

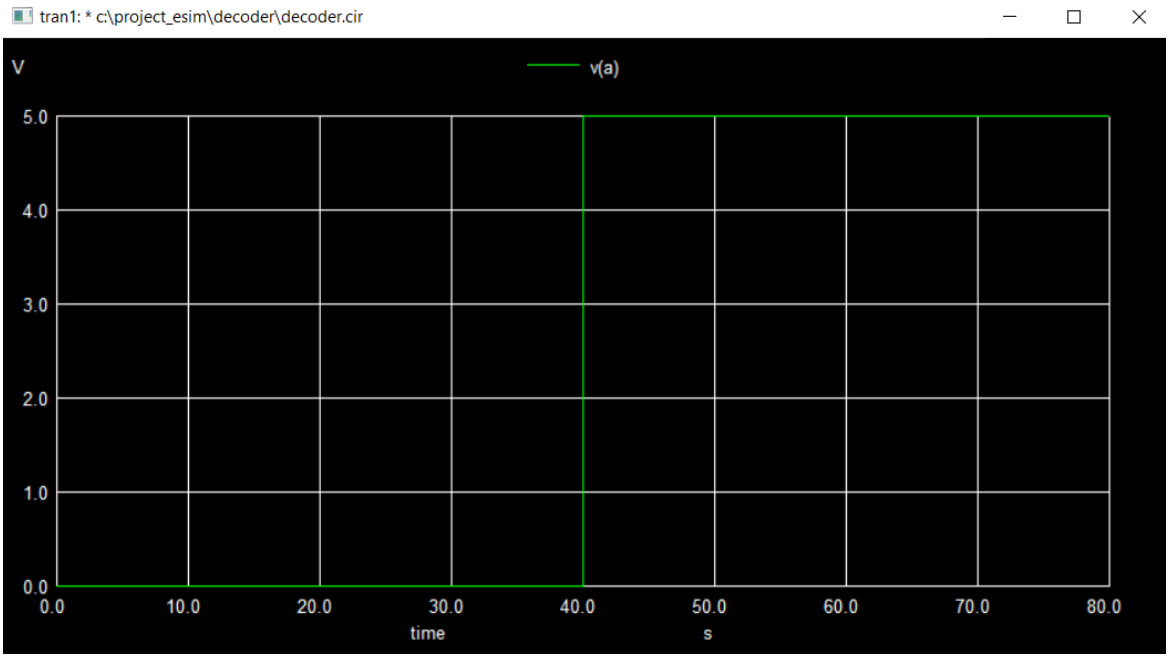

Analysis
Source Details
Ngspice Model
Device Modeling
Subcircuits
Select Analysis Type
AC
DC
TRANSIENT
Transient Analysis
Start Time
0
Sec
Step Time
10
ms
Stop Time
80
Sec

Results

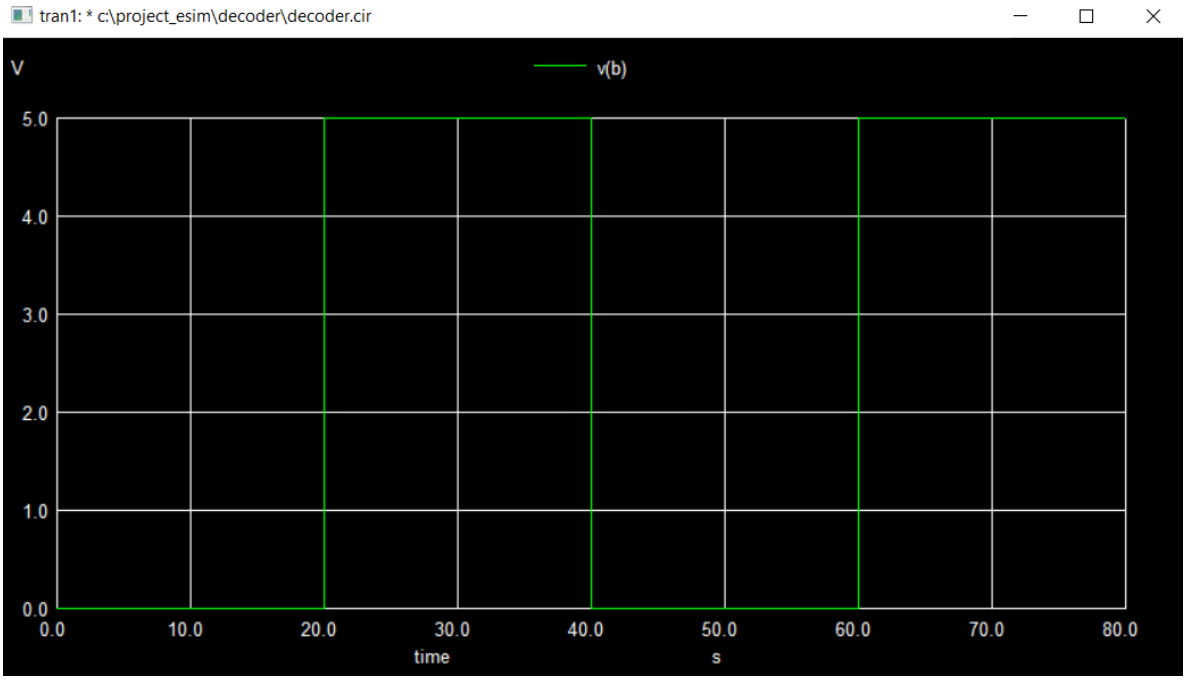
Ngspice plots:

Input waveforms:

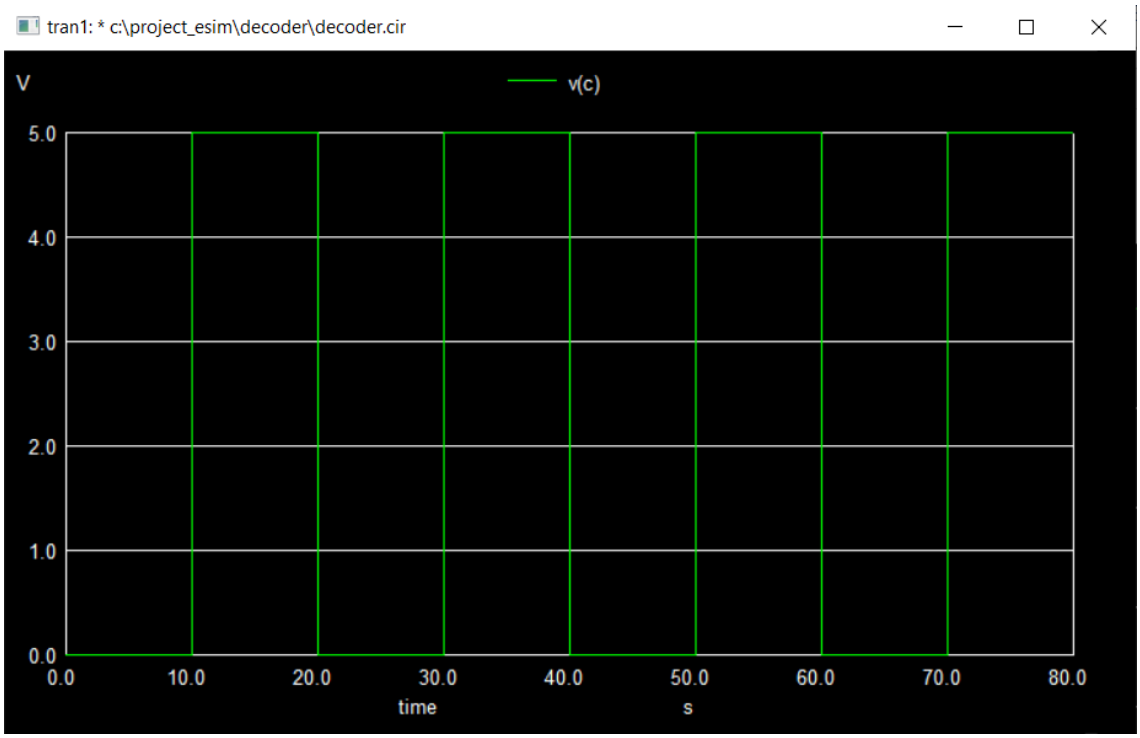
- **A**



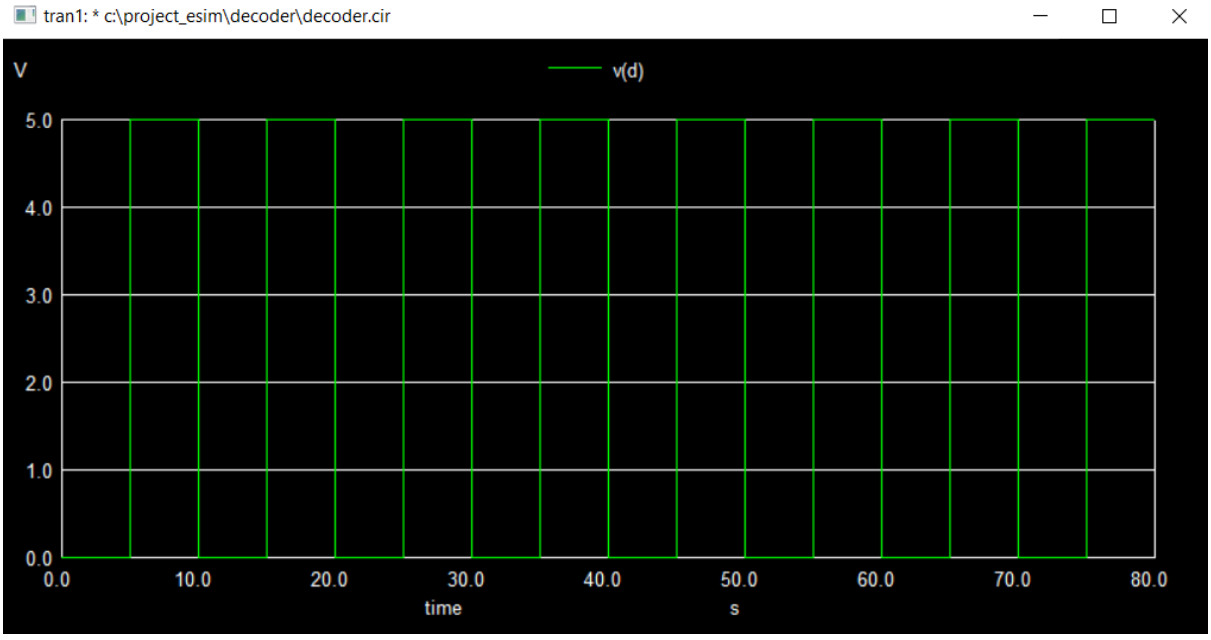
- **B**



- **C**

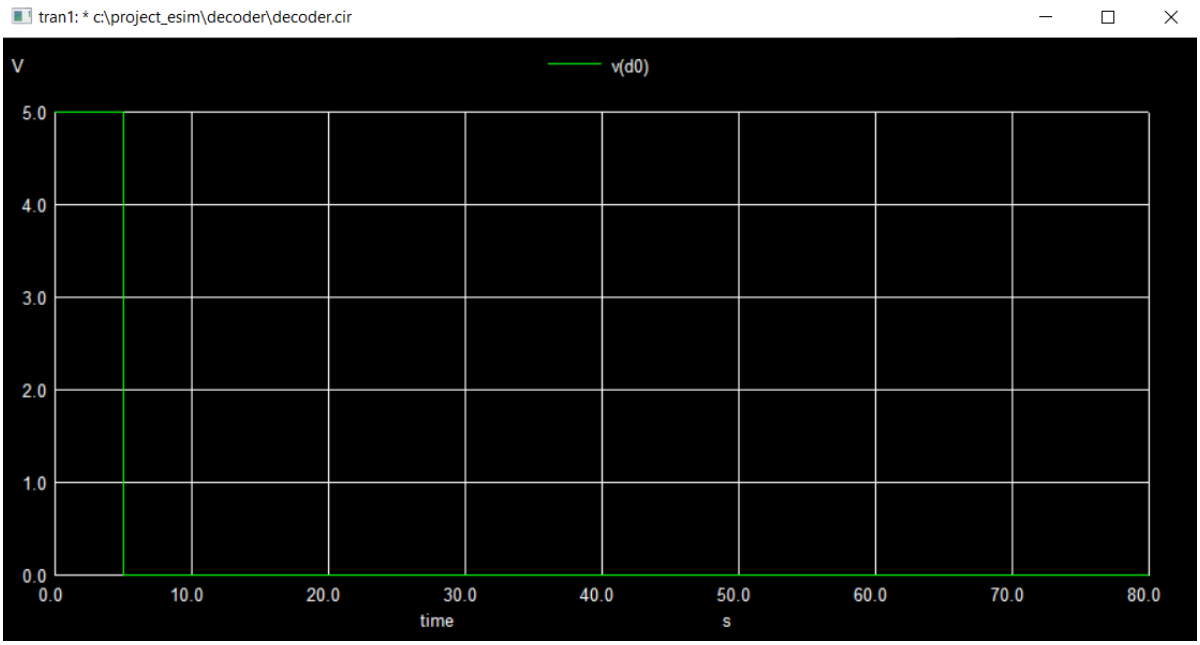

tran1: * c:\project_esim\decoder\decoder.cir
V
v(c)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
time
s

- **D**

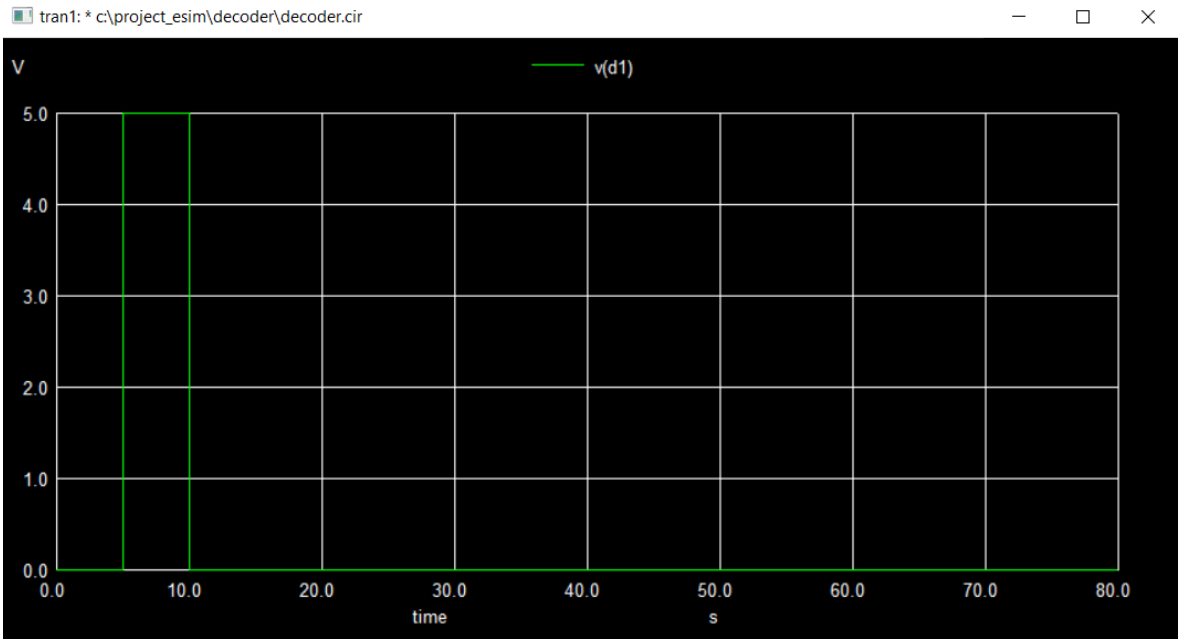

tran1: * c:\project_esim\decoder\decoder.cir
V
v(d)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
time
s

Output waveforms:

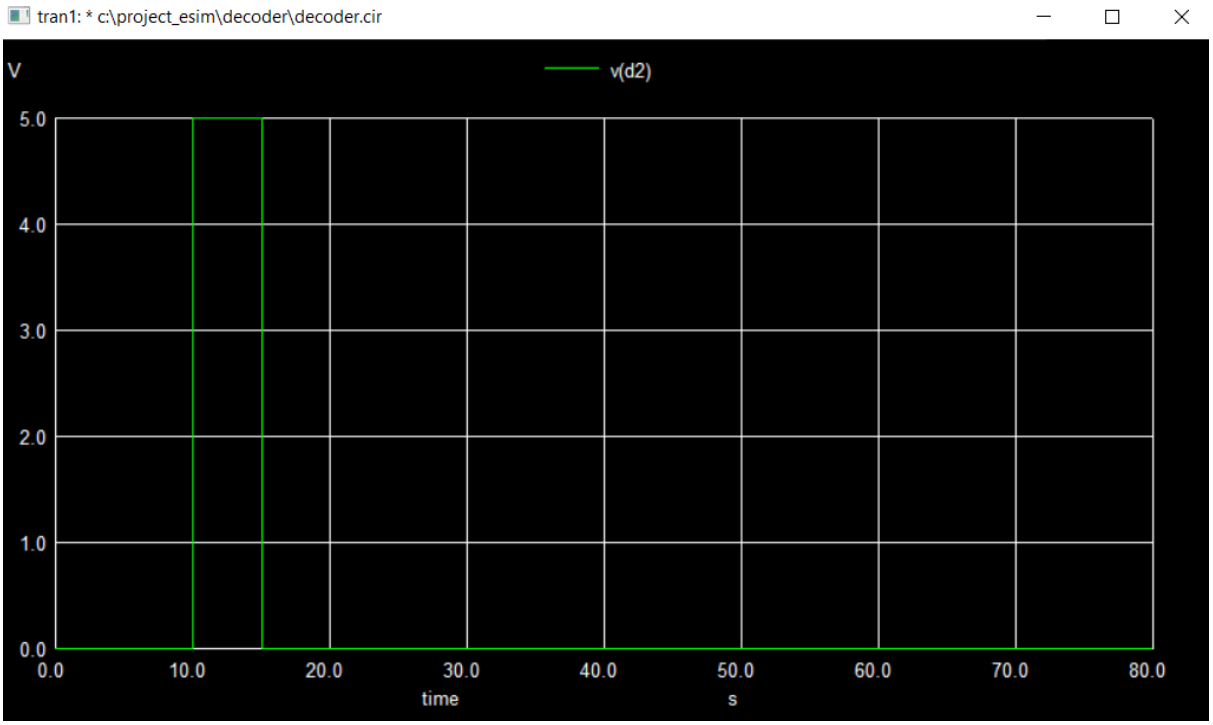
D0:



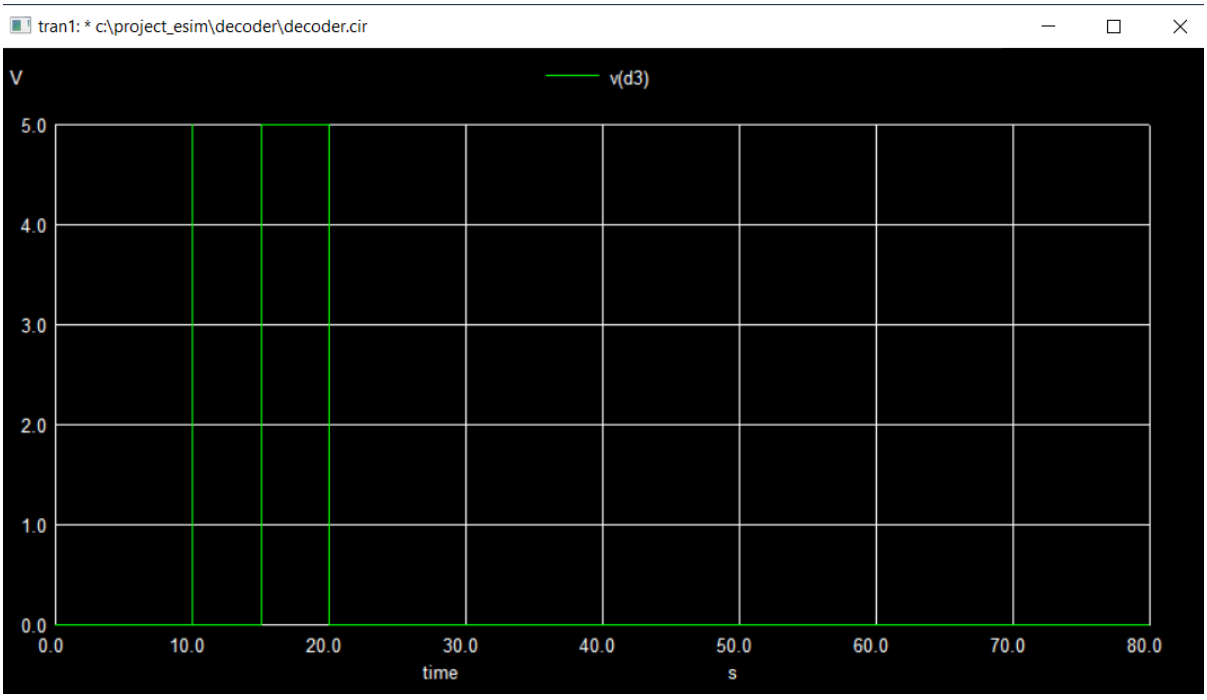
D1:



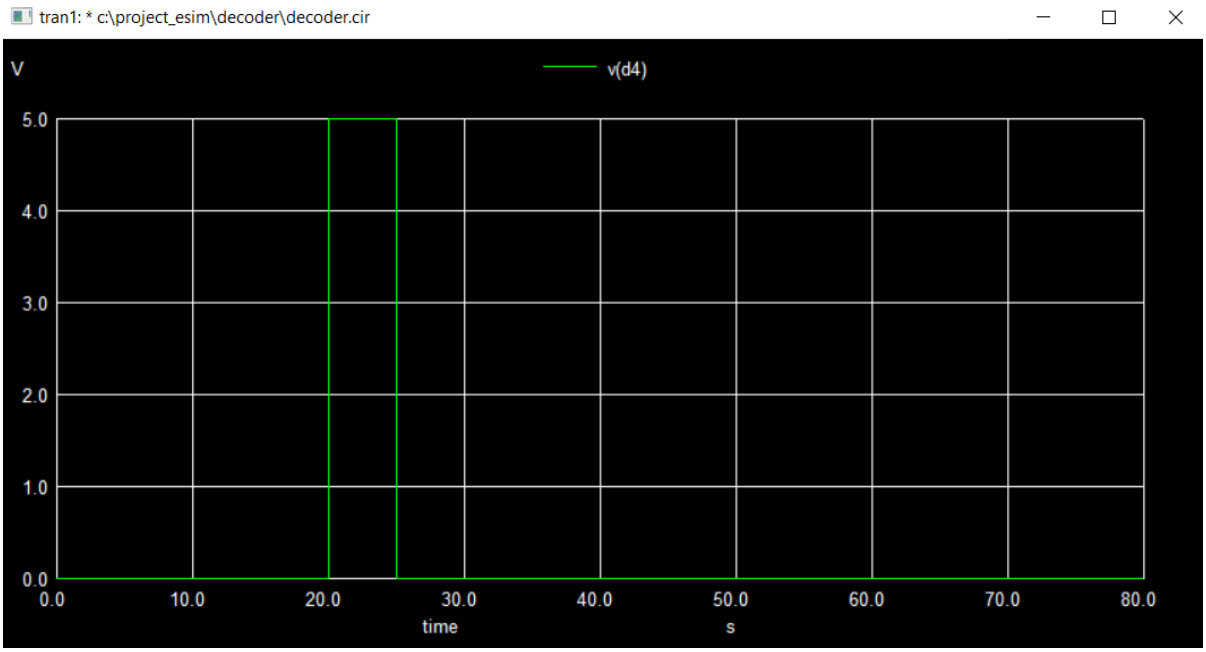
D2:


tran1: * c:\project_esim\decoder\decoder.cir
V
v(d2)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
time
s

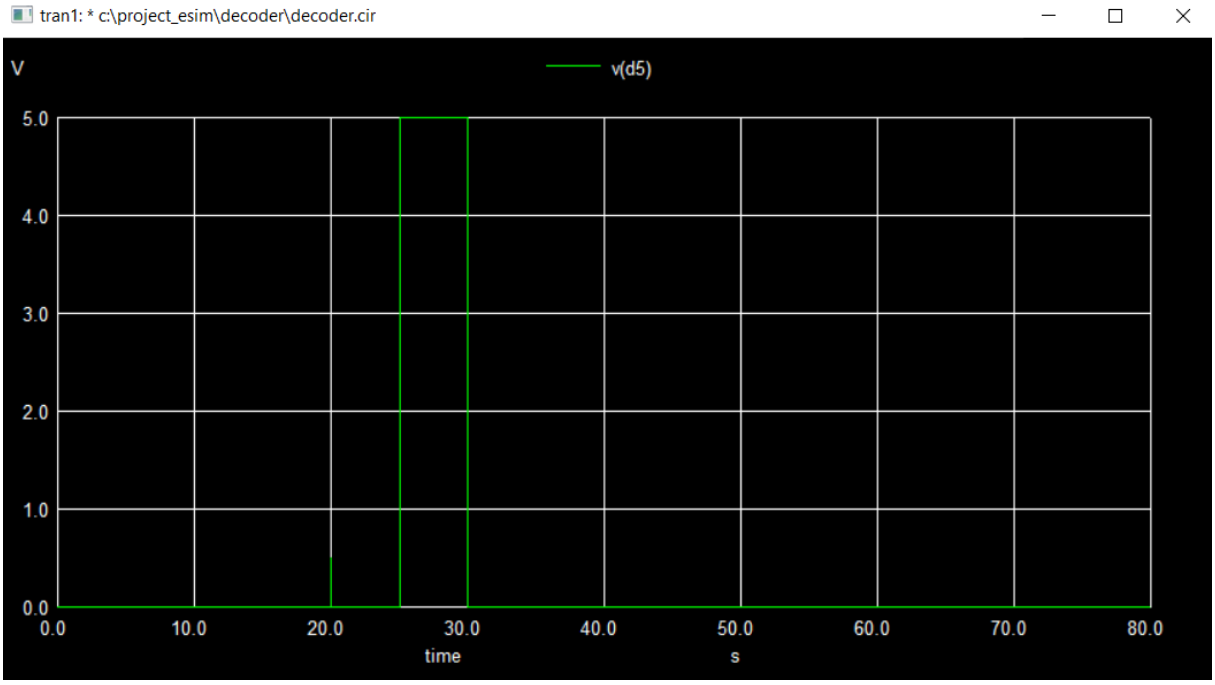
D3:


tran1: * c:\project_esim\decoder\decoder.cir
V
v(d3)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
time
s

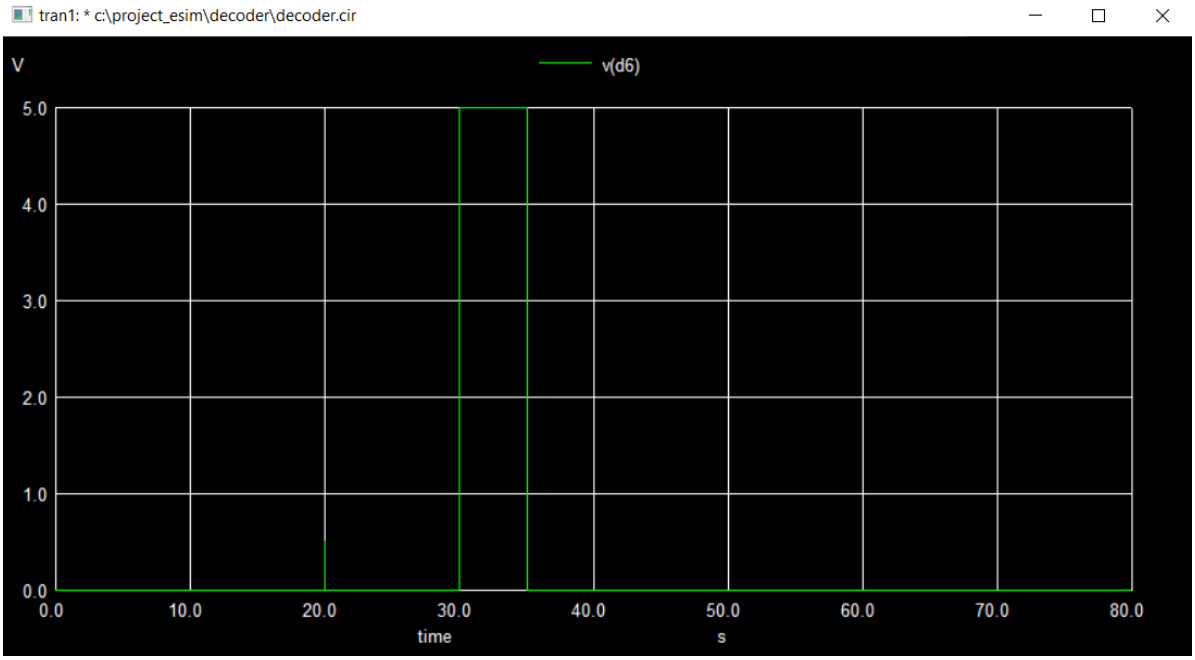
D4:


tran1: * c:\project_esim\decoder\decoder.cir
V
v(d4)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
time
s

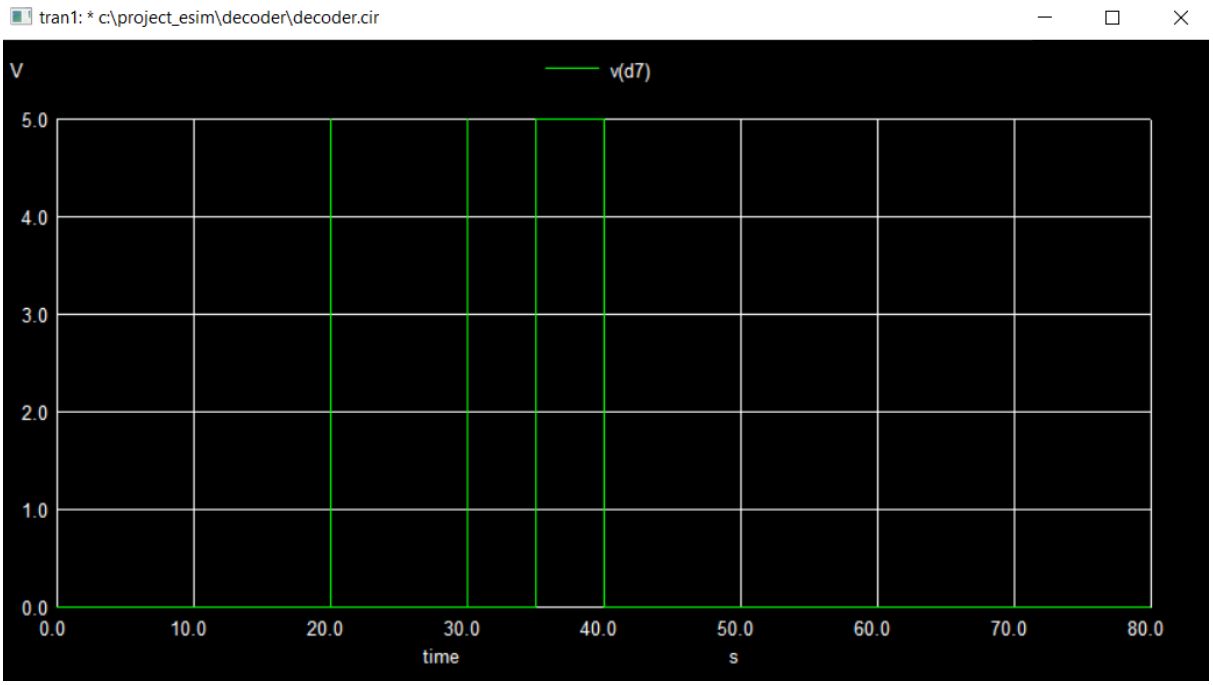
D5:


tran1: * c:\project_esim\decoder\decoder.cir
V
v(d5)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
time
s

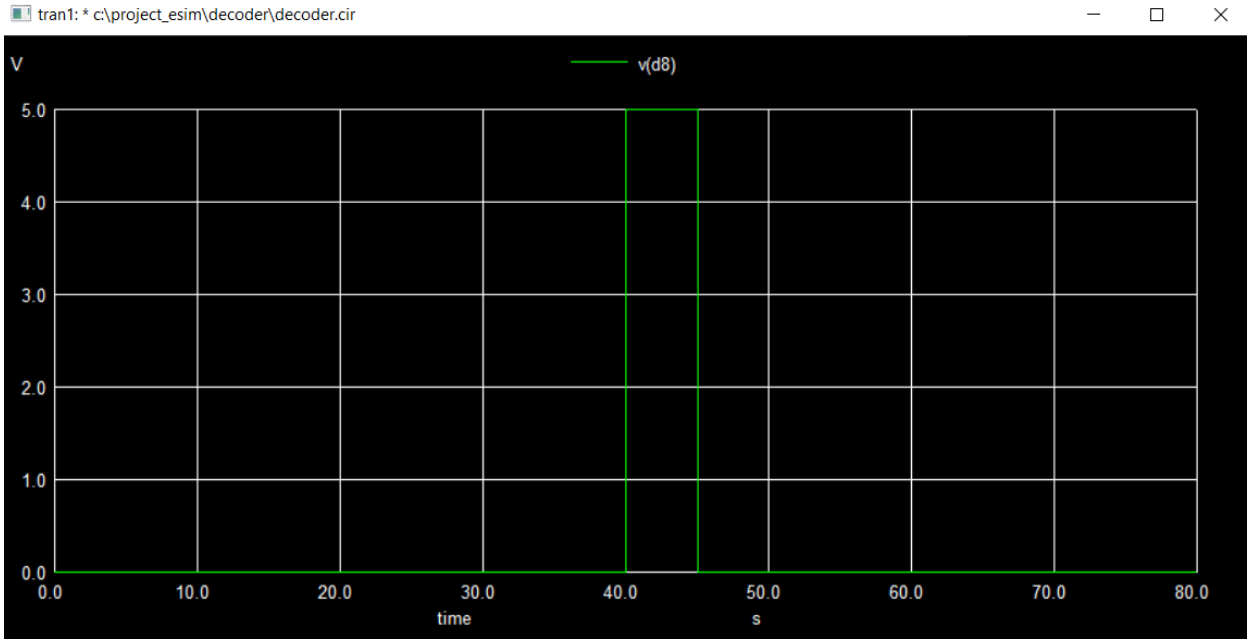
D6:


tran1: * c:\project_esim\decoder\decoder.cir
V
v(d6)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
time
s

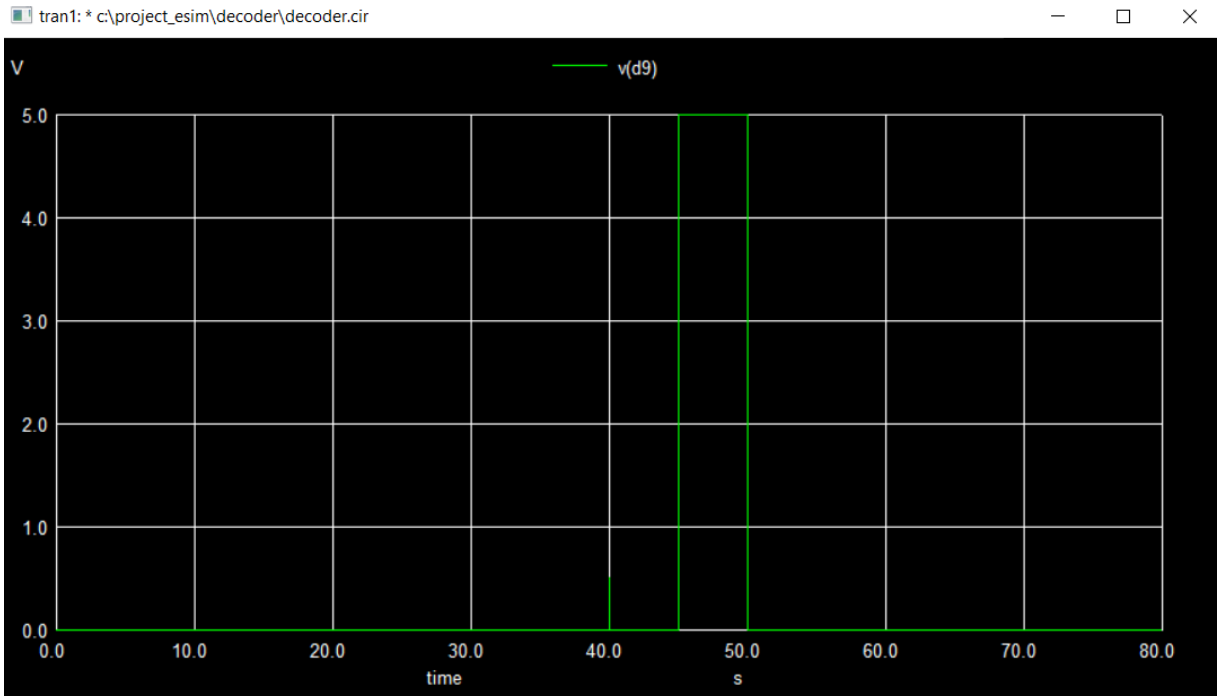
D7:


tran1: * c:\project_esim\decoder\decoder.cir
V
v(d7)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
time
s

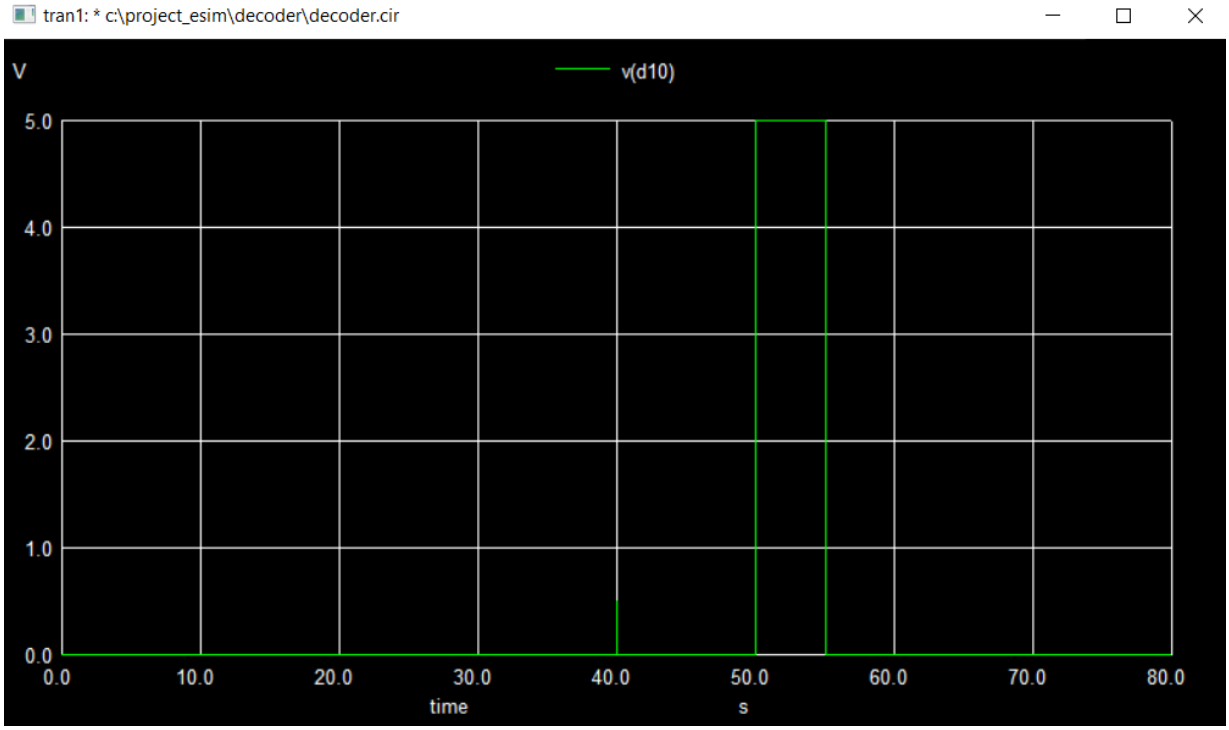
D8:


tran1: * c:\project_esim\decoder\decoder.cir
V
v(d8)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
time
s

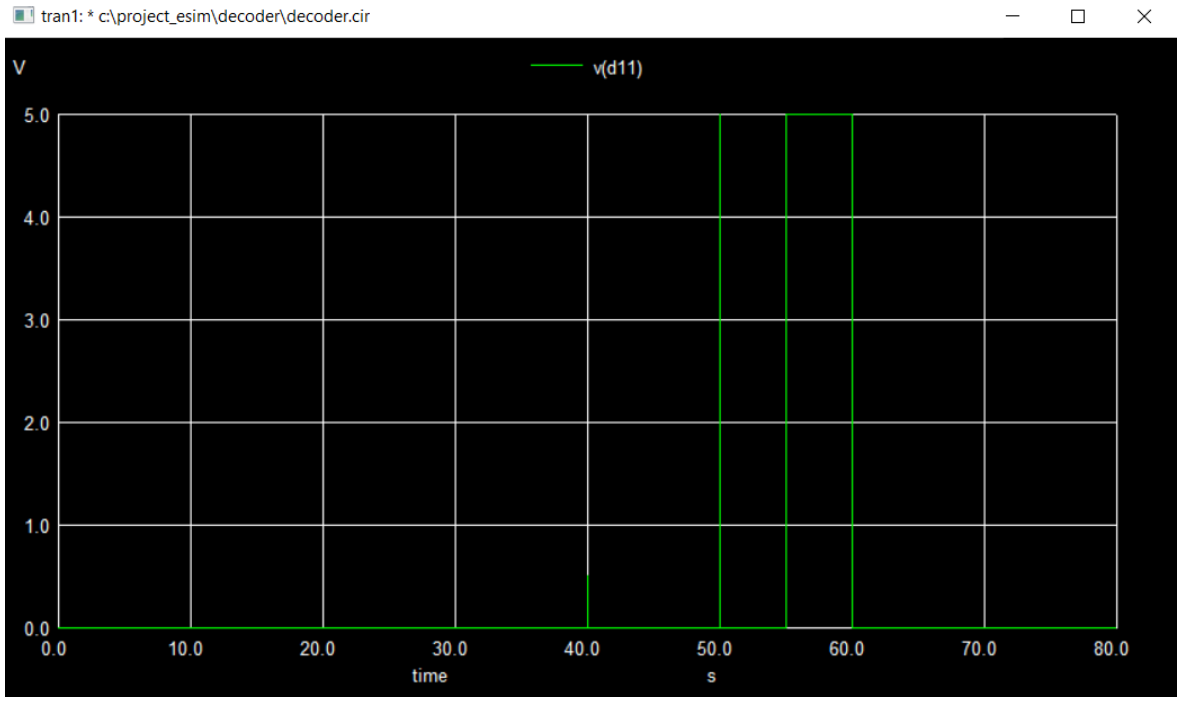
D9:


tran1: * c:\project_esim\decoder\decoder.cir
V
v(d9)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
time
s

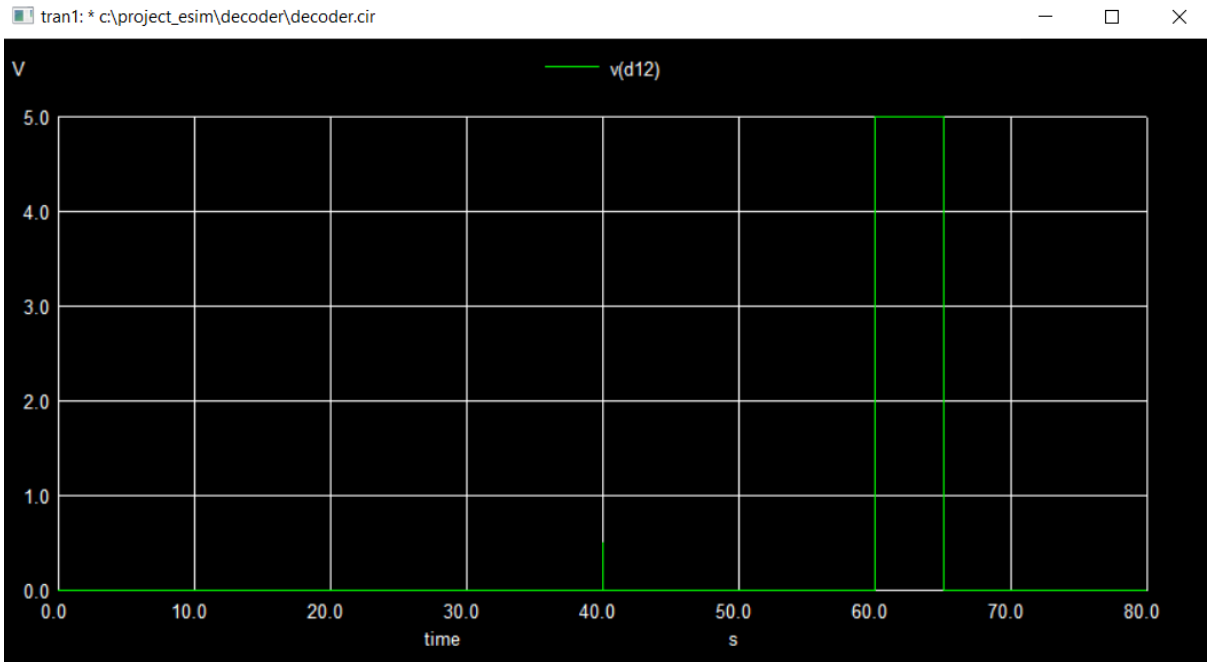
D10:


tran1: * c:\project_esim\decoder\decoder.cir
V
v(d10)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
time
s

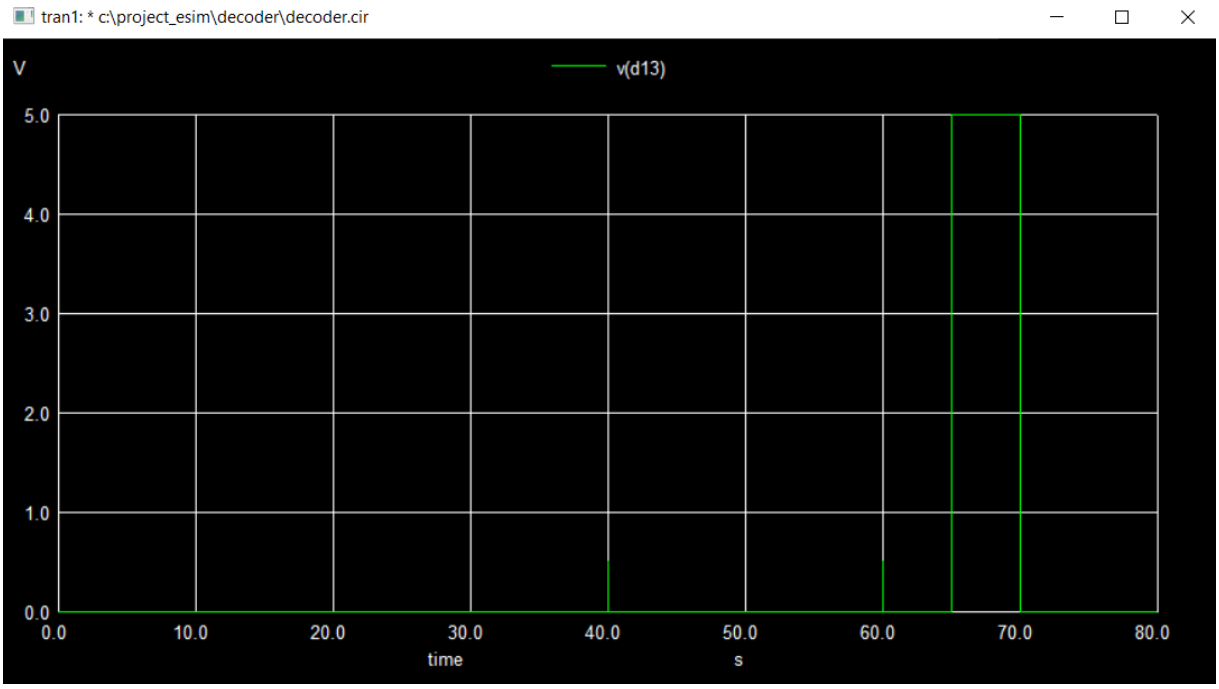
D11:


tran1: * c:\project_esim\decoder\decoder.cir
V
v(d11)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
time
s

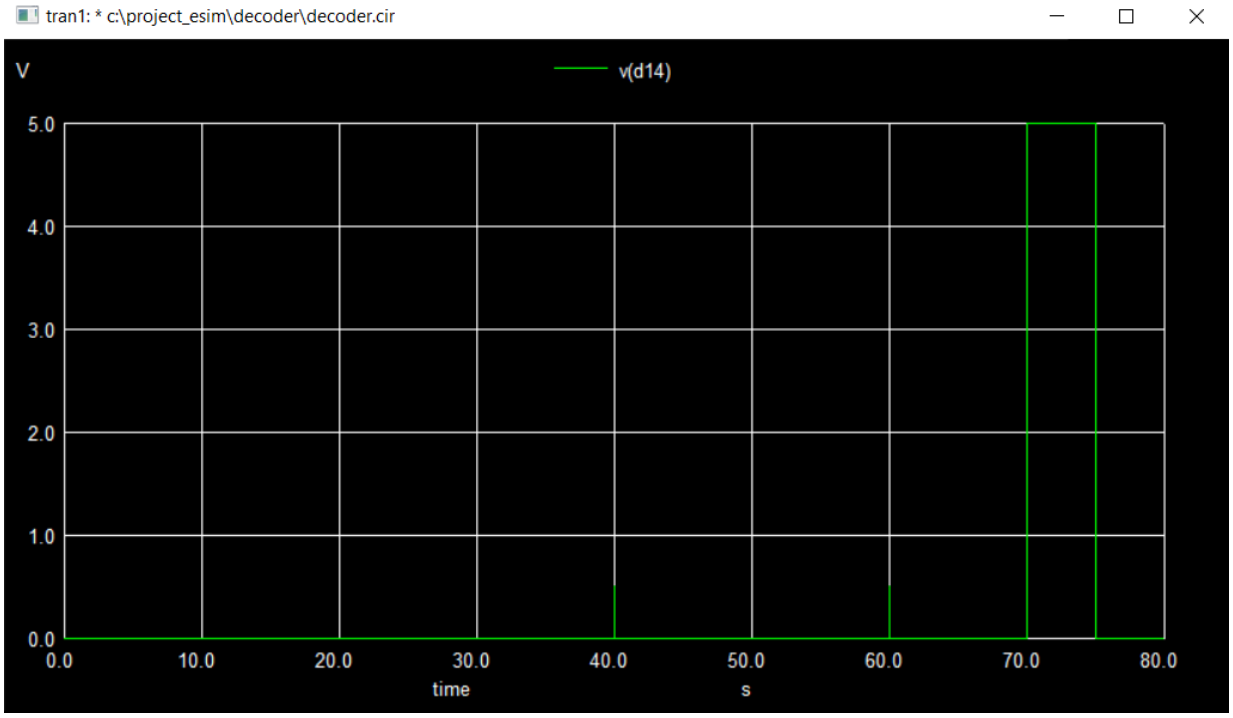
D12:


tran1: * c:\project_esim\decoder\decoder.cir
V
v(d12)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
time
s

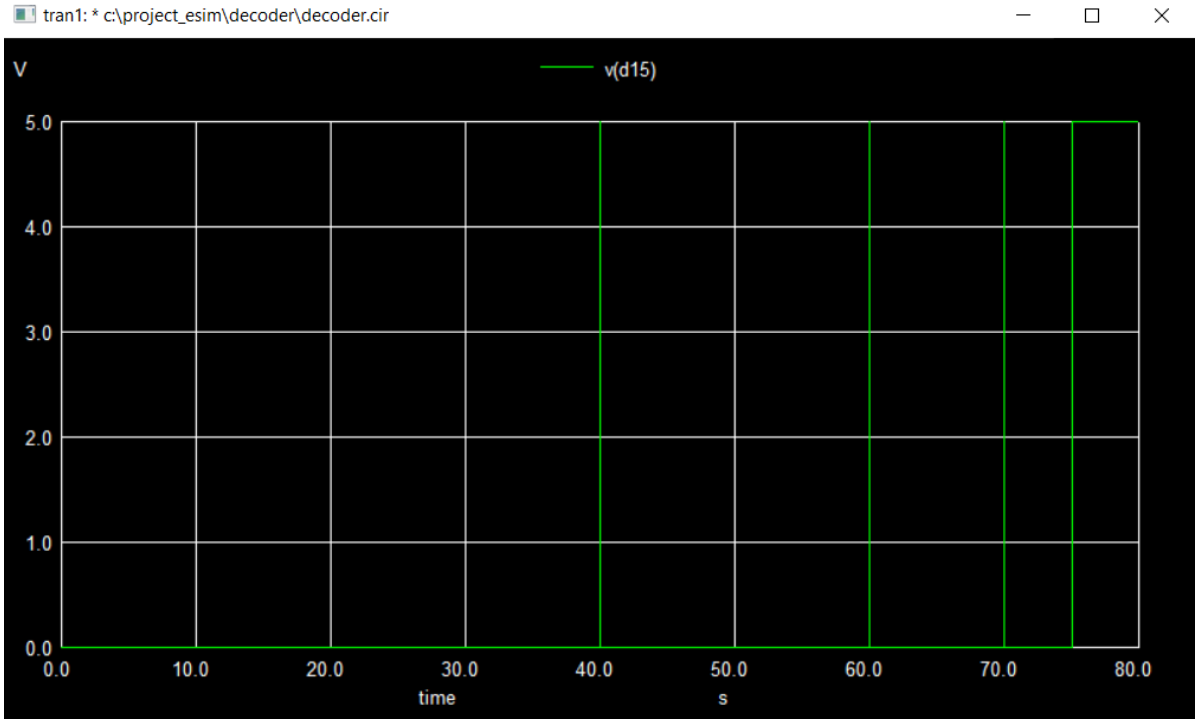
D13:


tran1: * c:\project_esim\decoder\decoder.cir
V
v(d13)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
time
s

D14:


tran1: * c:\project_esim\decoder\decoder.cir
V
v(d14)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
time
s

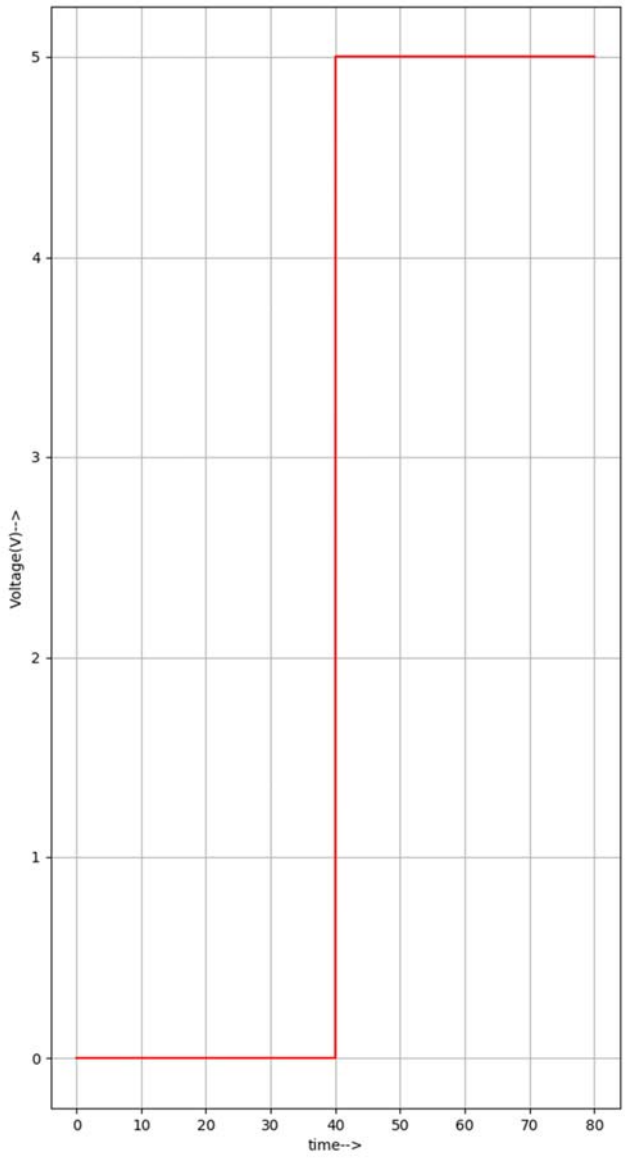
D15:


tran1: * c:\project_esim\decoder\decoder.cir
V
v(d15)
5.0
4.0
3.0
2.0
1.0
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
time
s

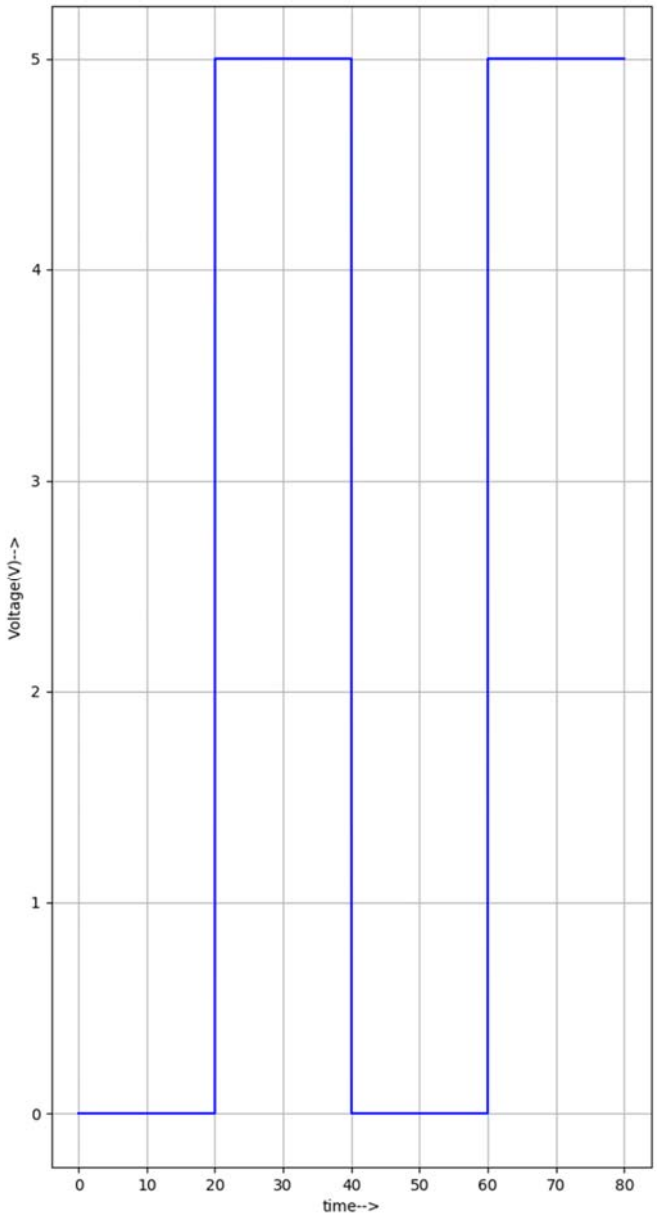
Python plots:

Inputs:

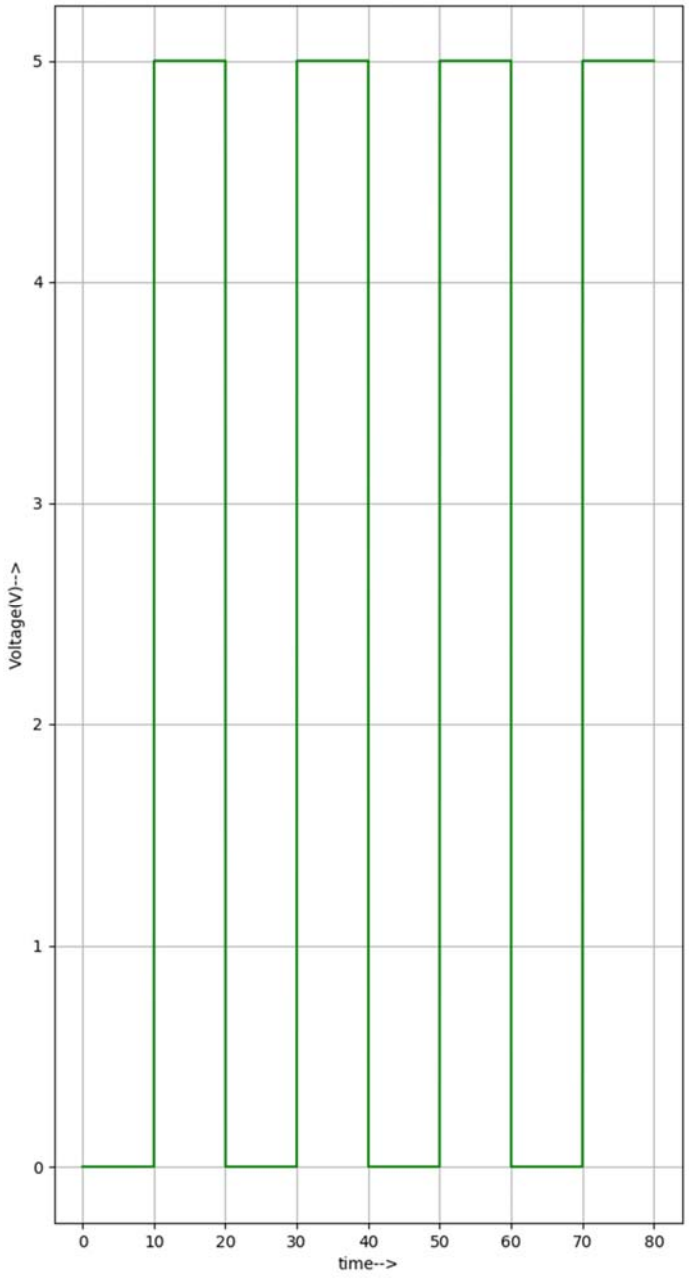
A:



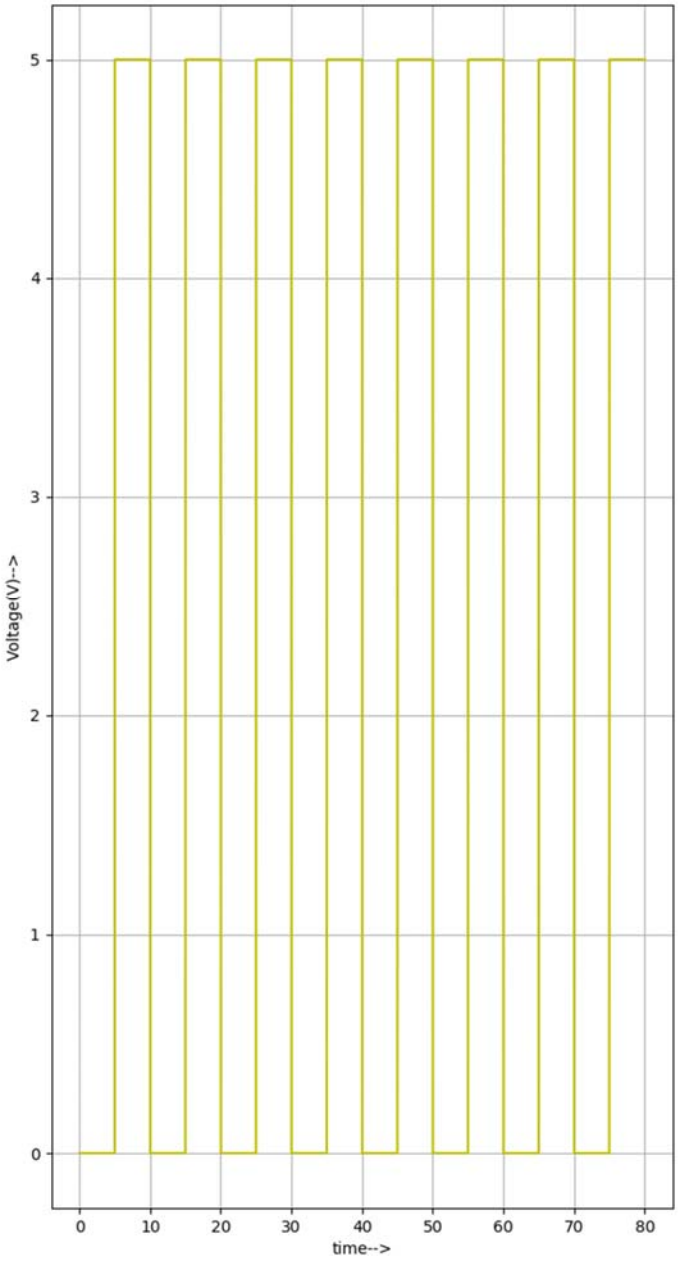
B:



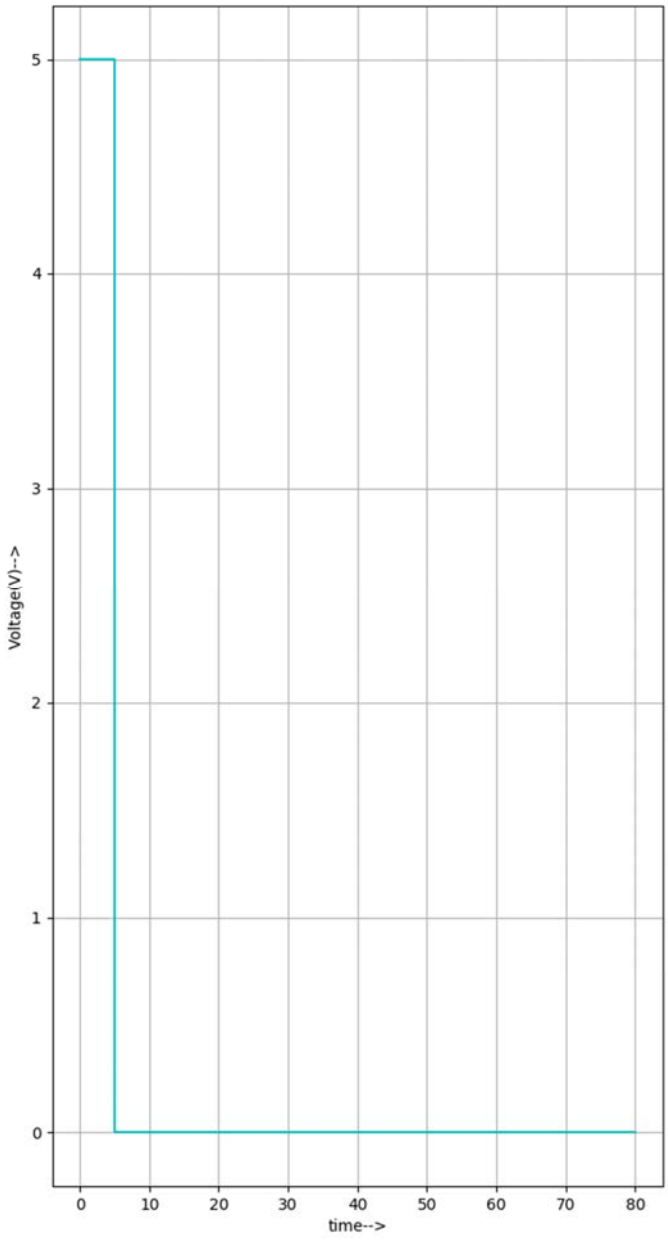
C:



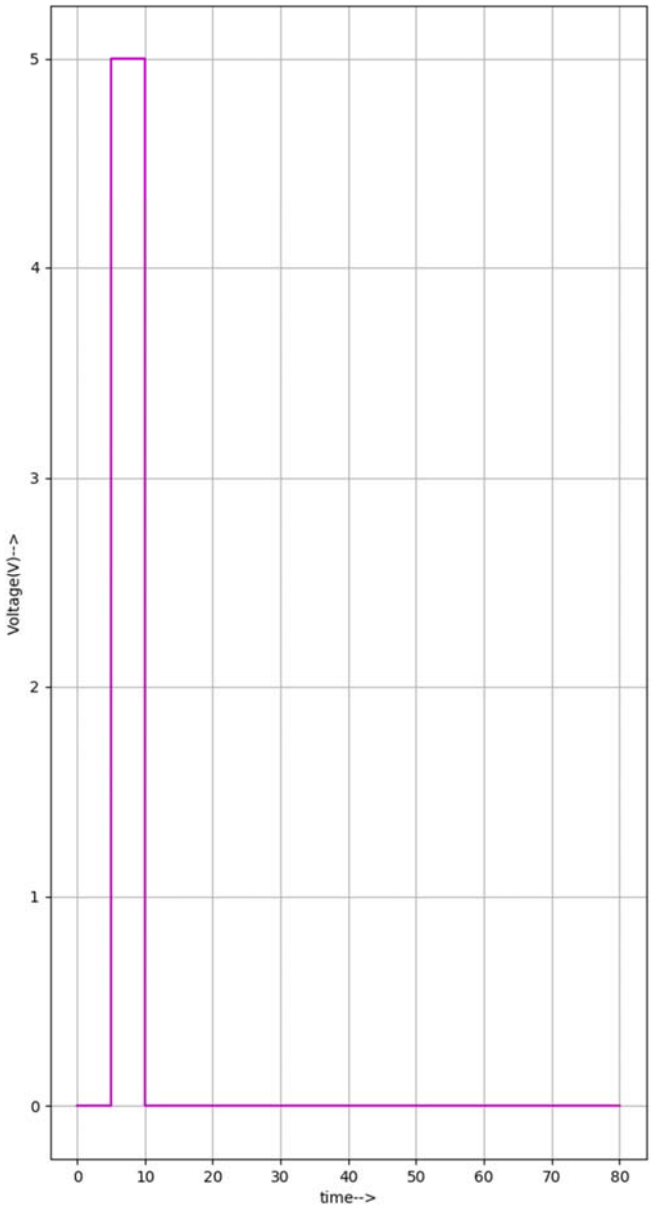
D:



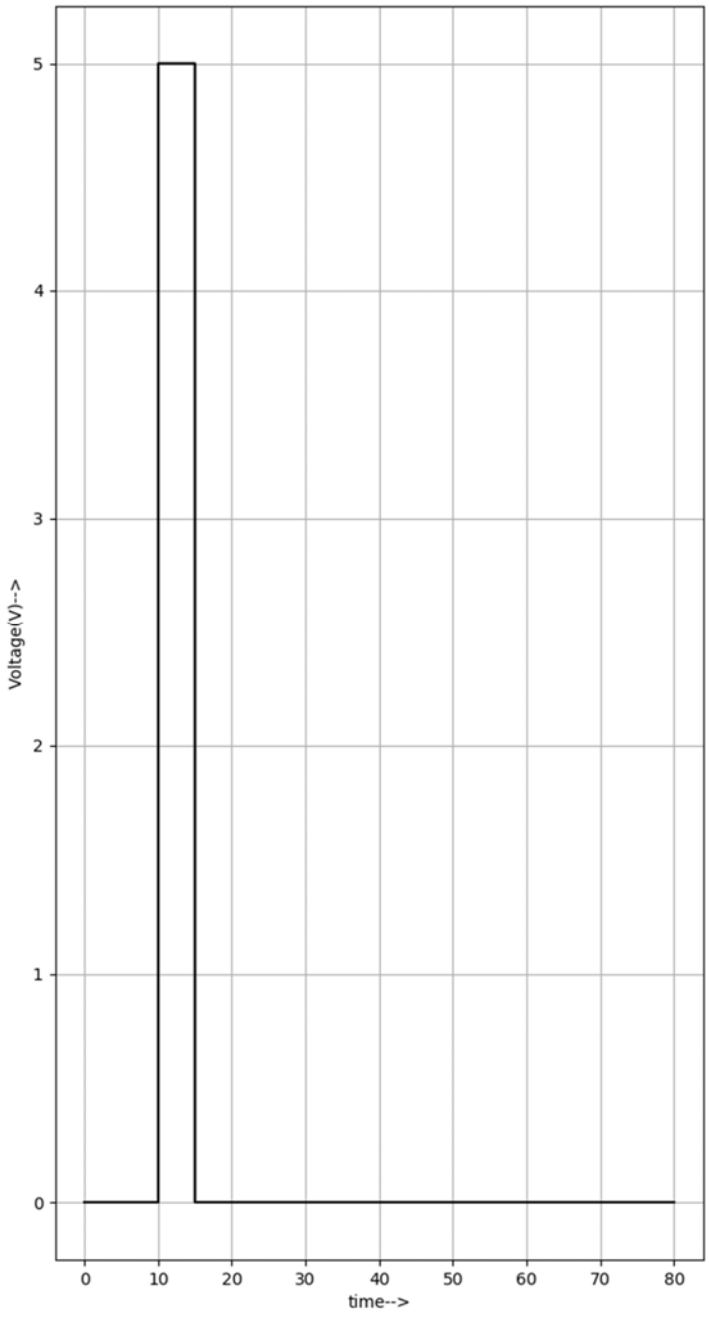
D0:



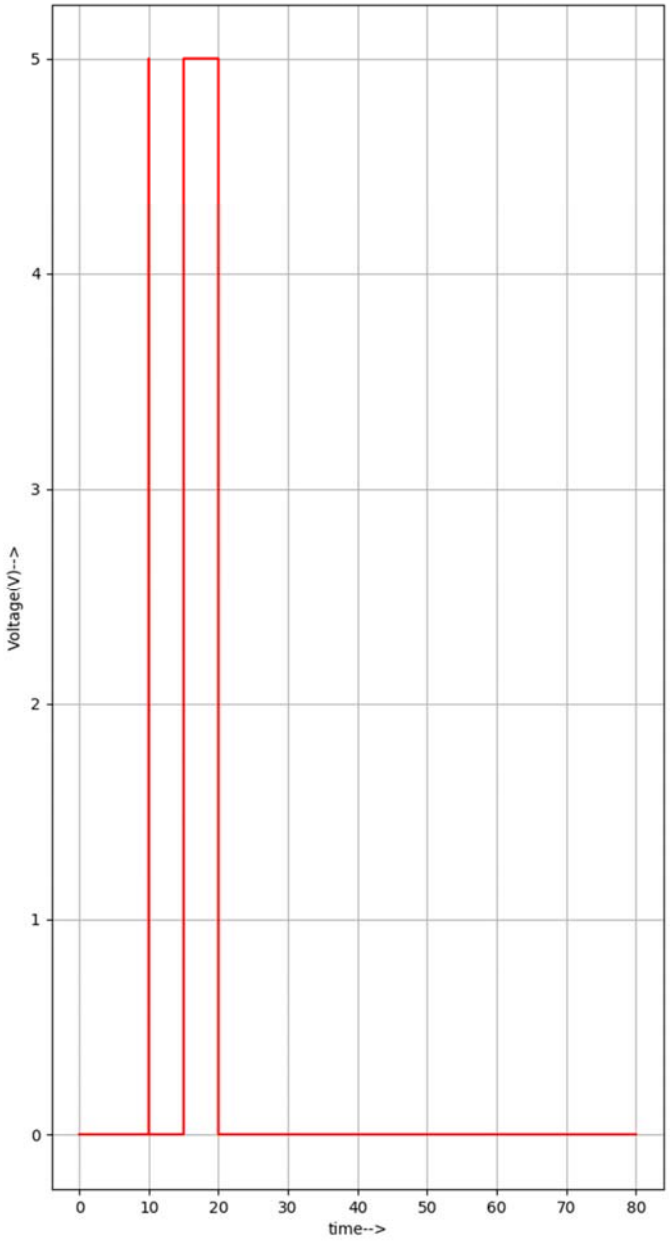
D1:



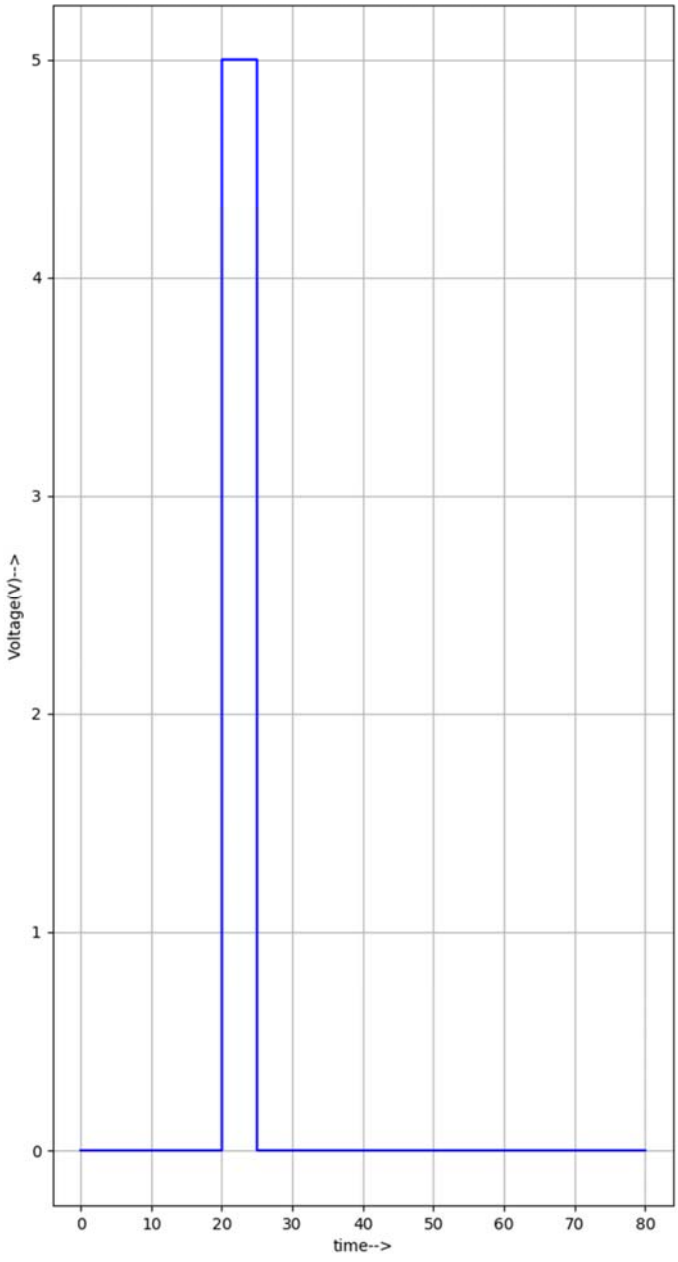
D2:



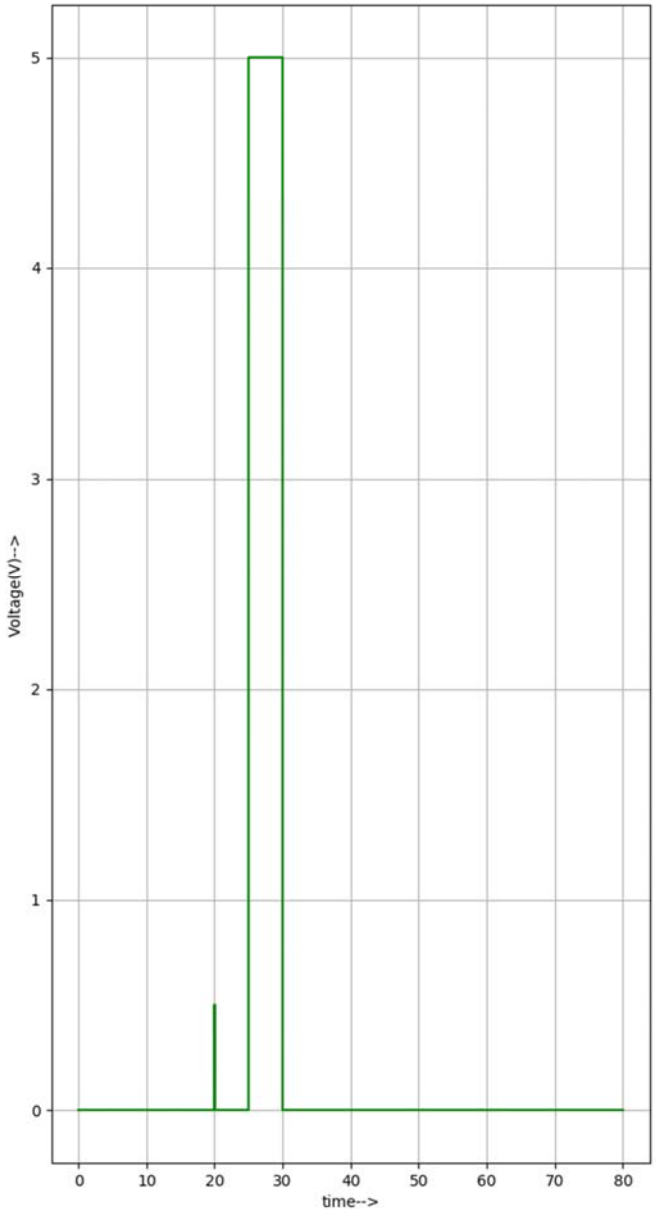
D3:



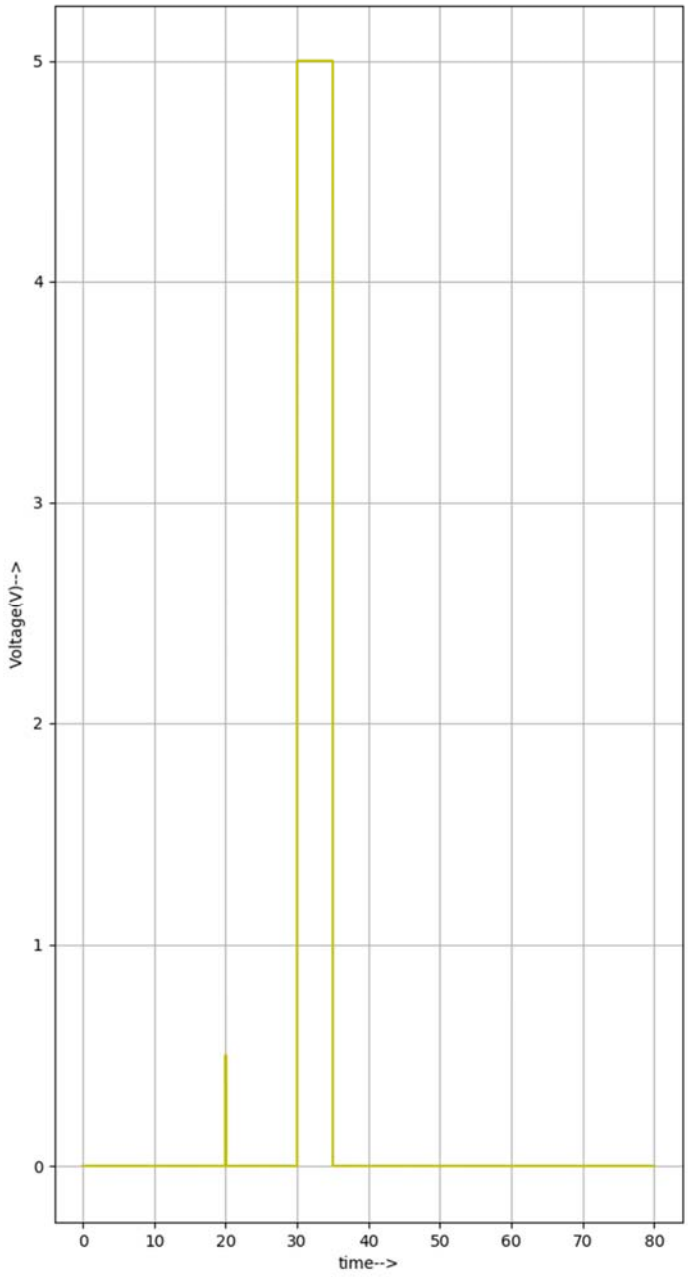
D4:



D5:



D6:



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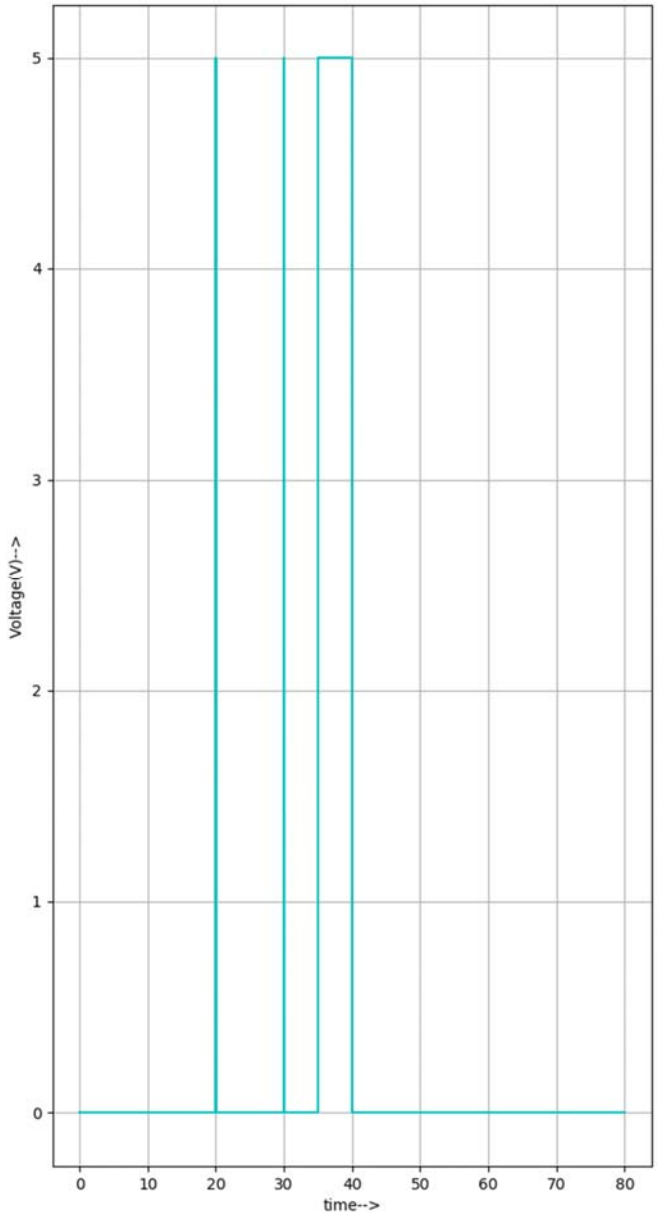

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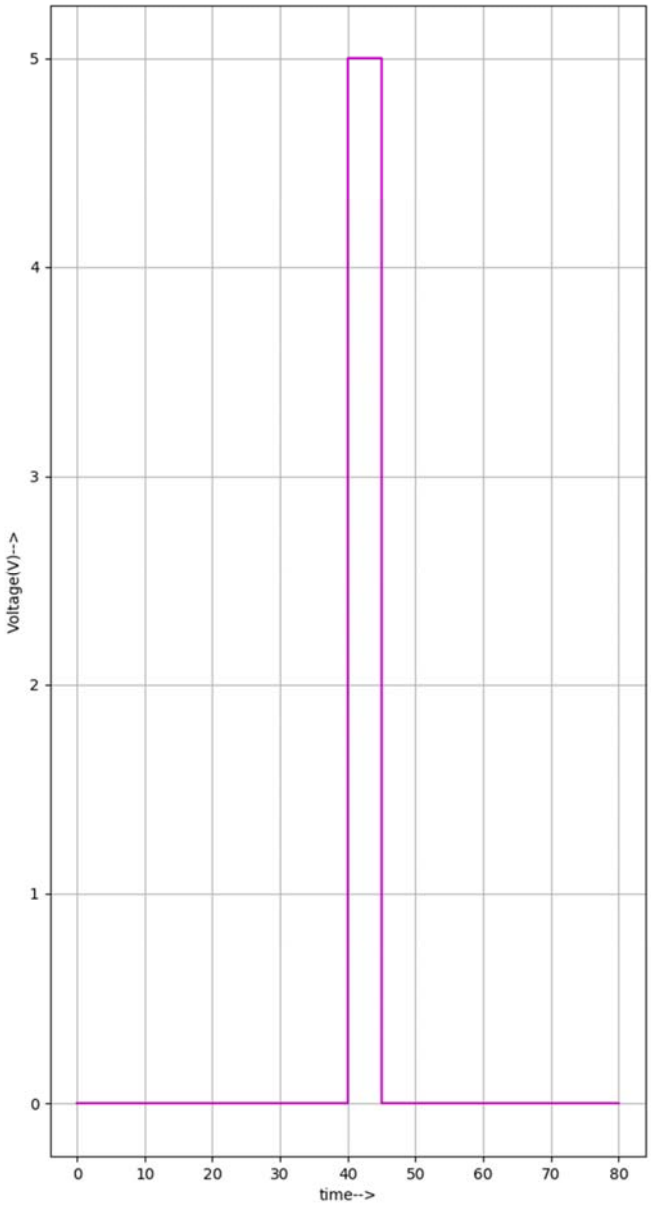

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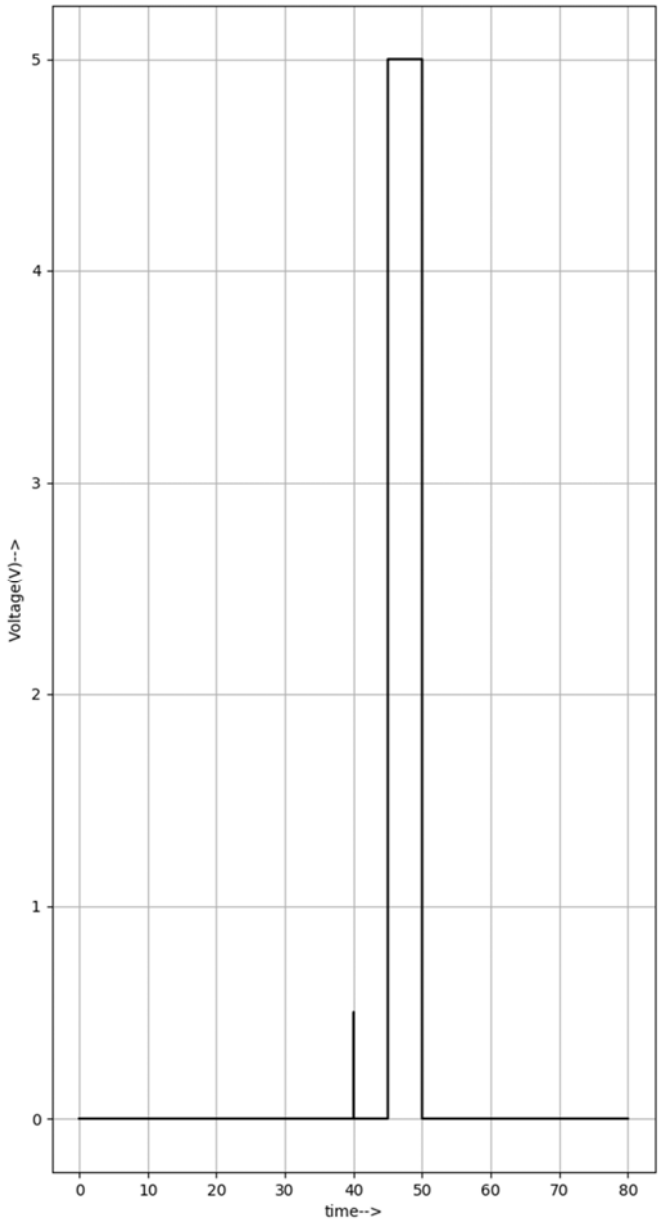

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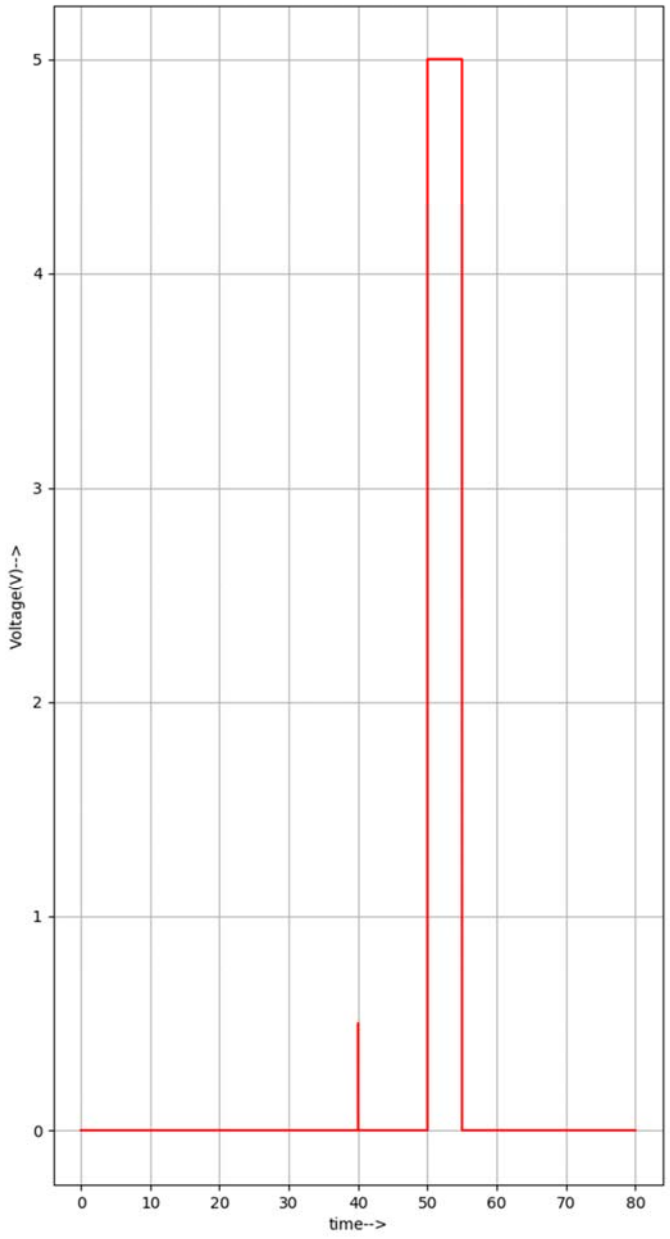

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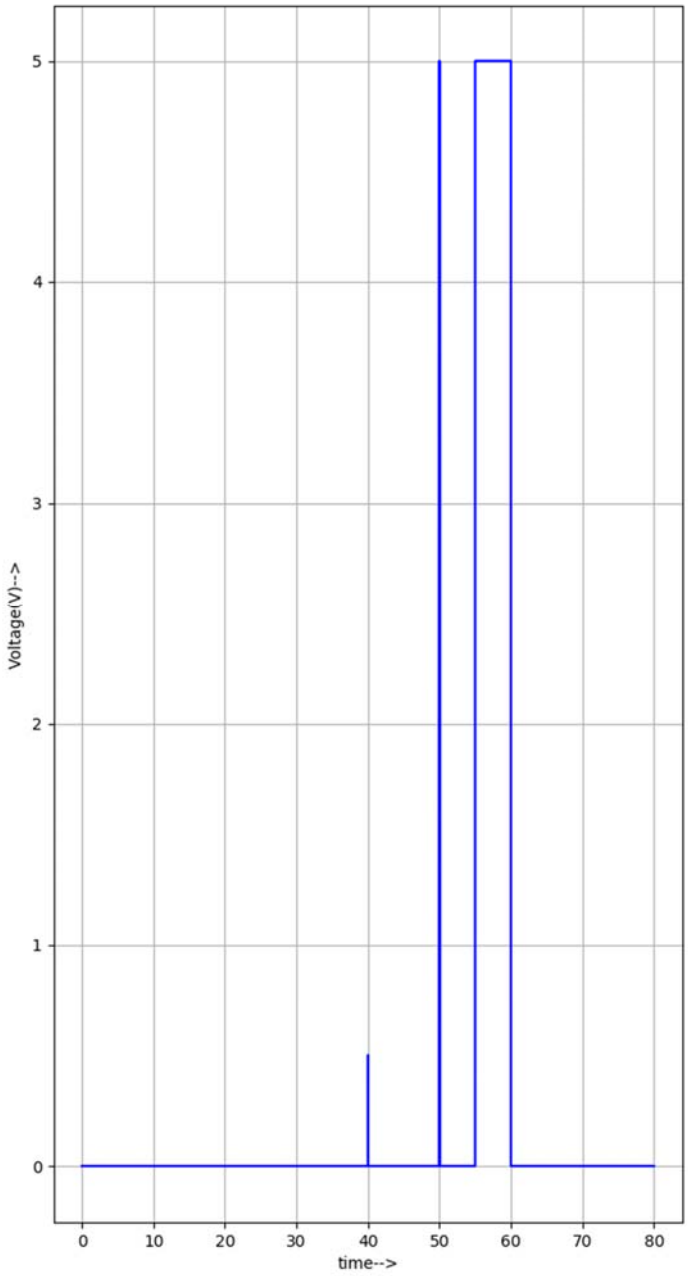

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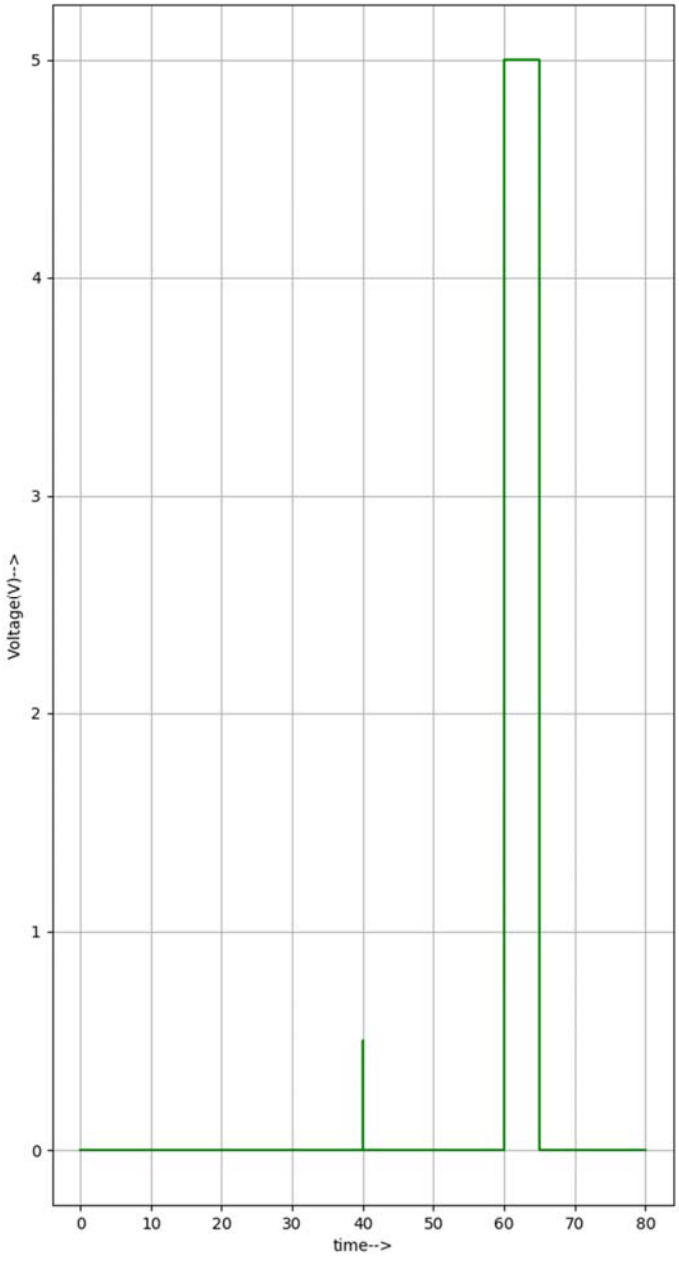

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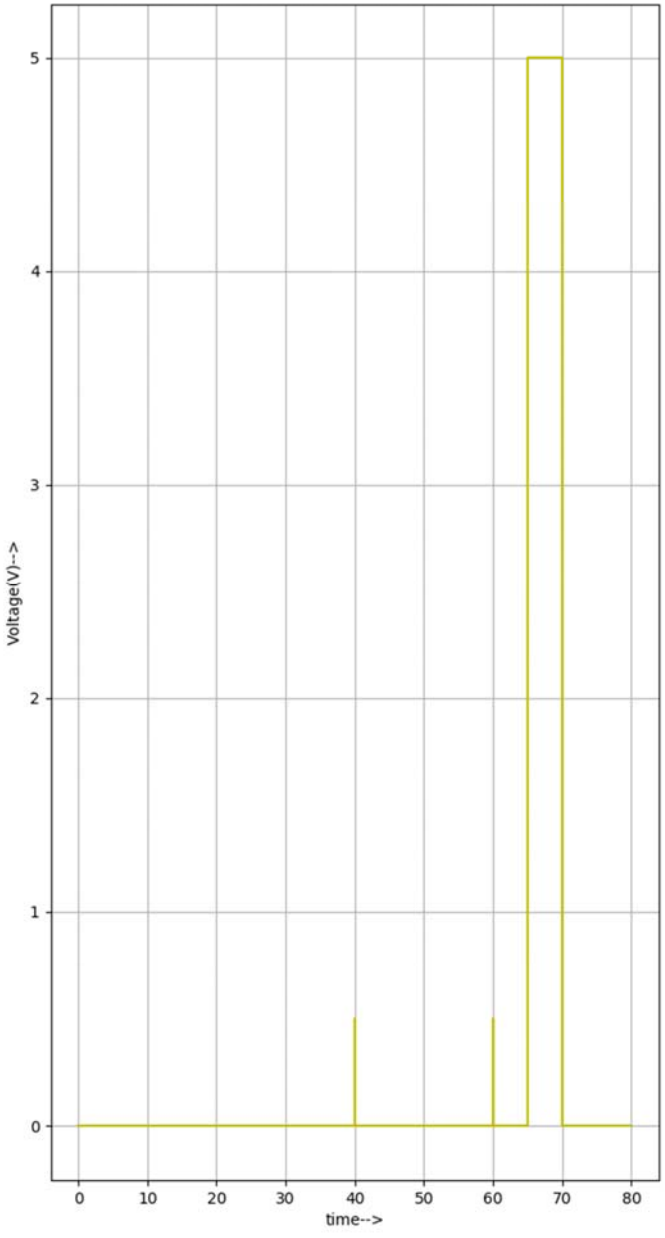

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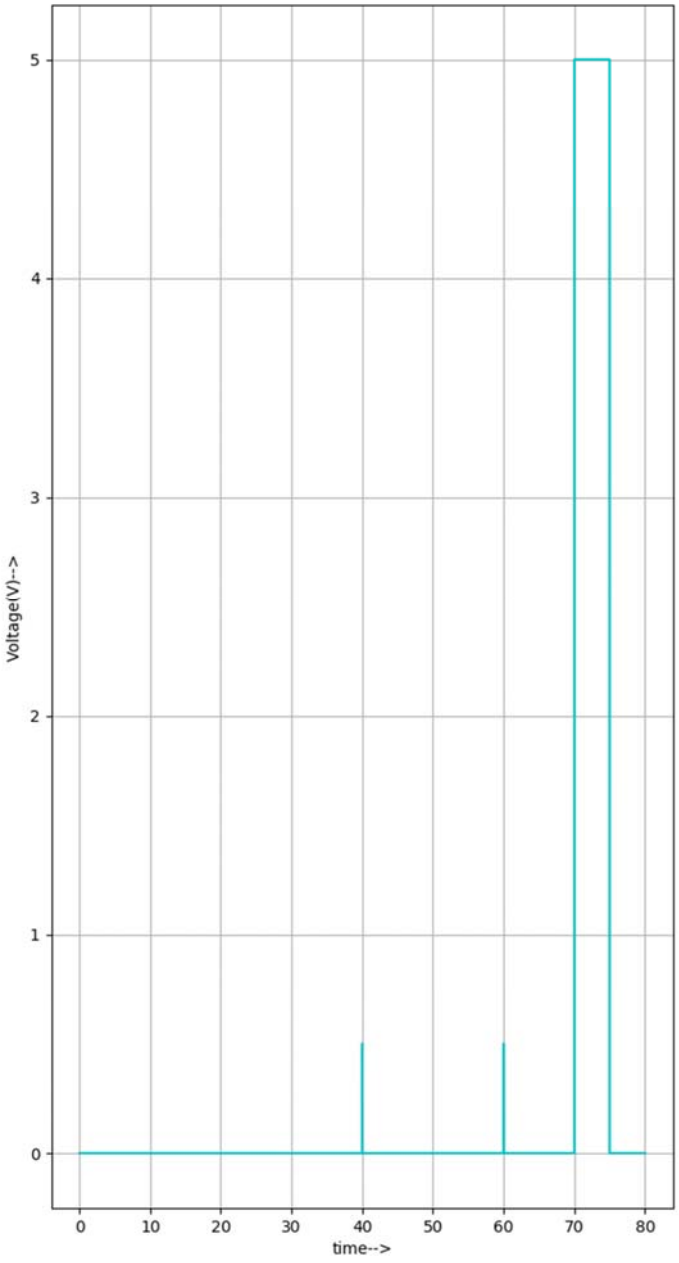

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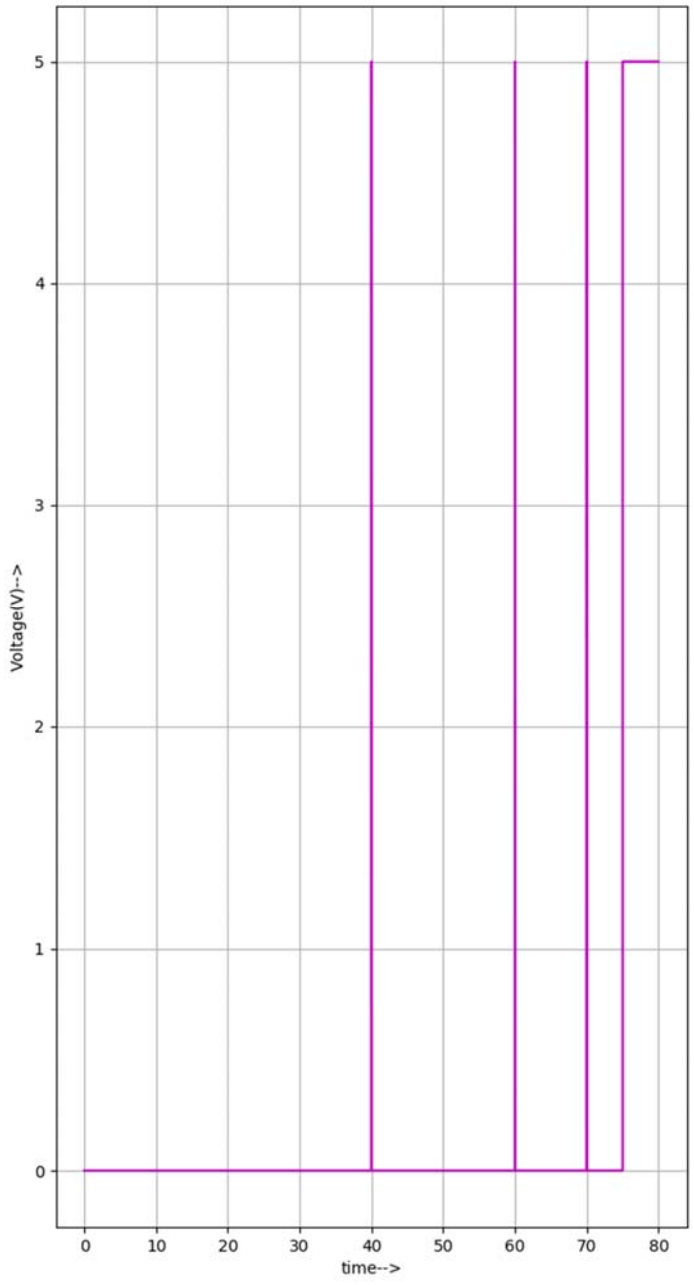

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