Title of the experiment:

Adiabatic Logic Gates

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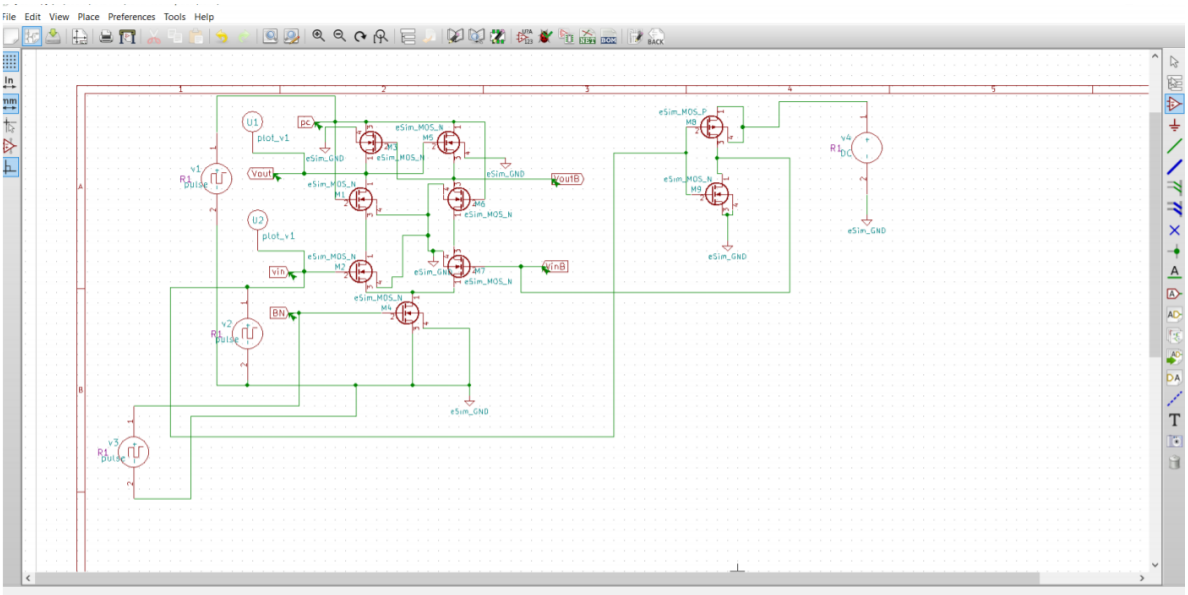
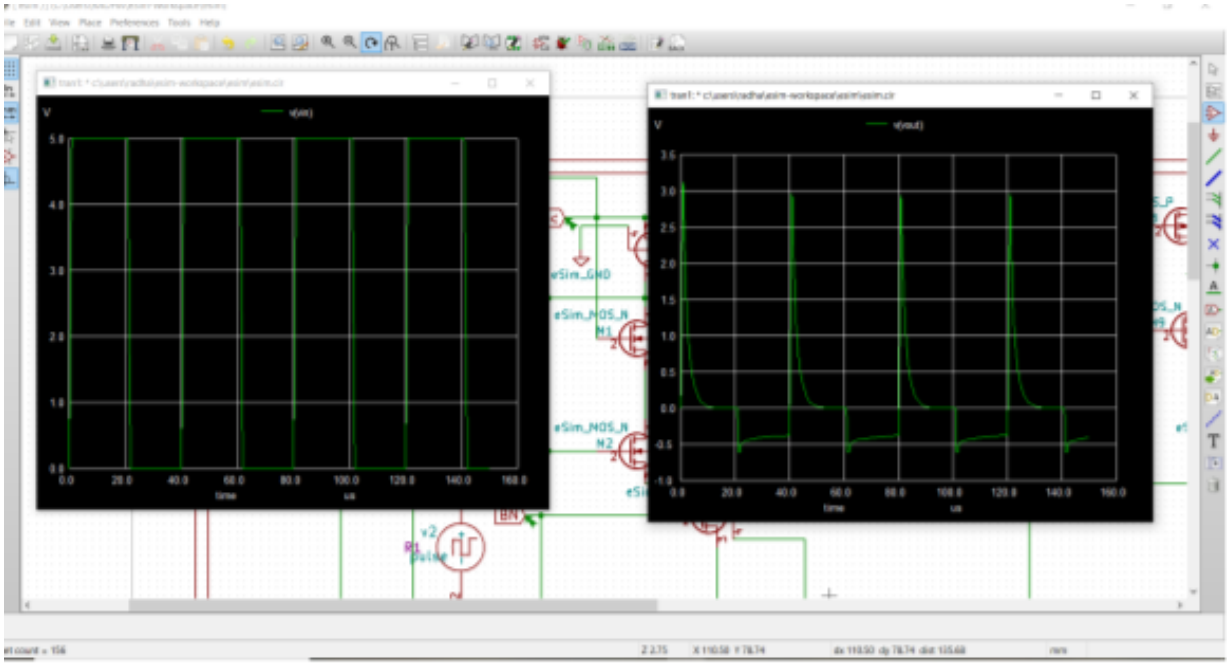
Theory:

Architecture of Adiabatic circuit can reduce energy dissipation by steering currents and recycling the stored energy in the capacitor. So here the SCAL can achieve increased energy efficiency by using tunable current source which controls the rate of charge flow . This adiabatic circuit can avoid problems like increased energy dissipation , multiple power-clock schemes etc. The structure of SCAL NMOS is described in the circuit. The inverter present in the circuit has a pair of cross-coupled latches and two current controlled switches, a current source and two functional blocks. Through the current source the charge flow rate is controlled by W/L ratio. Their activity is by and by subject to major energy-speed compromises, actually like some other actual acknowledgment of boolean rationale. Subsequently, adiabatic circuits with very low energy utilization at low frequencies neglect to work at high working frequencies. Alternately, rapid adiabatic circuits will in general be dissipative at low clock rates. The PMOS SCAL can operate in two phases namely : Evaluate and Discharge. During discharge the energy stored in the node out is discharged. The crosscoupled latches performs as a sense-amplifier and boosts the voltage difference of the two output nodes. SCAL seems to be less dissipative as compared to the TSEL and 2N-2P for the entire operating regime.

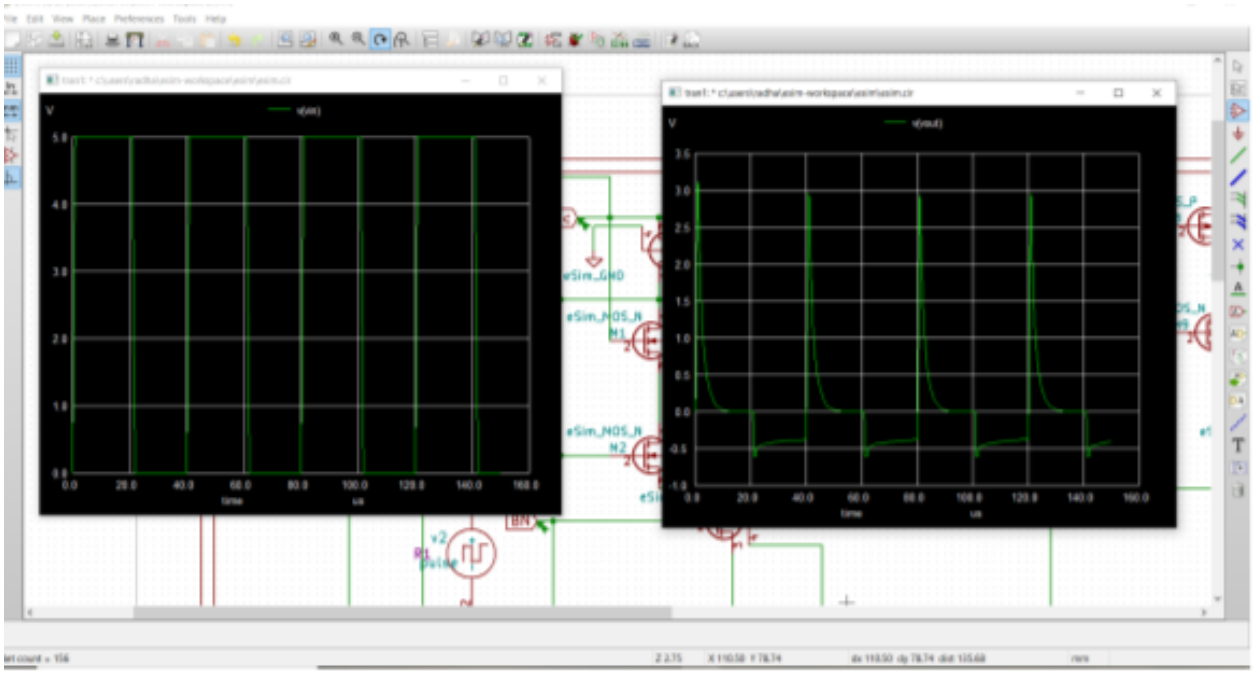
Schematic Diagram :



Simulation Results :



Implemented Waveforms:



Conclusion:

Thus the circuit is designed and the required output is obtained.

References :

D. K. Aaina Nandal. A study on adiabatic logic circuits for low power applications. https://www.ijert.org/research/a-study-onadiabatic-logic-circuits-for-low-power-applicationsIJERTCONV5IS03008.pdf.