CMOS RS FLIPFLOP

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THEORY:

This paper constitutes of the layout and analysis of CMOS RS flip-flop in metastable state. Generally, RS flip-flops are used in many applications in logic or digital fields as they offer a uncomplicated switching features. Successful layout of digital systems with asynchronous inputs requires cautious control of timing relations. Flip-flops used as synchronizers in these systems are underneath asynchronous control therefore it can be consequently affected by propagation delays because of metastable operations which leads to system malfunctions so to avoid it an analysis of metastable operation in CMOS RS flip-flops are used.

SCHEMATIC DIAGRAM:

The circuit schematic of the CMOS RS FLIPFLOP in eSim is as shown below:

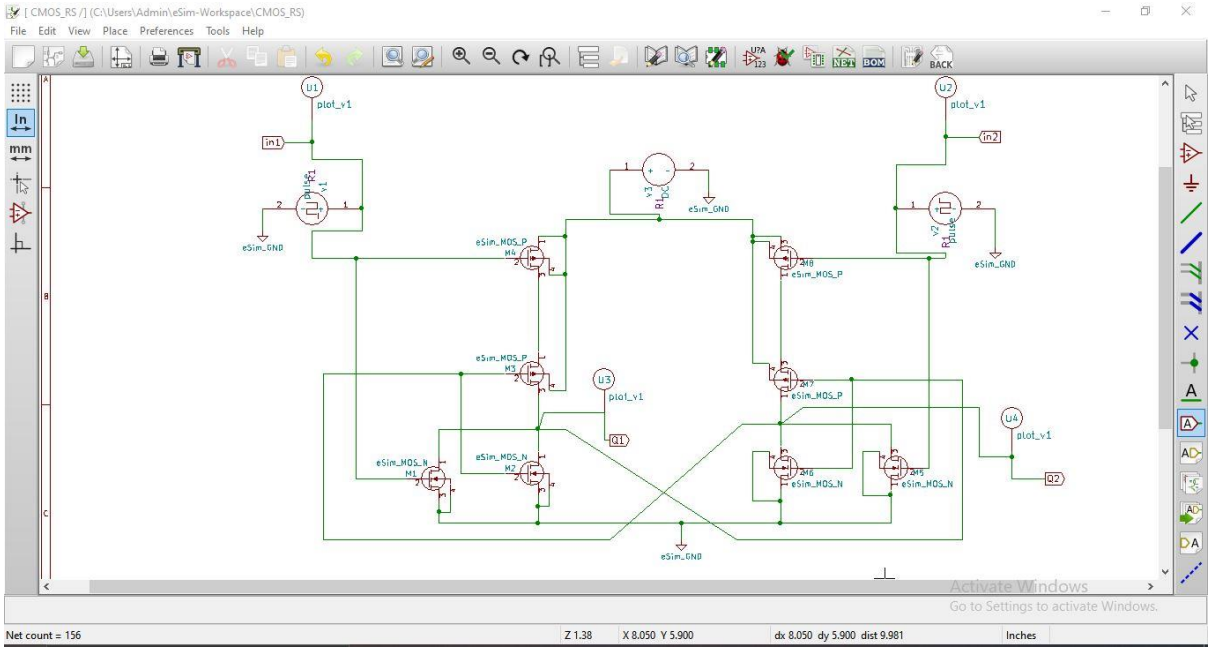

Figure 1: CMOS RS Flip-Flop

SIMULATION RESULTS:

1. NGSPICE PLOTS

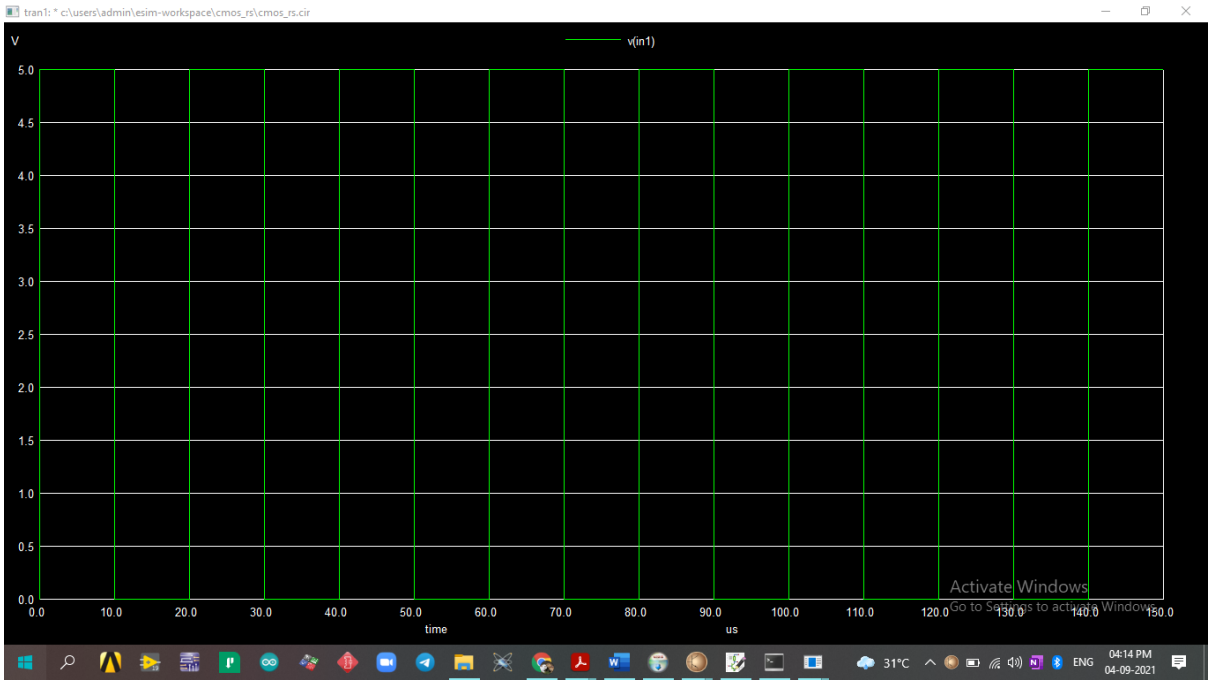

Figure 2: Ngspice Input1 plot

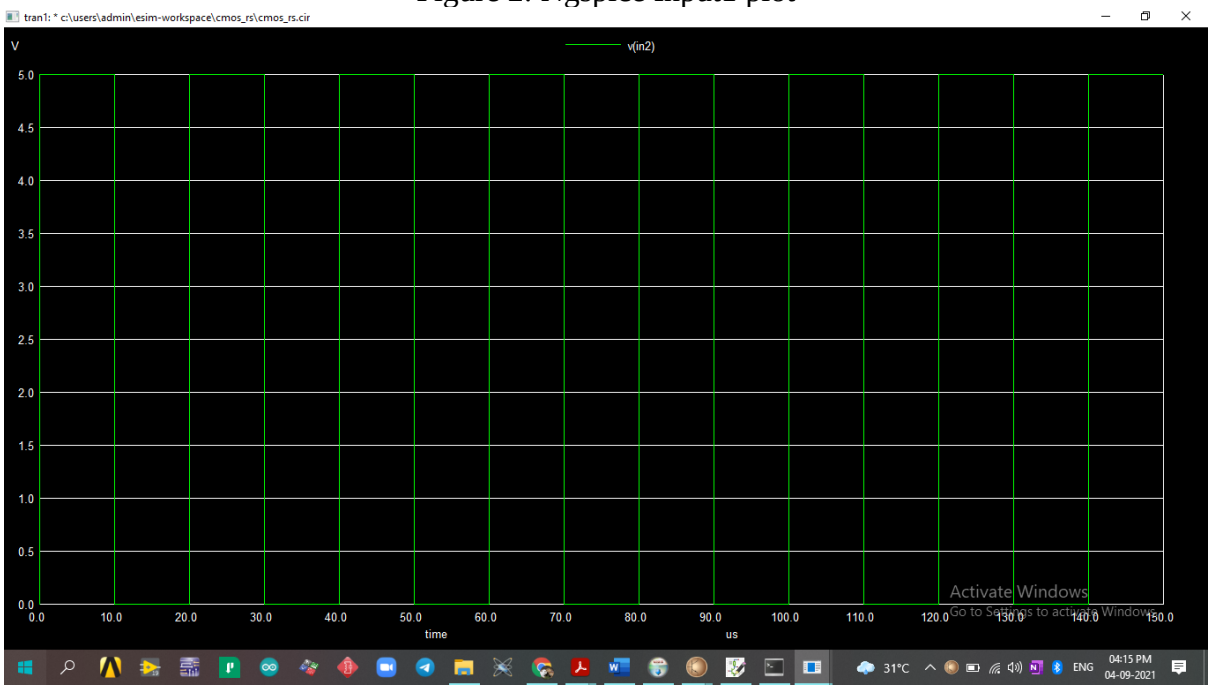

Figure 3: Ngspice Input2 plot

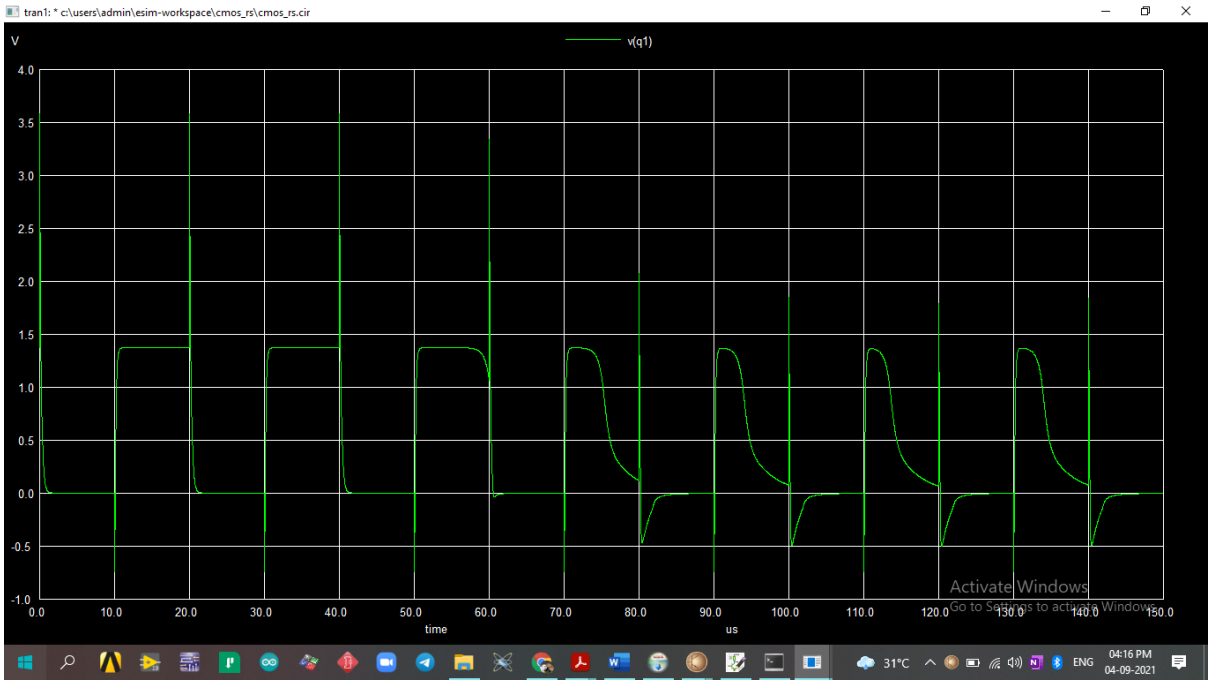

Figure 4: Ngspice output1 phase plot

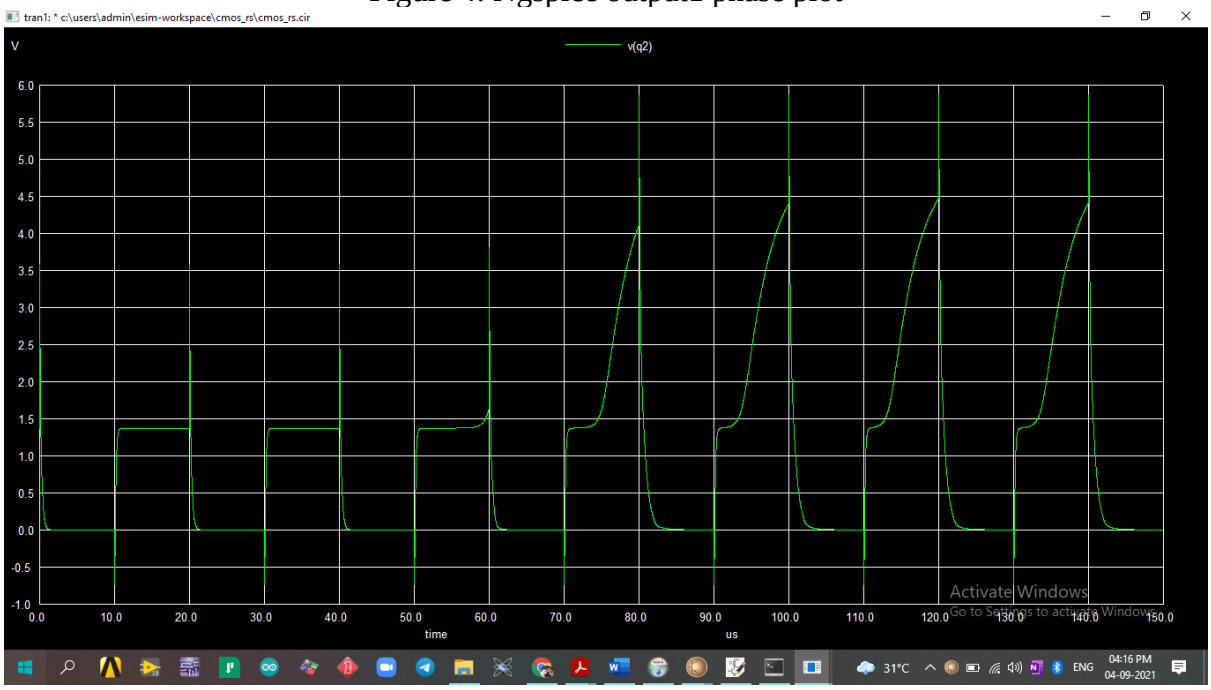

Figure 5: Ngspice output2 phase plot

2. PYTHON PLOT

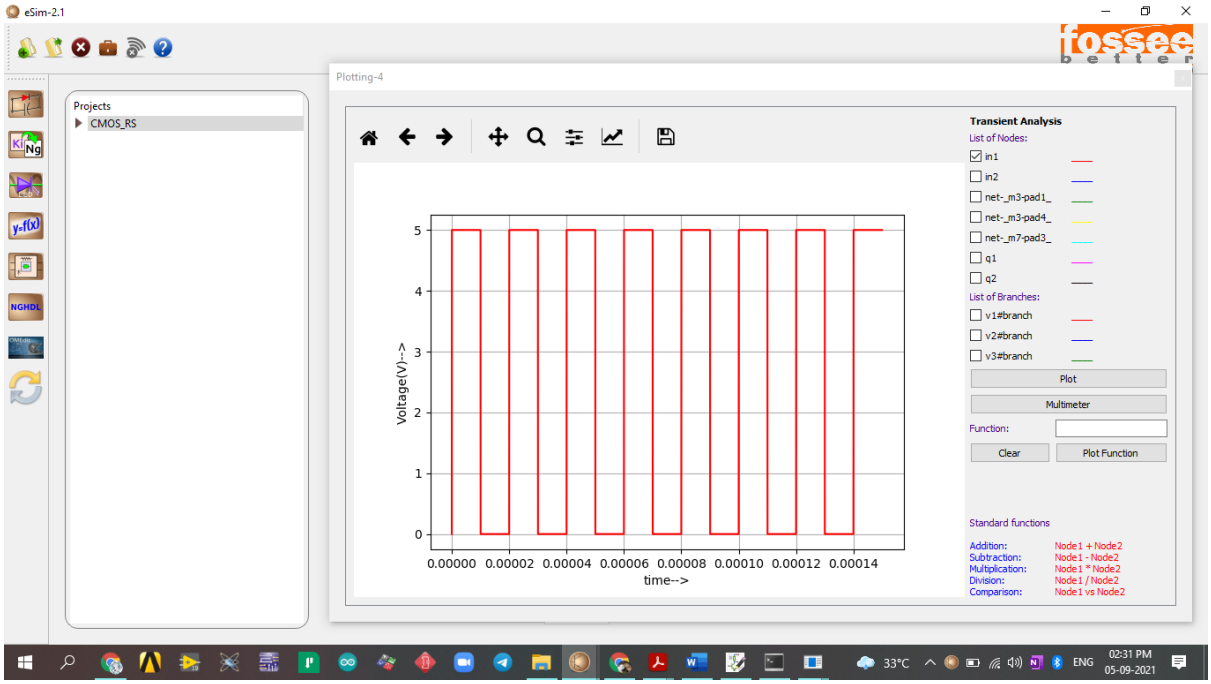

Figure 6: Python Plot Input1

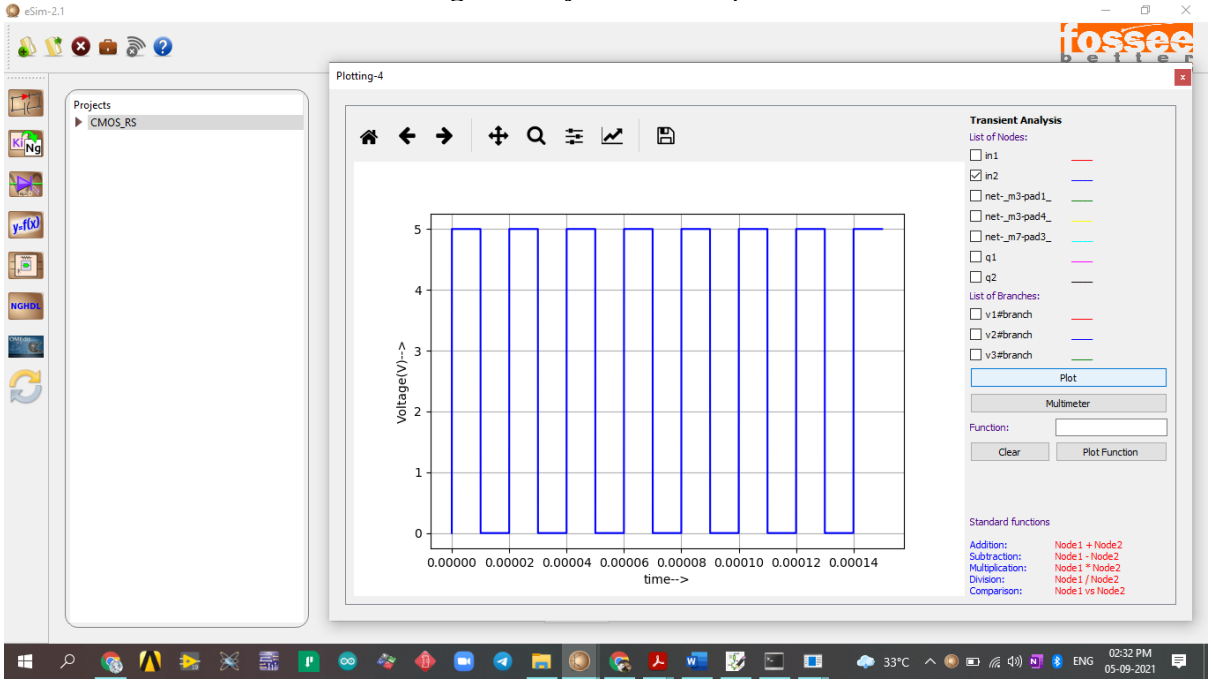

Figure 7: Python Plot Input2

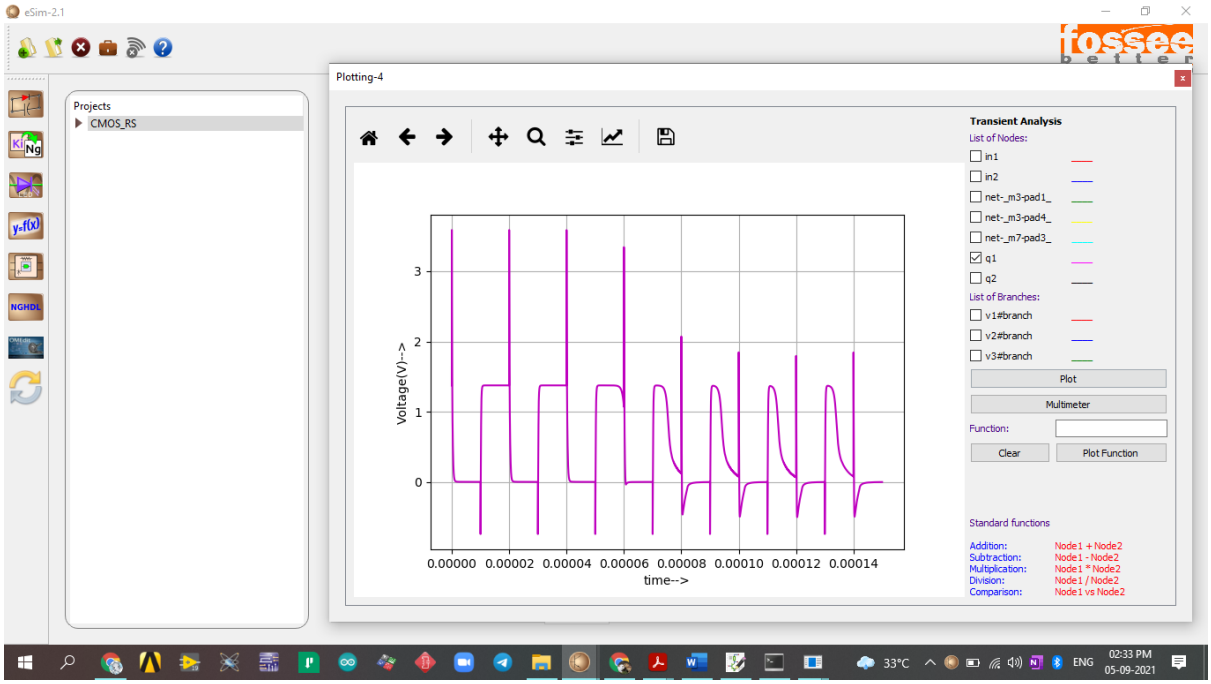

Figure 8: Python Plot Output1

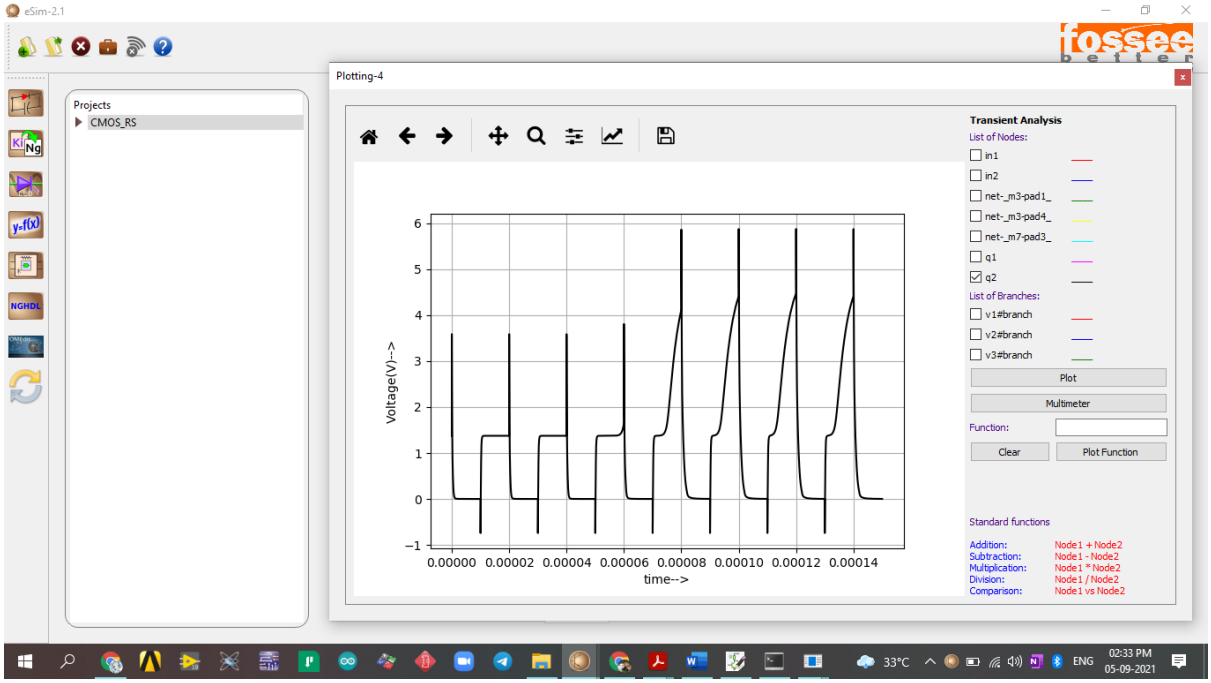

Figure 9: Python Plot Output2

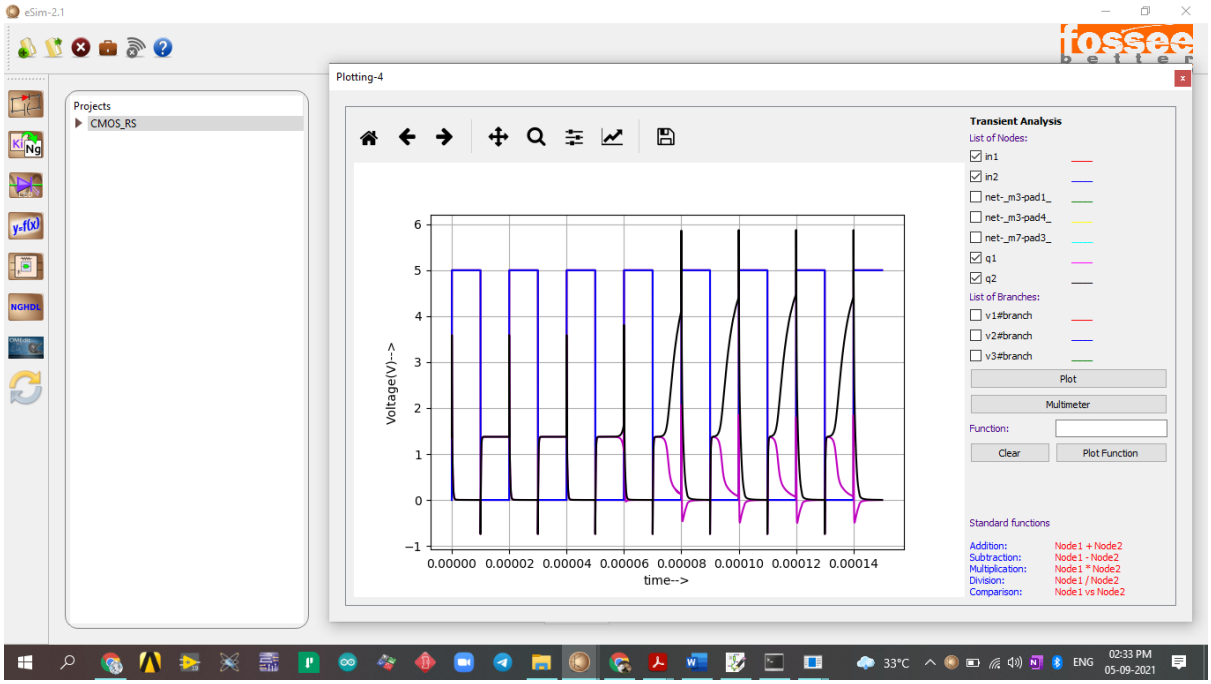

Figure 10: Python Plot CMOS RS Flip-Flop

CONCLUSION:

Thus, we have came to know about the analysis of CMOS RS Flip-Flop in metastable state using eSim and we get the appropriate waveforms.

REFERENCES:

https://ieeexplore.ieee.org/abstract/document/1052671.