

Circuit Simulation Project

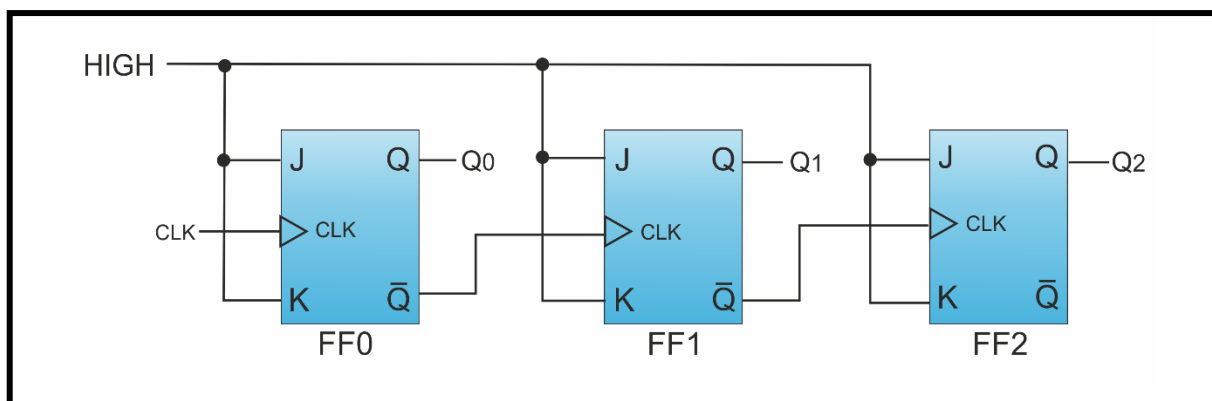
<https://esim.fossee.in/circuit-simulation-project>

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Project Guide: Dr R. Maheswari

Title of the circuit: 3-Bit Asynchronous Up counter

Theory/Description:



In asynchronous up counter with JK Flip-Flops, a clock pulse drives first JK flip-flop FF0. Then its Output drives the second flip flop FF1 and output of second flip-flop drives the third flip-flop FF2. All the J and K inputs are connected to Logic 1.

The 3-bit asynchronous up counter consists of 3 JK flip flops. Overall propagation delay time is the sum of individual delays. Initially all flip flops are reset to produce 0. The output conditions are $Q_2 Q_1 Q_0 = 0 0 0$.

When the first clock pulse is applied, the FF0 changes state on its negative edge. Therefore, $Q_2 Q_1 Q_0 = 0 0 1$. On the negative edge of second clock pulse flip flop FF0 toggles. Its output changes from 1 to 0. This being negative change, FF1 changes state. Therefore, $Q_2 Q_1 Q_0 = 0 1 0$. Similarly, the output of flipflop FF2 changes only when there is negative transition at its input when fourth clock pulse is applied.

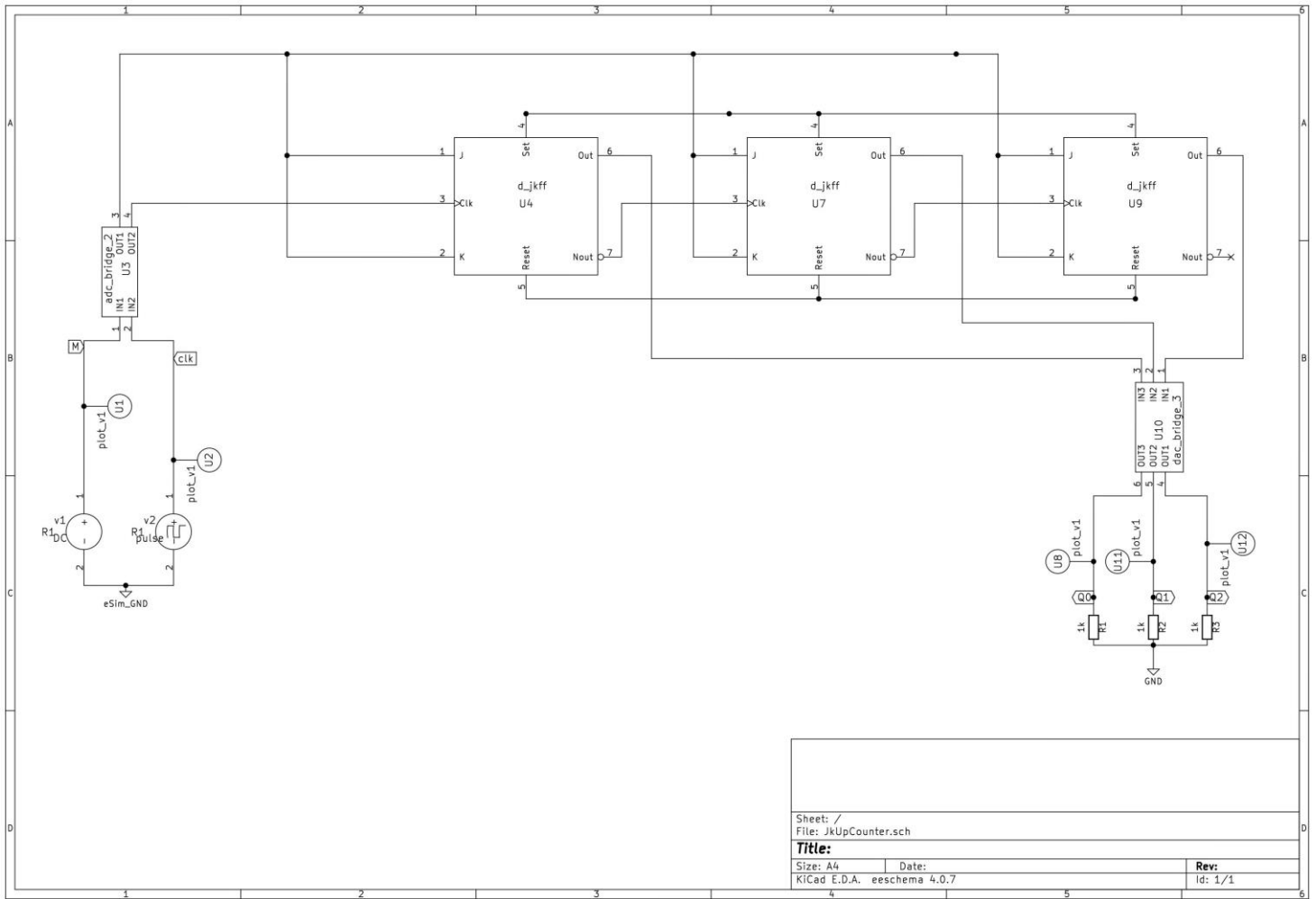
The output of the flip flops is a binary number equivalent to the number of clock pulses received. The output conditions are as shown in the truth table.

Counter State	Q2	Q1	Q0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

e-Sim Required Components

Asynchronous Up counter	
Component	Type
d_jkff	JK flip flop
pulse	Clock
DC	DC Source for logic high

e-Sim Schematic



Sheet: /
File: JkUpCounter.sch

Title:

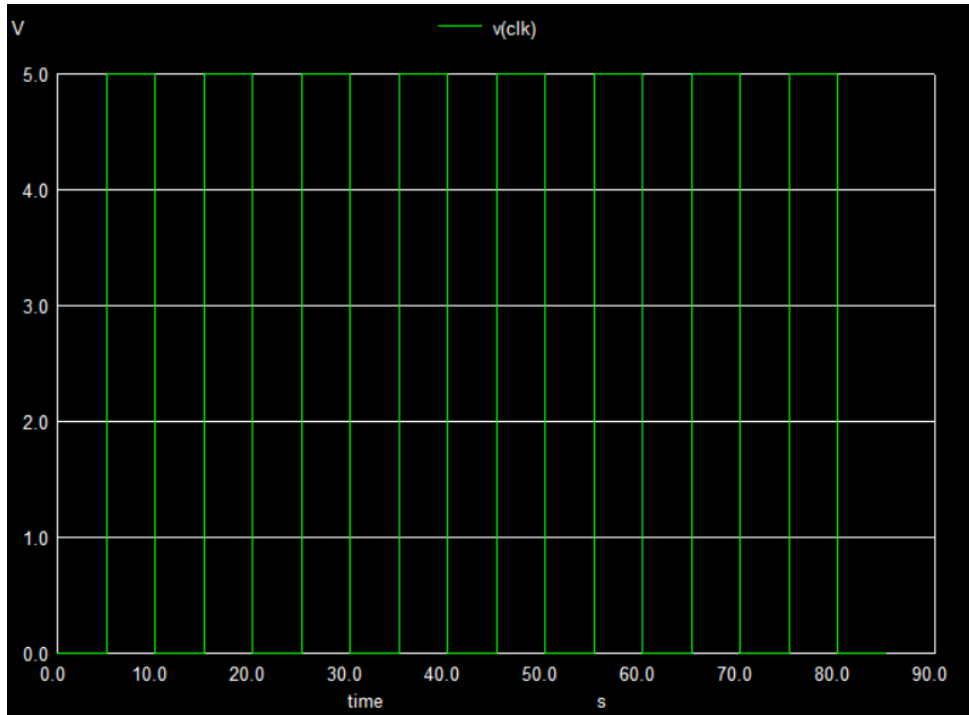
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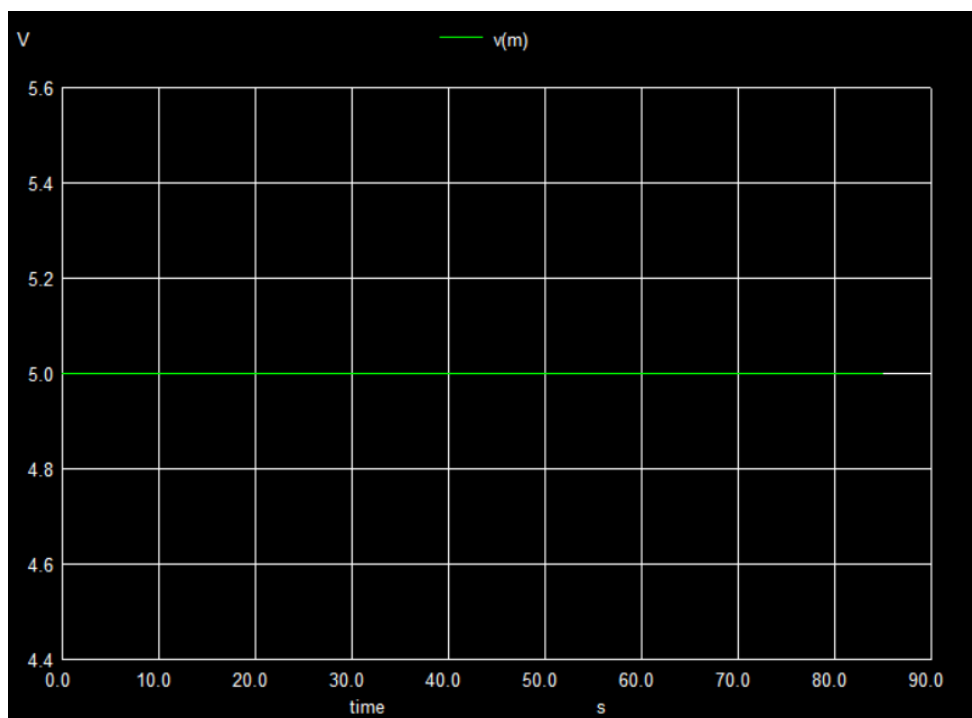
Simulation Result

(i) NG Spice Waveforms:

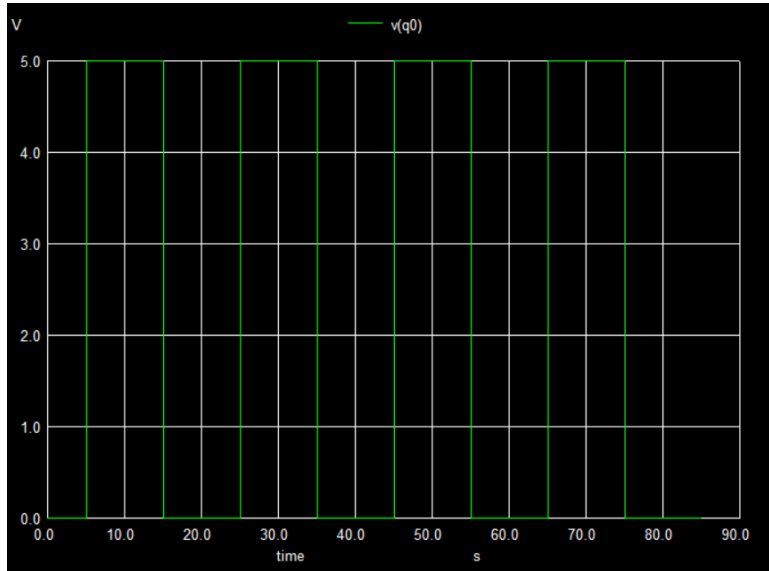
clk (Clock Pulse)



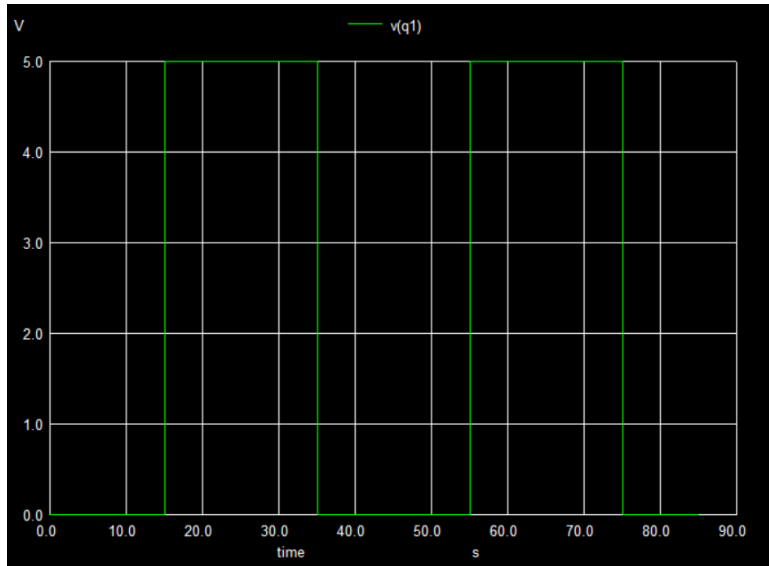
m (Logic High)



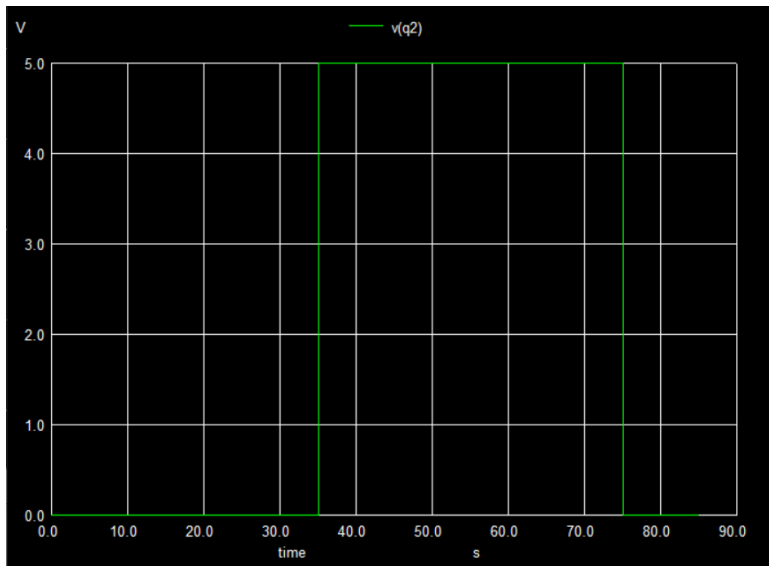
Q₀ (LSB)



Q₁

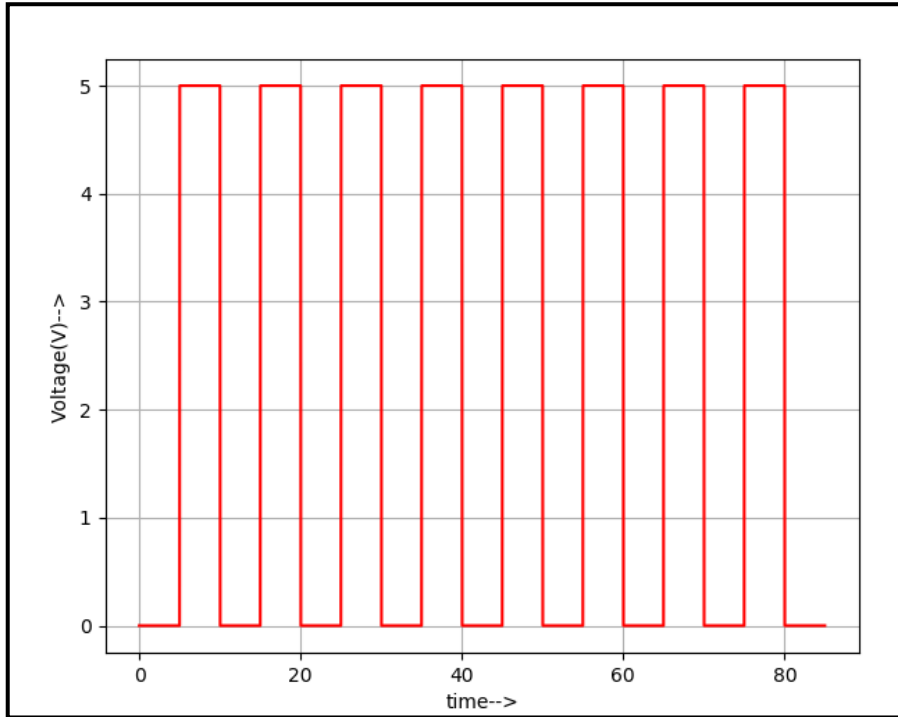


Q₂ (MSB)

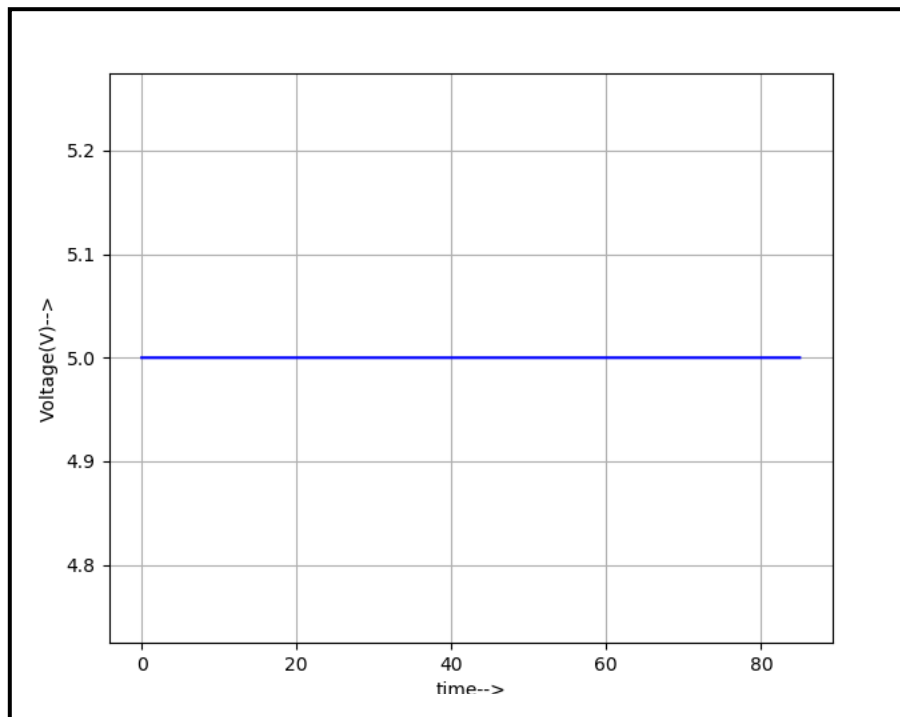


(ii) Python Waveforms (for better visualization)

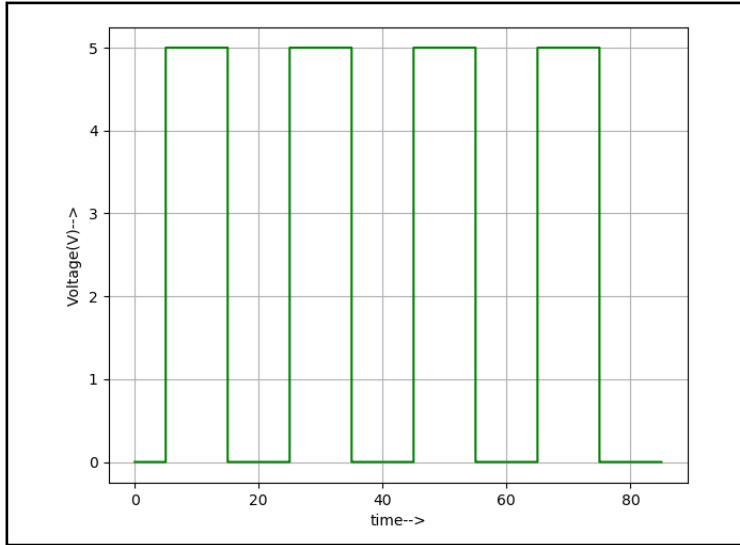
clk



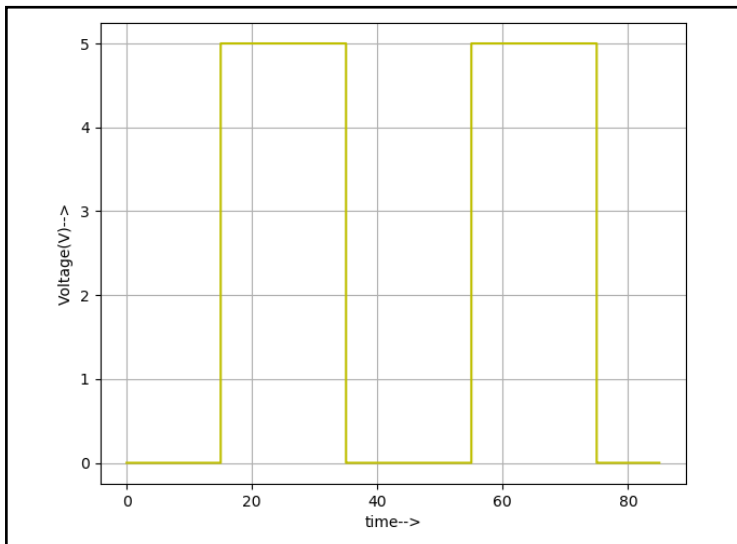
m (Logic High)



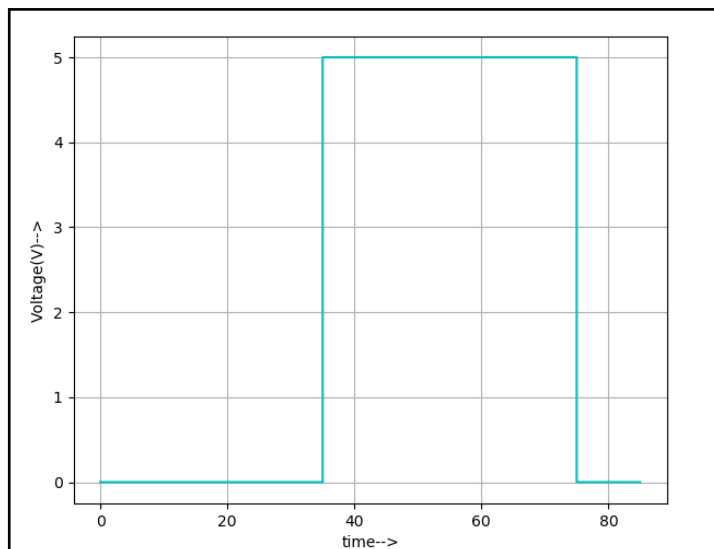
Q₀ (LSB)



Q₁



Q₂ (MSB)



Simulation Parameters for reference:

Transient Analysis

The screenshot shows the 'kicadToNgspice-1' application window with the 'Analysis' tab selected. The 'Source Details' sub-tab is active. Under 'Select Analysis Type', the 'TRANSIENT' checkbox is checked, while 'AC' and 'DC' are unchecked. The 'Transient Analysis' section contains three input fields: 'Start Time' set to 0 with a unit dropdown set to 'Sec'; 'Step Time' set to 10 with a unit dropdown set to 'ms'; and 'Stop Time' set to 85 with a unit dropdown set to 'Sec'. A 'Convert' button is located at the bottom right of the window.

Source Details

The screenshot shows the 'kicadToNgspice-1' application window with the 'Source Details' sub-tab selected. The 'Add parameters for pulse source v2' section contains seven input fields: 'Enter initial value(Volts/Amps):' (0), 'Enter pulsed value(Volts/Amps):' (5), 'Enter delay time (seconds):' (5), 'Enter rise time (seconds):' (0), 'Enter fall time (seconds):' (0), 'Enter pulse width (seconds):' (5), and 'Enter period (seconds):' (10). The 'Add parameters for DC source v1' section contains one input field: 'Enter value(Volts/Amps):' (5). A 'Convert' button is located at the bottom right of the window.

Conclusion:

Hence, designed and verified 3-bit asynchronous up counter using JK flip flops on eSim

References:

<https://learn.circuitverse.org/docs/seq-msi/counters.html>