Circuit Simulation Project

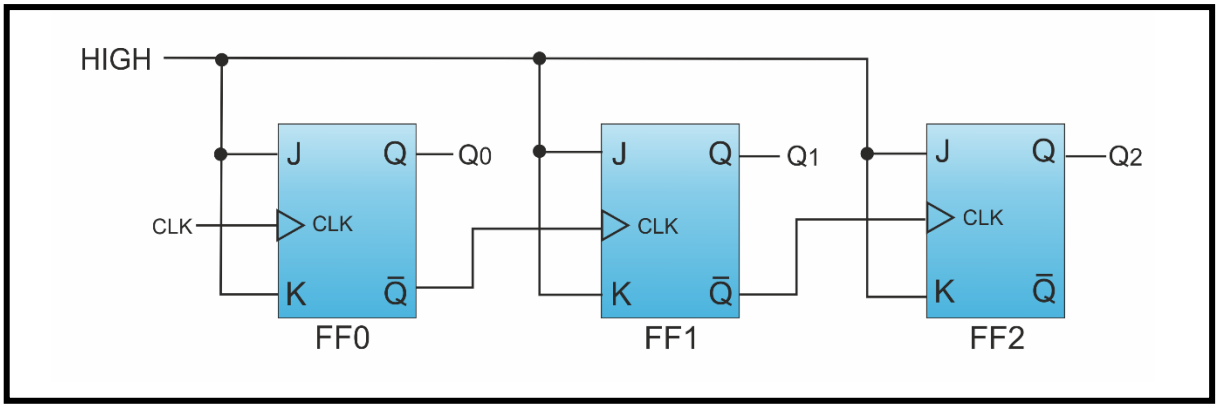
https://esim.fossee.in/circuit-simulation-project

Name of the participant: Gokul Jayan (20BCE1249)

Project Guide: Dr R. Maheswari

Title of the circuit: 3-Bit Asynchronous Up counter

Theory/Description:



In asynchronous up counter with JK Flip-Flops, a clock pulse drives first JK flip-flop FF0. Then its Output drives the second flip flop FF1 and output of second flip-flop drives the third flip-flop FF2. All the J and K inputs are connected to Logic 1.

The 3-bit asynchronous up counter consists of 3 JK flip flops. Overall propagation delay time is the sum of individual delays. Initially all flip flops are reset to produce 0. The output conditions are $\mathbf{Q_2\ Q_1\ Q_0 = 0\ 0\ 0}$.

When the first clock pulse is applied, the FF0 changes state on its negative edge. Therefore, $\mathbf{Q_2\ Q_1\ Q_0 = 0\ 0\ 1}$. On the negative edge of second clock pulse flip flop F0 toggles. Its output changes from 1 to 0. This being negative change, FF1 changes state. Therefore, $\mathbf{Q_2\ Q_1\ Q_0 = 0\ 1\ 0}$. Similarly, the output of flipflop FF2 changes only when there is negative transition at its input when fourth clock pulse is applied.

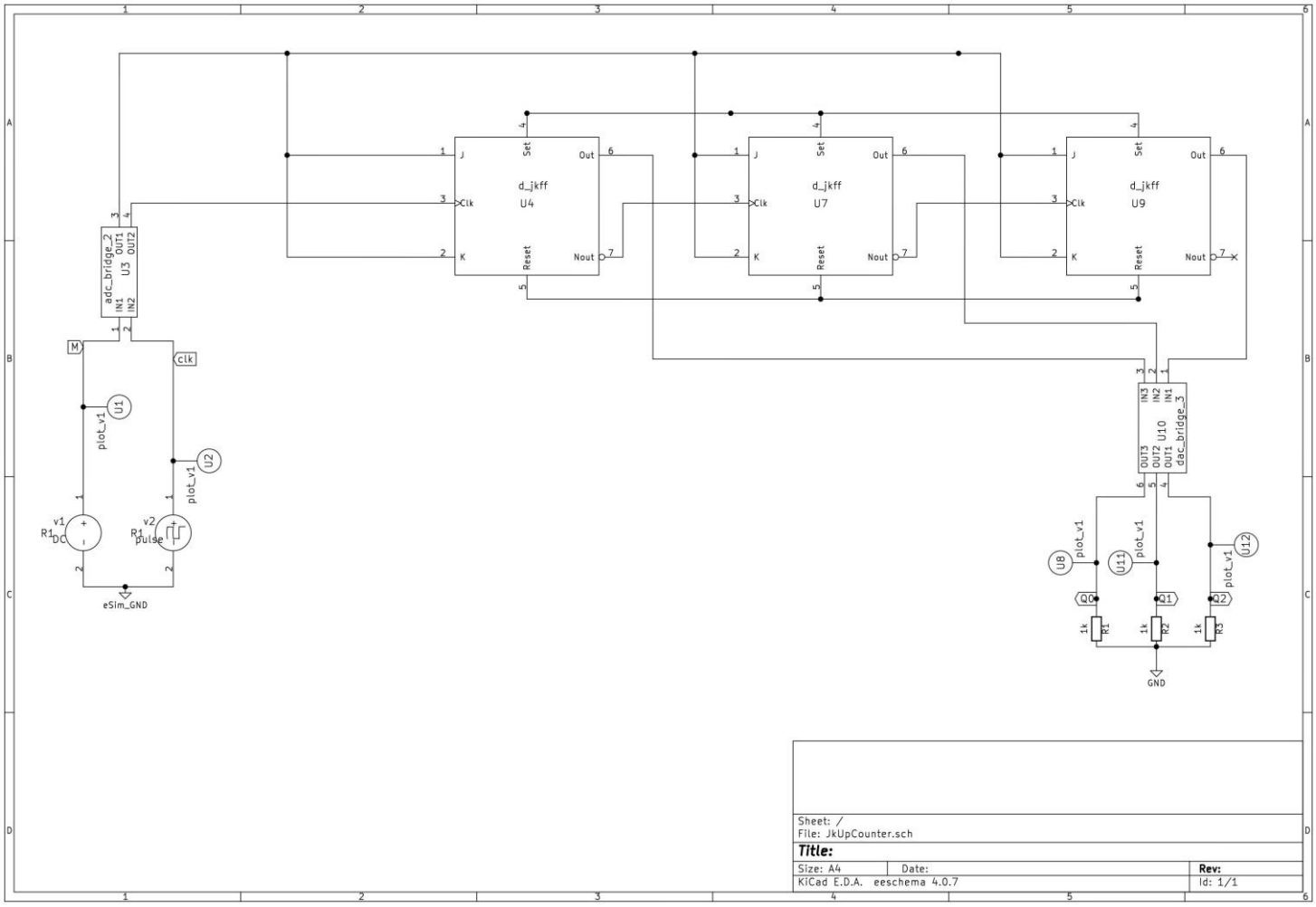
The output of the flip flops is a binary number equivalent to the number of clock pulses received. The output conditions are as shown in the truth table.

Counter State	Q2	Q1	Q0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

e-Sim Required Components

Asynchronous Up counter	
Component	**Type**
d_jkff	JK flip flop
pulse	Clock
DC	DC Source for logic high

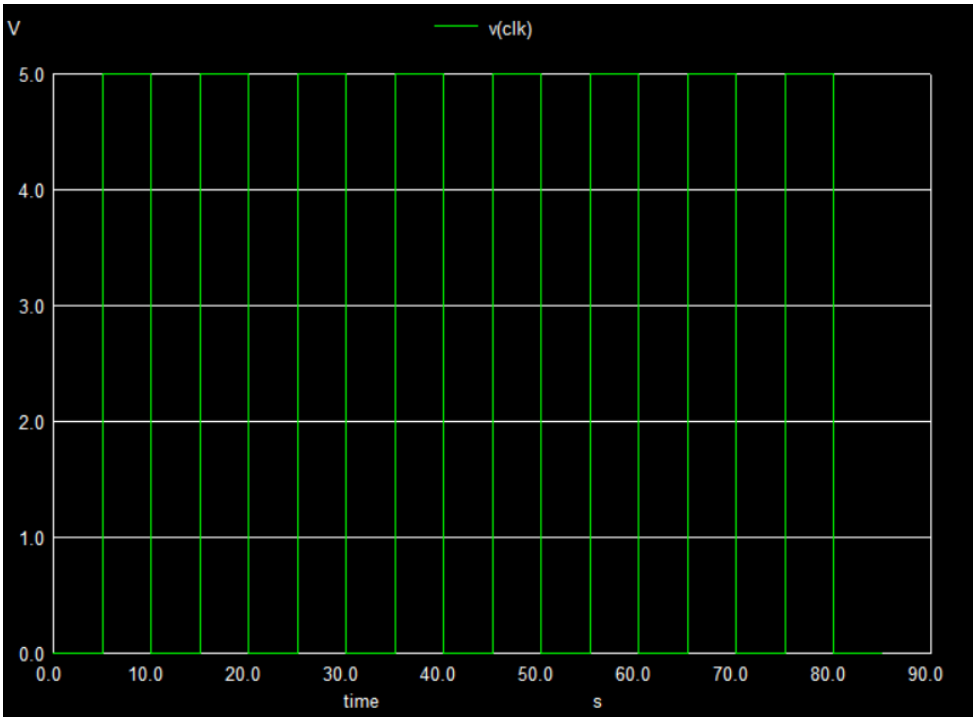
e-Sim Schematic



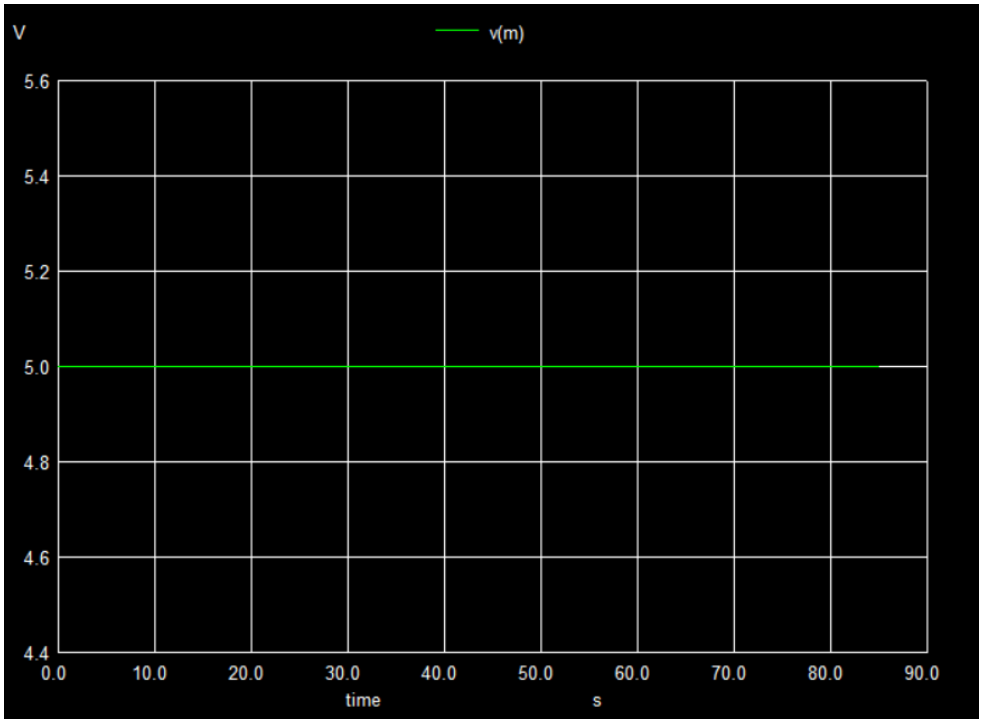
Simulation Result

(i) NG Spice Waveforms:

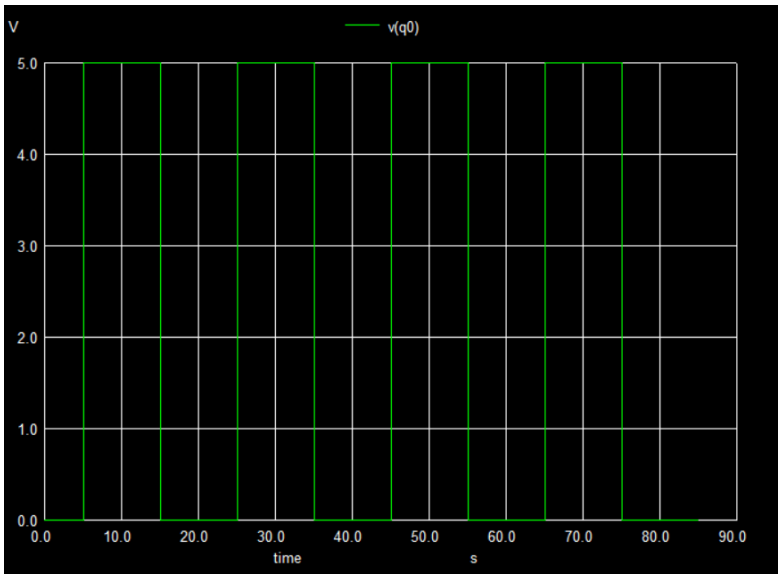
clk (Clock Pulse)



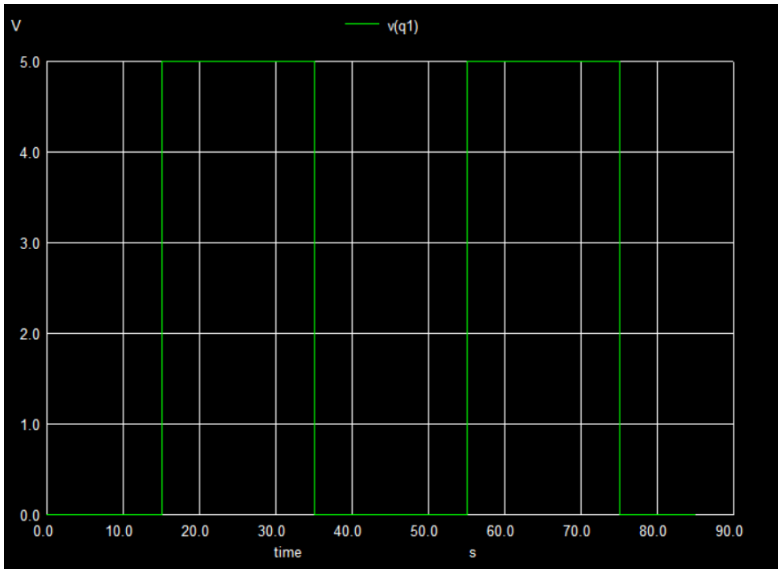
m (Logic High)



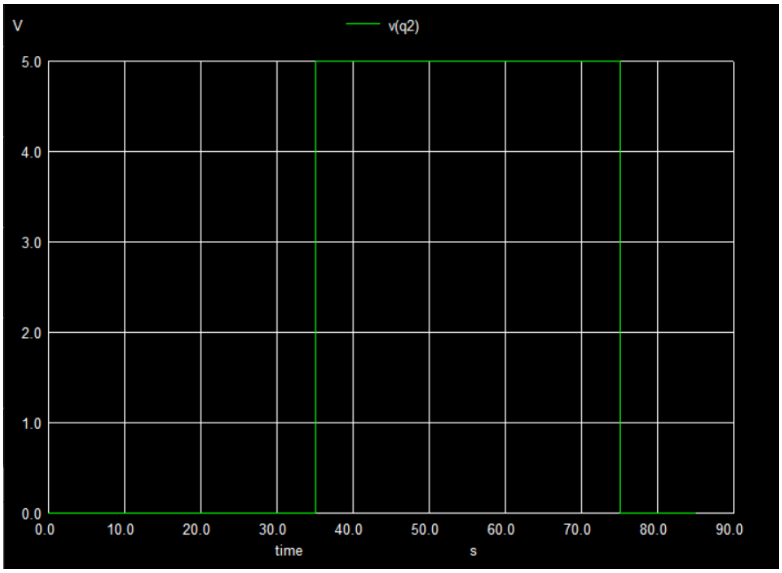
Q_0 (LSB)



Q_1

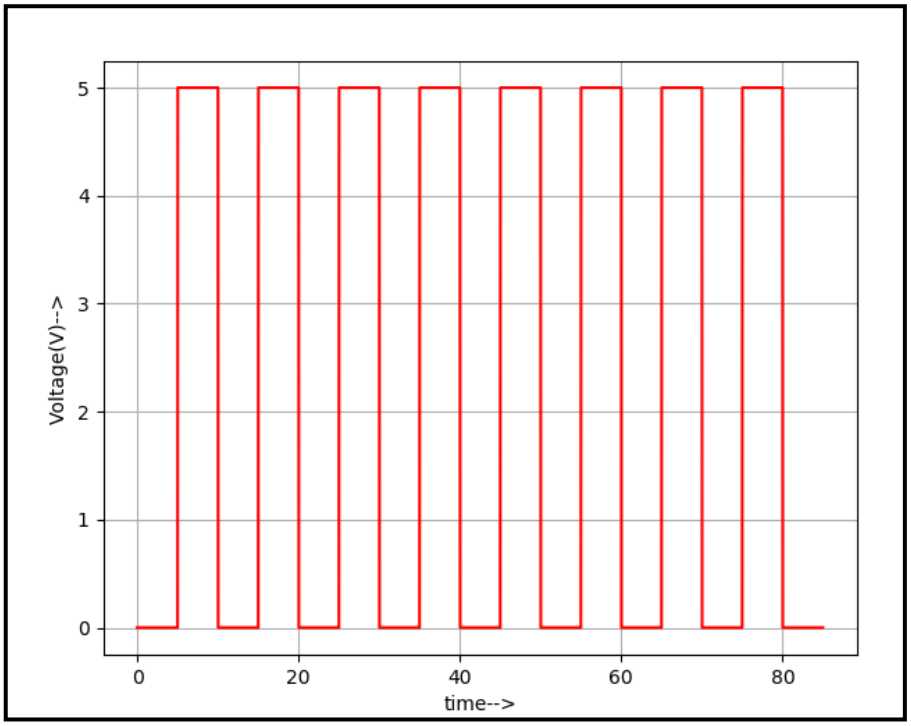


Q_2 (MSB)

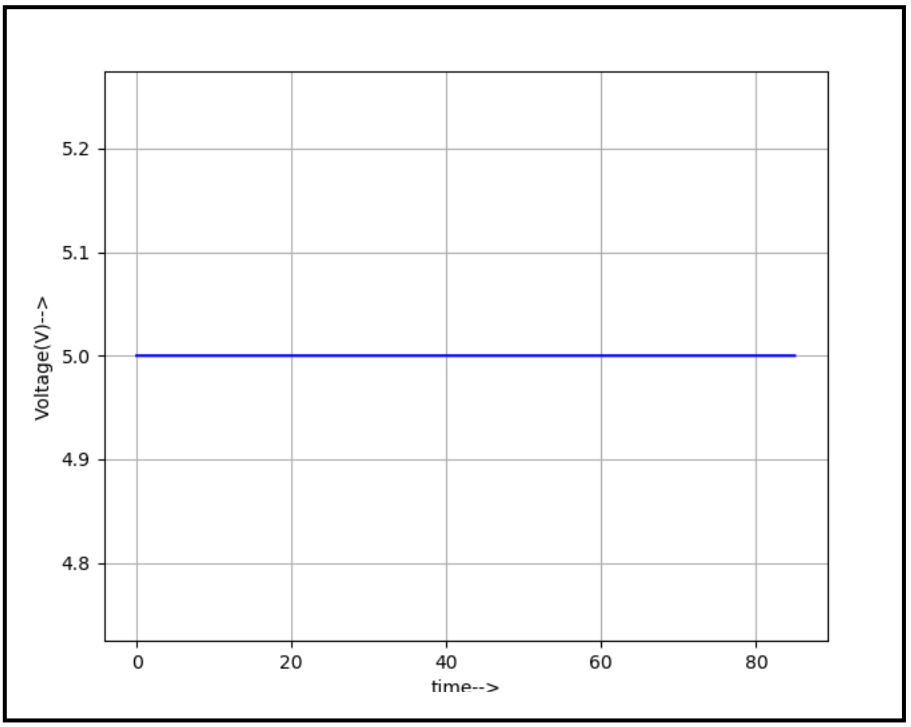


(ii) **Python Waveforms** (for better visualization)

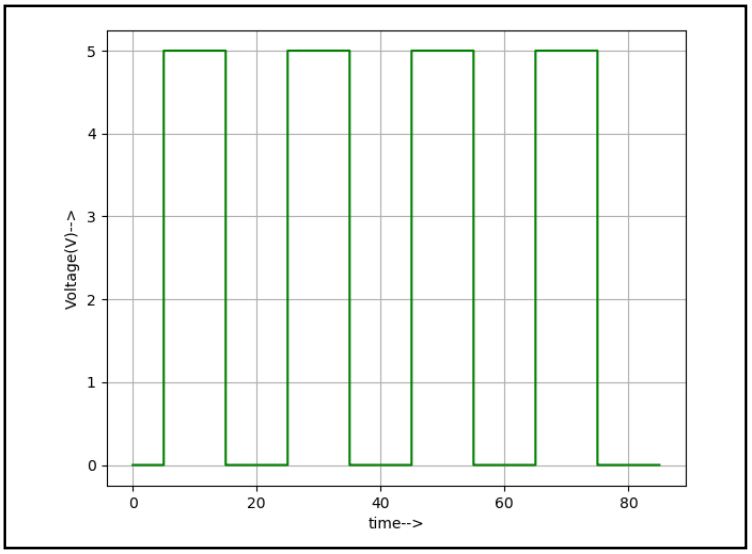
clk



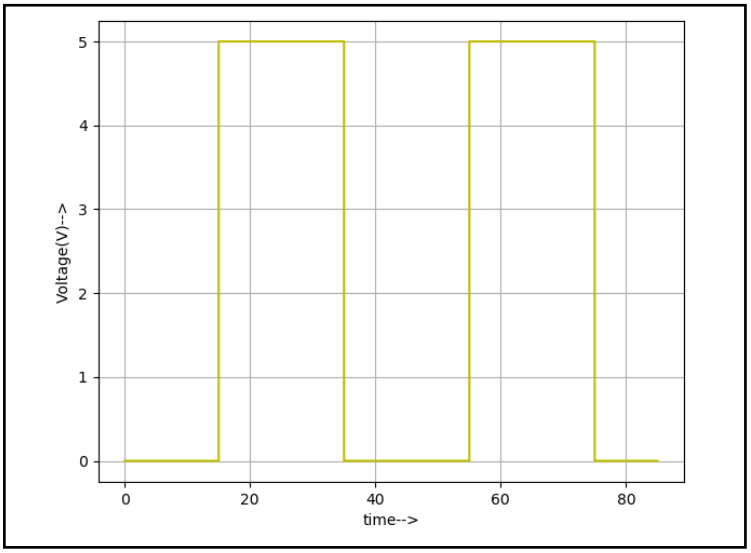
m (Logic High)



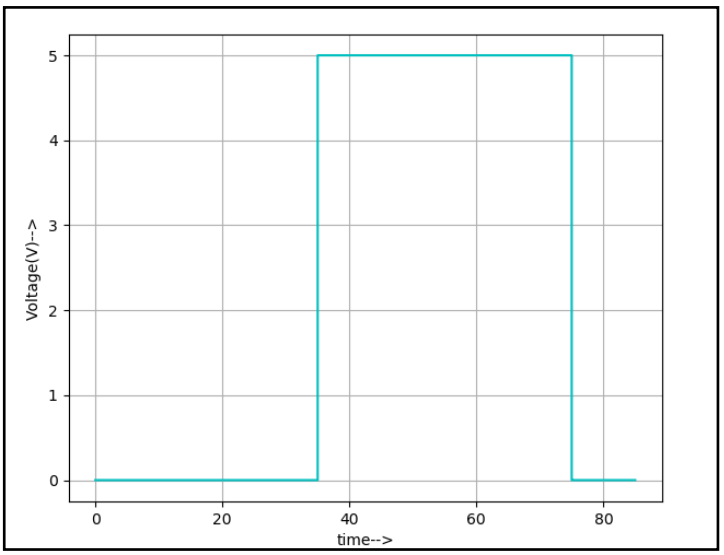
Q_0 (LSB)



Q_1

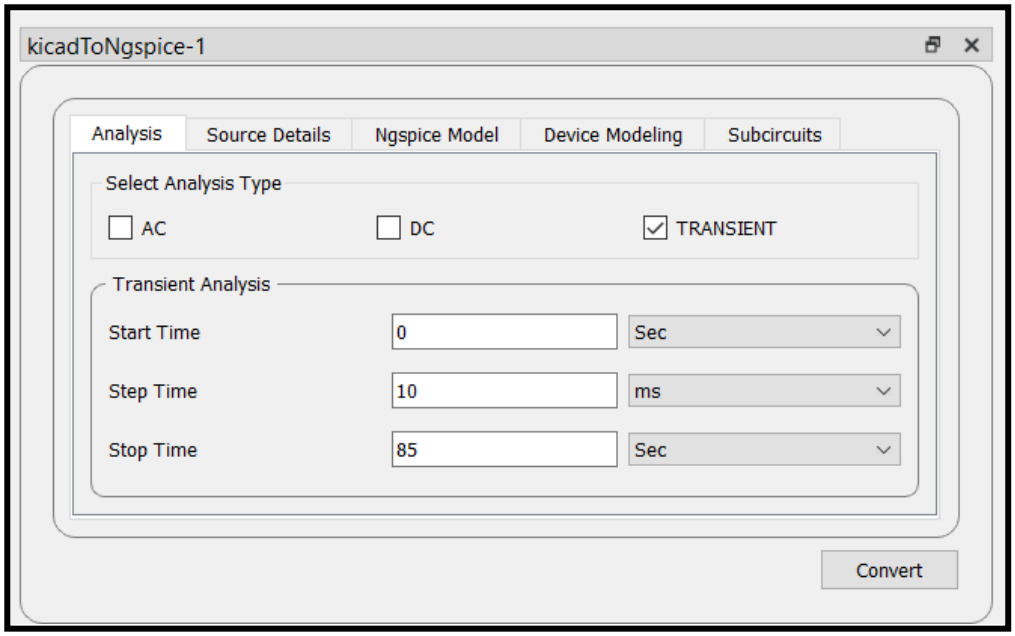


Q_2 (MSB)

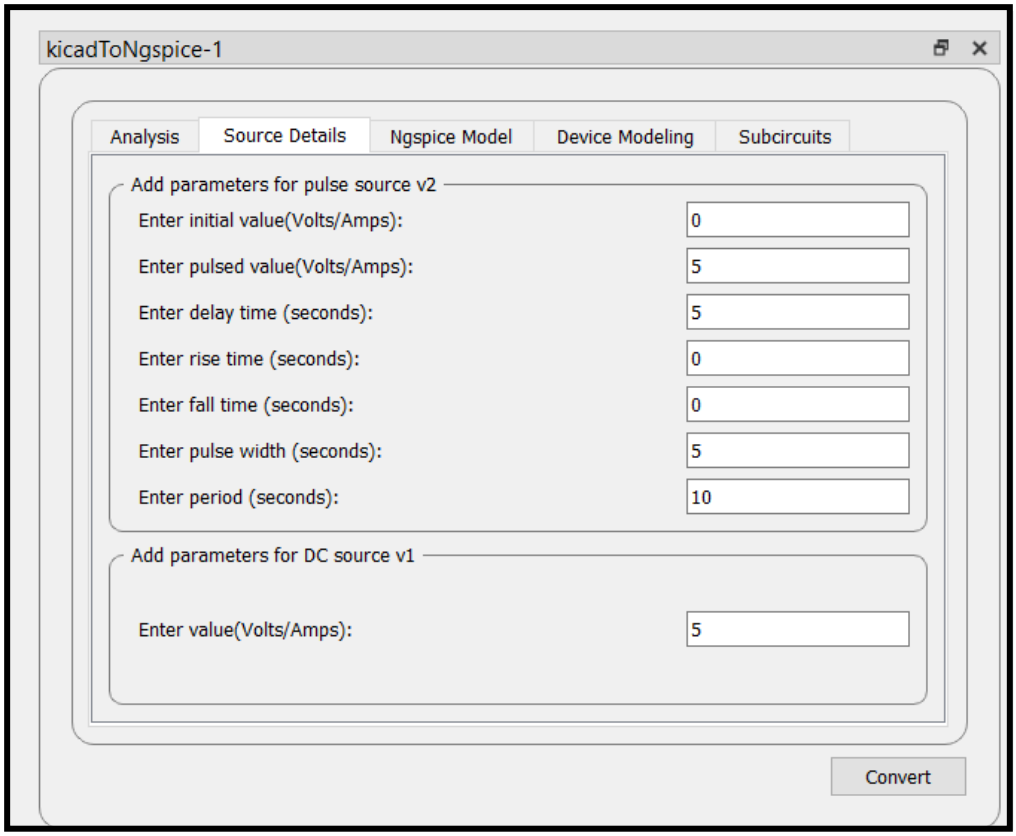


Simulation Parameters for reference:

Transient Analysis



Source Details



Conclusion:

Hence, designed and verified 3-bit asynchronous up counter using JK flip flops on eSim

References:

https://learn.circuitverse.org/docs/seq-msi/counters.html