Title of the experiment:

Conventional Cmos Full Adder Circuit

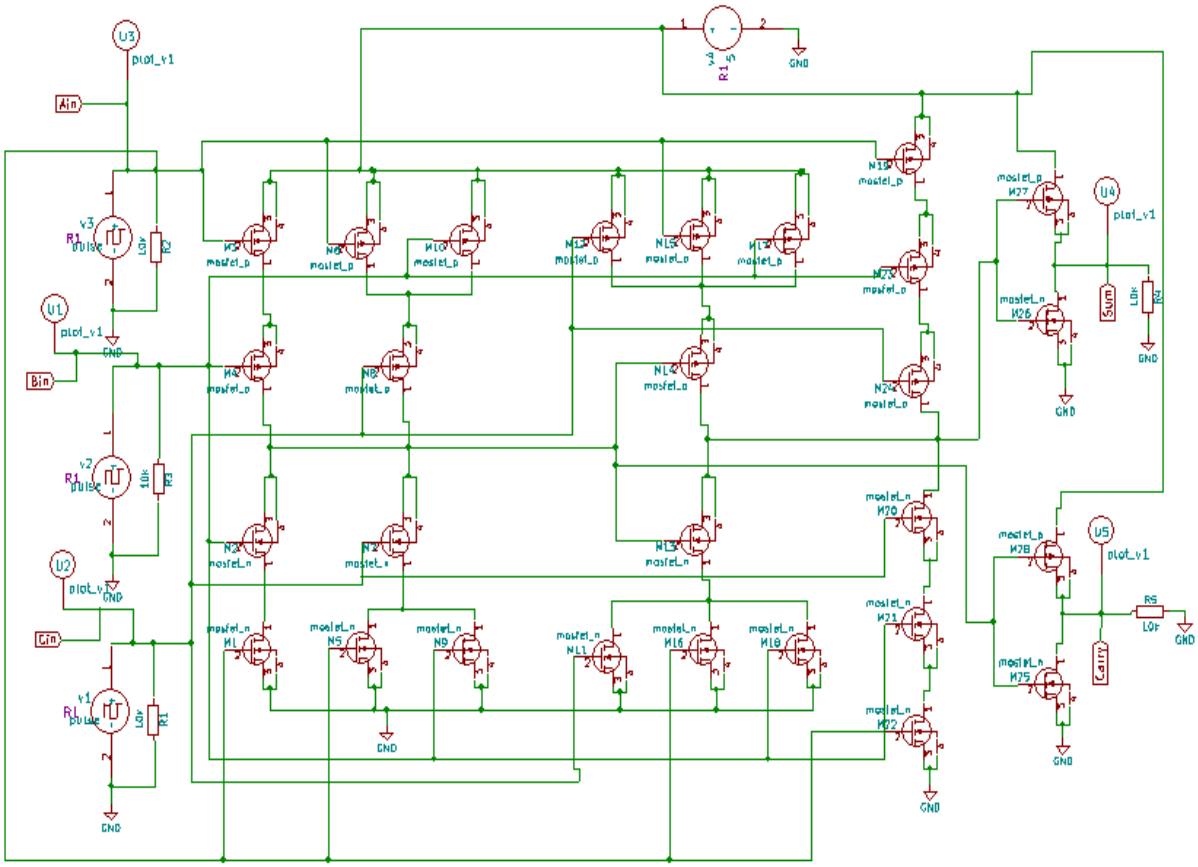
Theory:

In this paper a new low power and high performance adder cell using a new design style called “Bridge” is proposed. The bridge design style enjoys a high degree of regularity, higher density than conventional CMOS design style as well as lower power consumption, by using some transistors, named bridge transistors.

Index Terms—CMOS Circuit, VLSI, Full adder, Bridge style

Schematic Diagram:

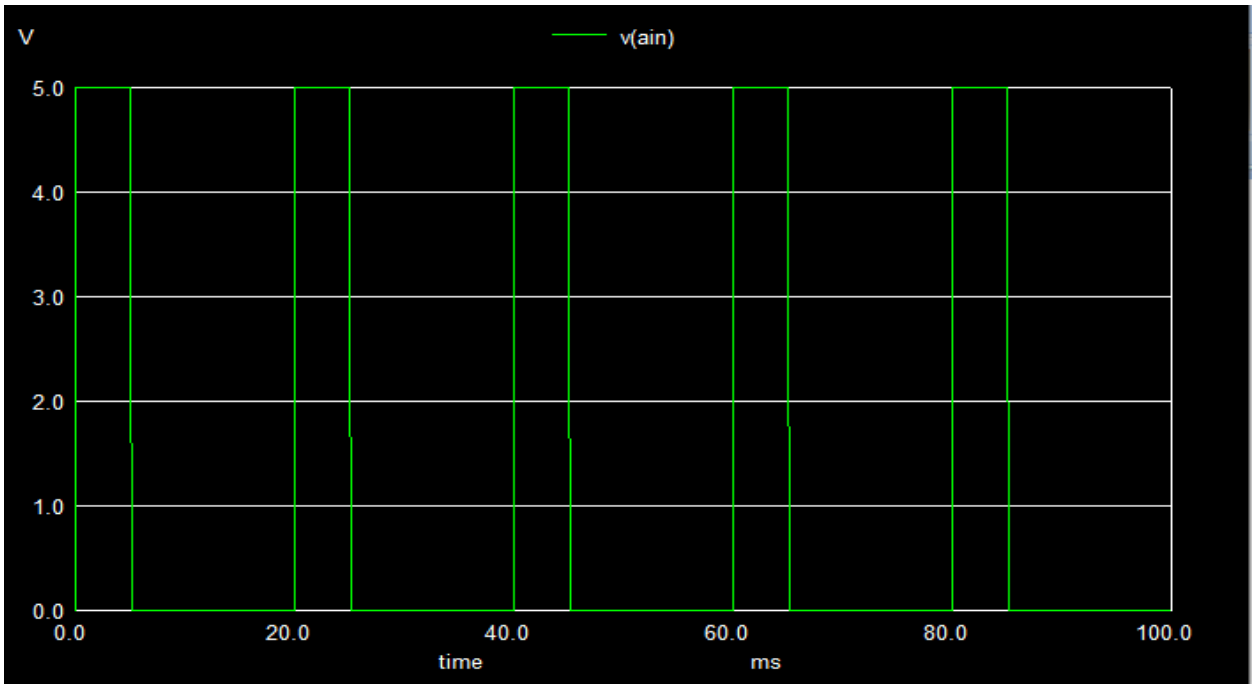
The circuit schematic of CMOS full adder circuit in eSim is as shown below:



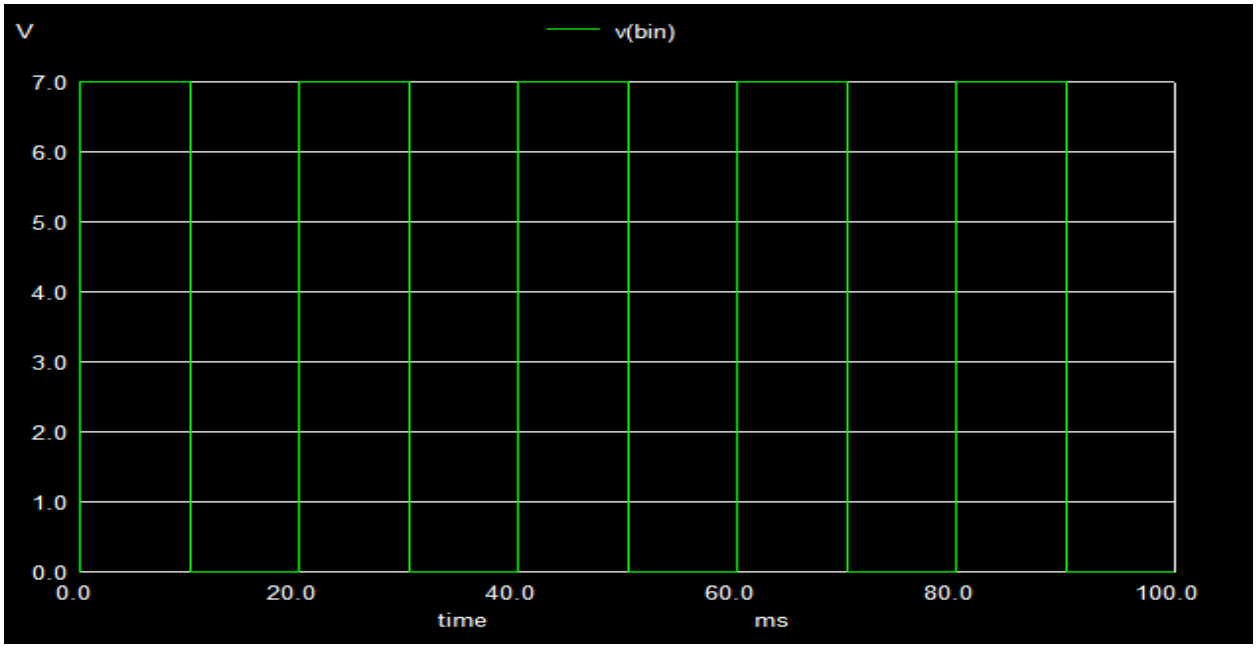
Simulation Results :

1. Ngspice Plots

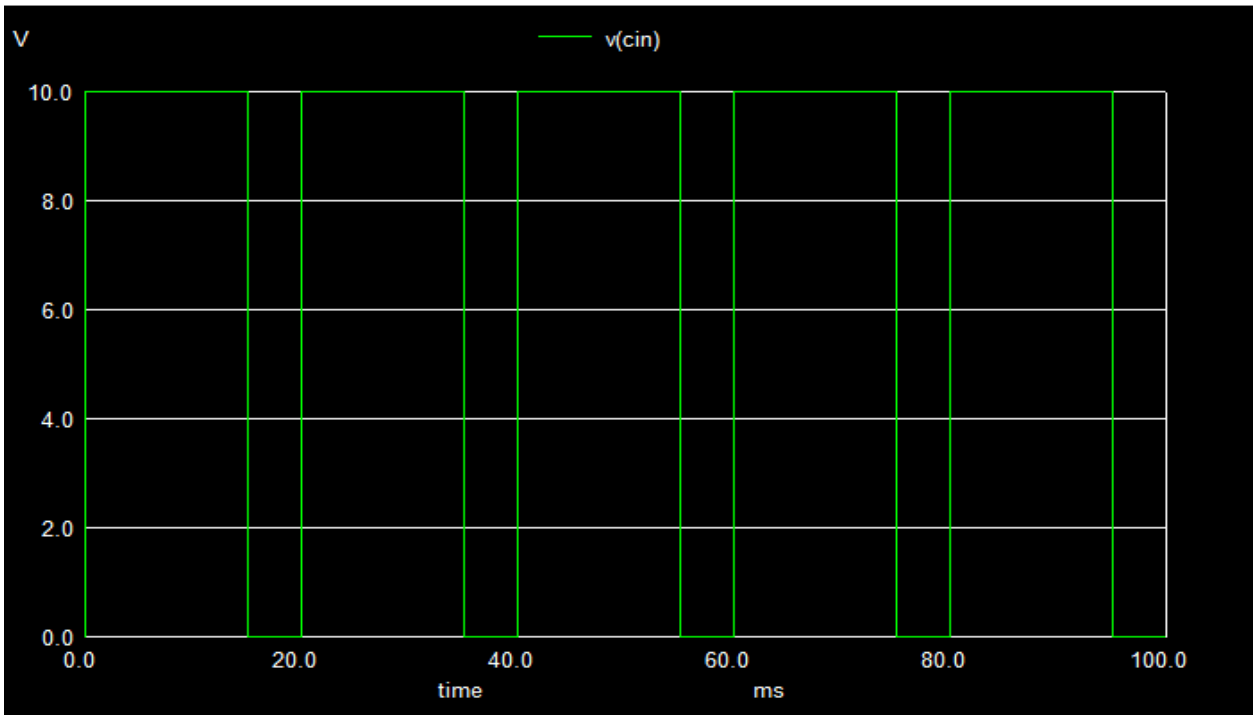
- Ngspice input plot (a)



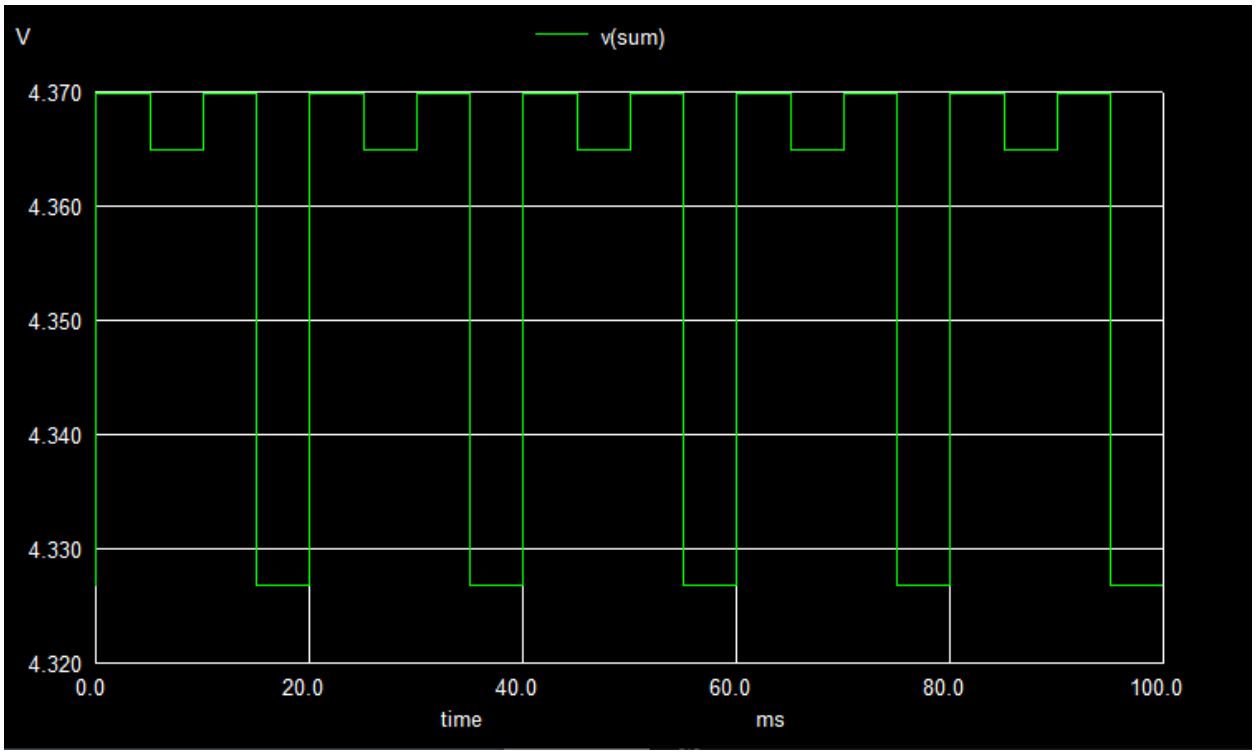
- Ngspice input plot (b)



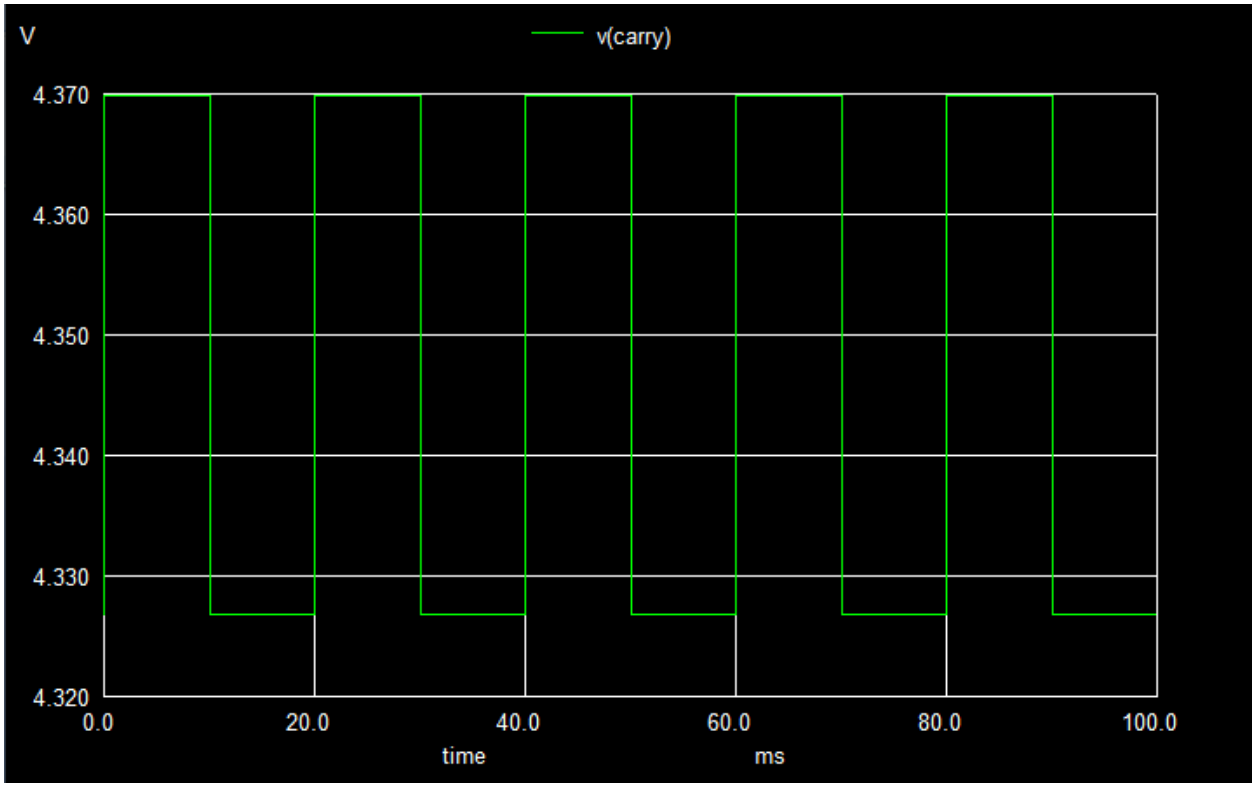
❖ Ngspice input plot (c)



❖ Ngspice output sum plot

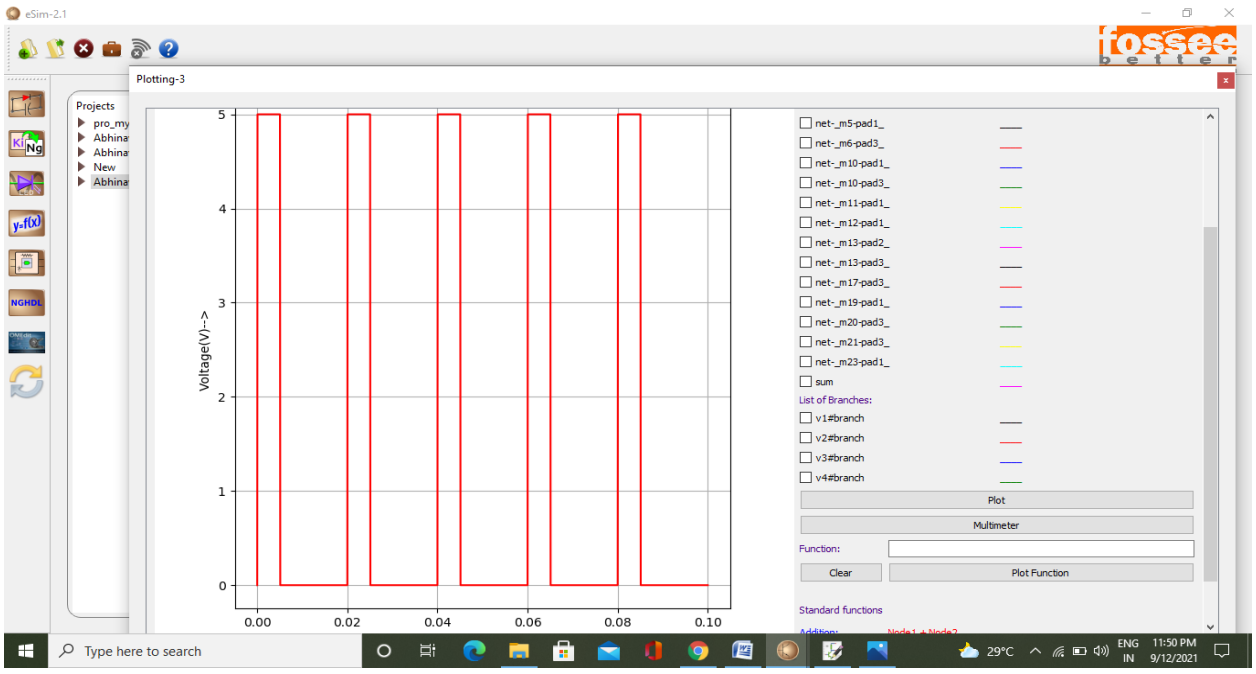


❖ Ngspice output carry plot

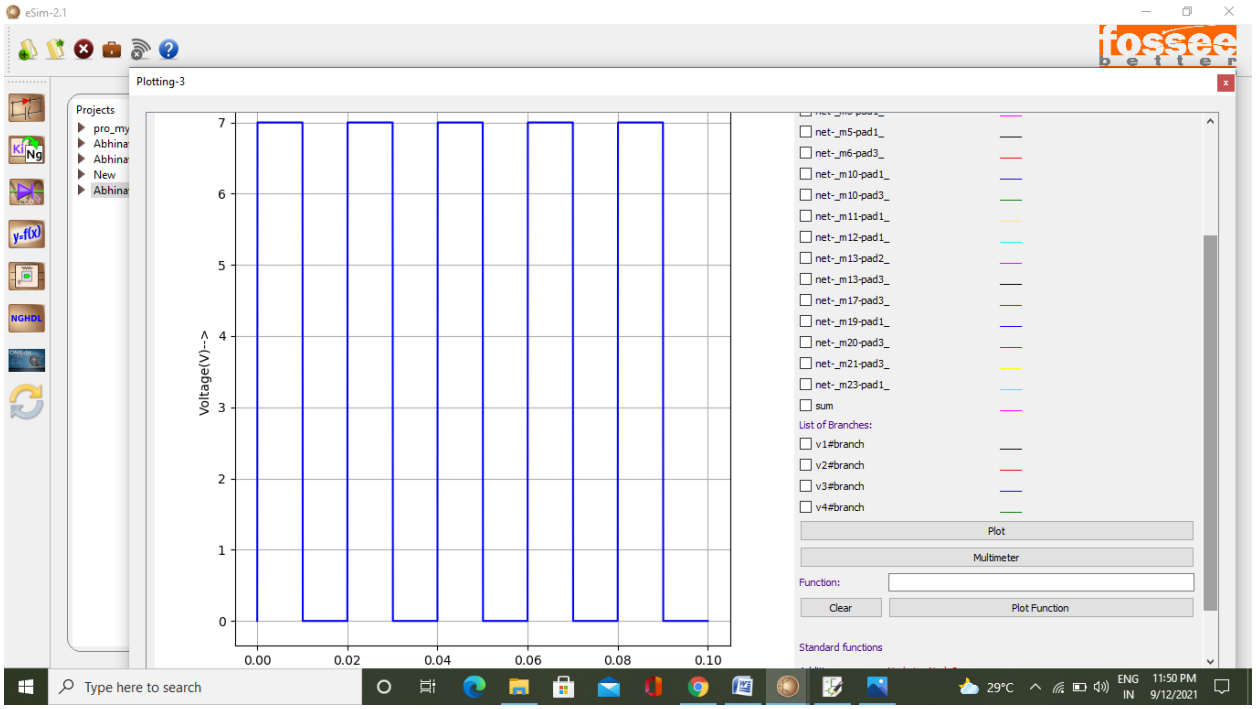


2. Python Plots:

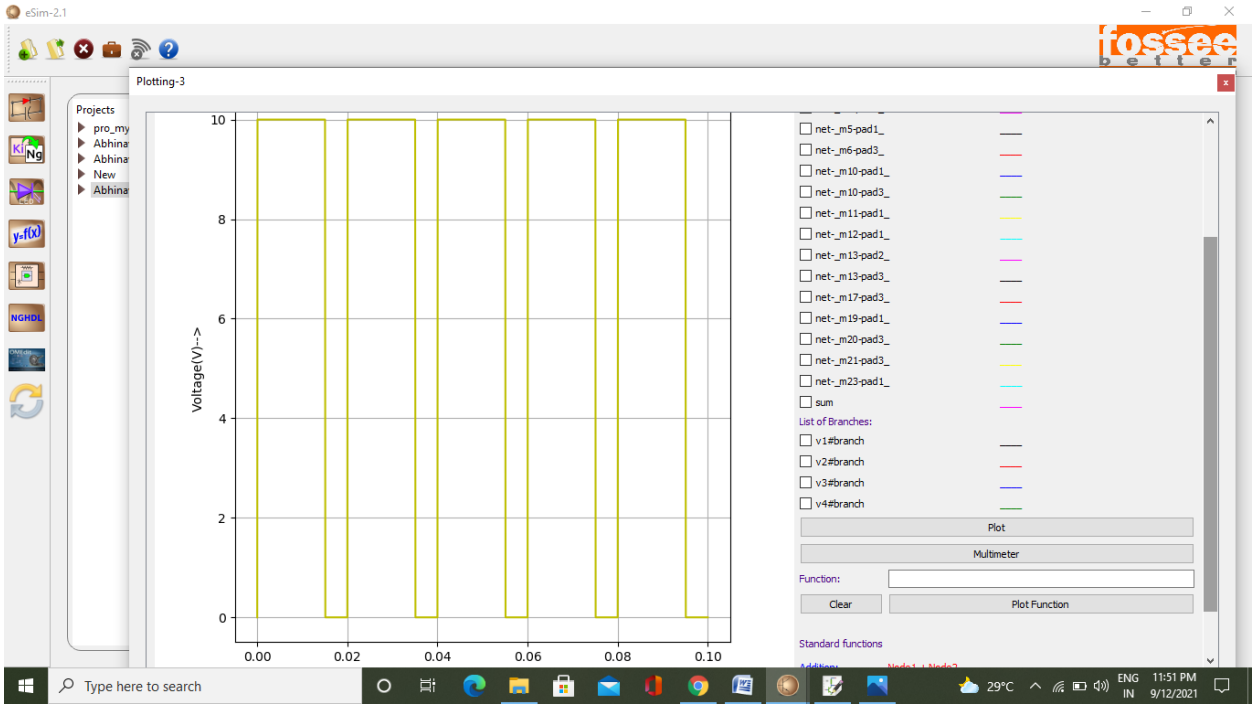
❖ Python plot input (a)



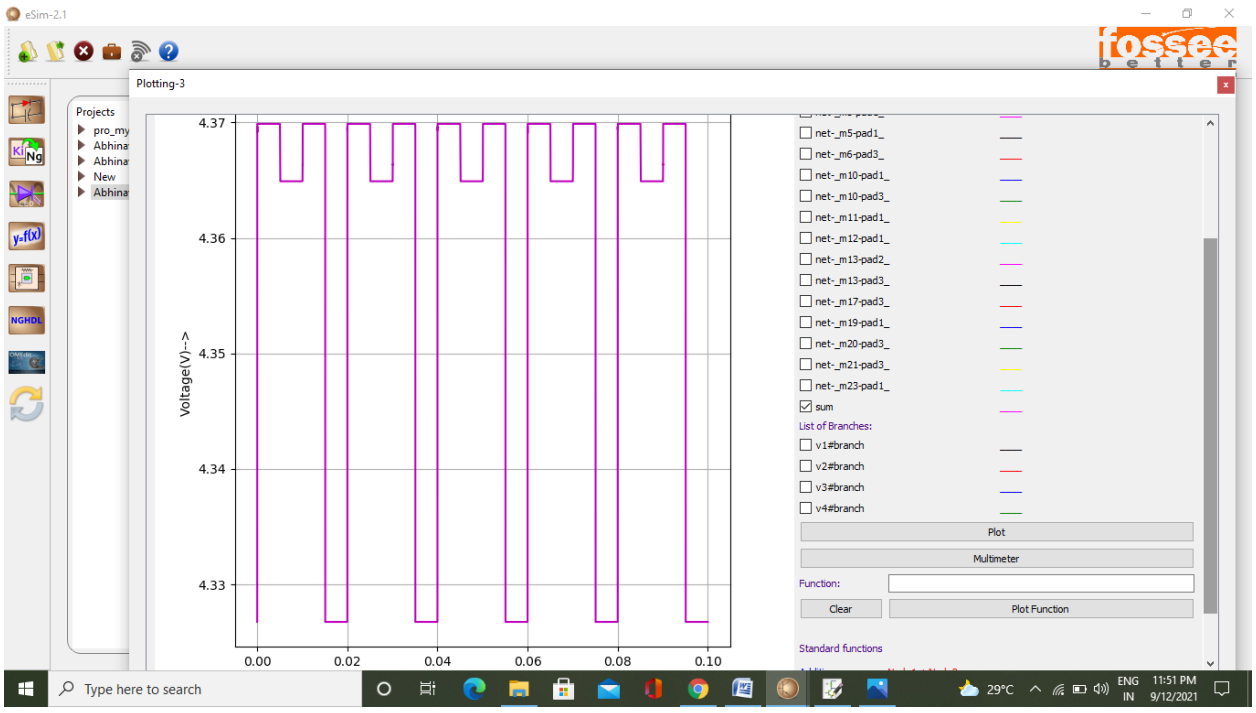
❖ Python plot input (b)



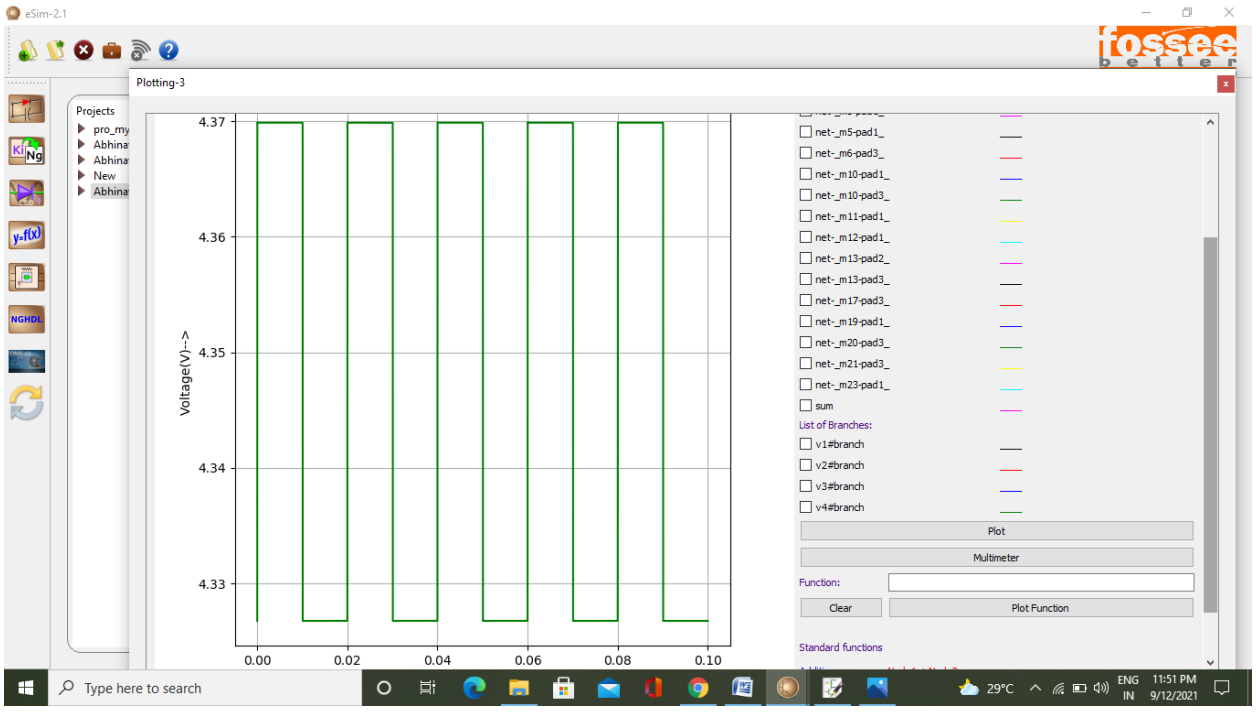
❖ Python plot input (c)



❖ Python plot output sum



- Python plot output carry



Conclusion :

Thus, we have studied CMOS full adder circuit using eSim and we get the appropriate waveforms.

References :

https://www.researchgate.net/publication/249567605