Title of the experiment:

**12T Full Adder Design**

## Theory:

The 1-bit Full Adder circuit is a vital segment in the plan of use explicit coordinated circuits. It has a novel low-power multiplexer-based 1-bit full adder that utilizes 12 transistors (MBA-12T). Notwithstanding diminished progress movement and charge reusing ability, this circuit has no immediate associations with the force supply hubs, driving to a noticeable decrease in short-current force utilization. The new viper has more than 26% in power investment funds over standard 28-semiconductor CMOS, and it devours 23% less power than 10-semiconductor adders and is operates 64% faster. The touchy development in PCs, versatile individual correspondence frameworks, and the advancement of the contracting innovation.

## Schematic Diagram:

The circuit schematic of 12T Full Adder Design in eSim is as shown below:

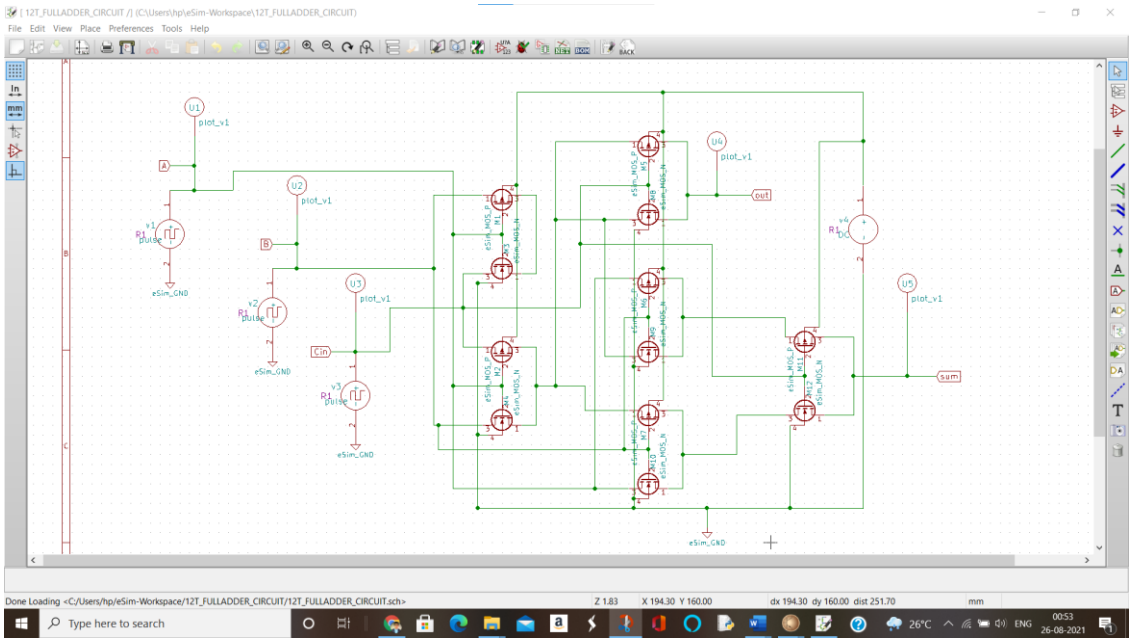


Figure 1: 12T Full Adder Circuit

Simulation Results:

1. Ngspice Plots

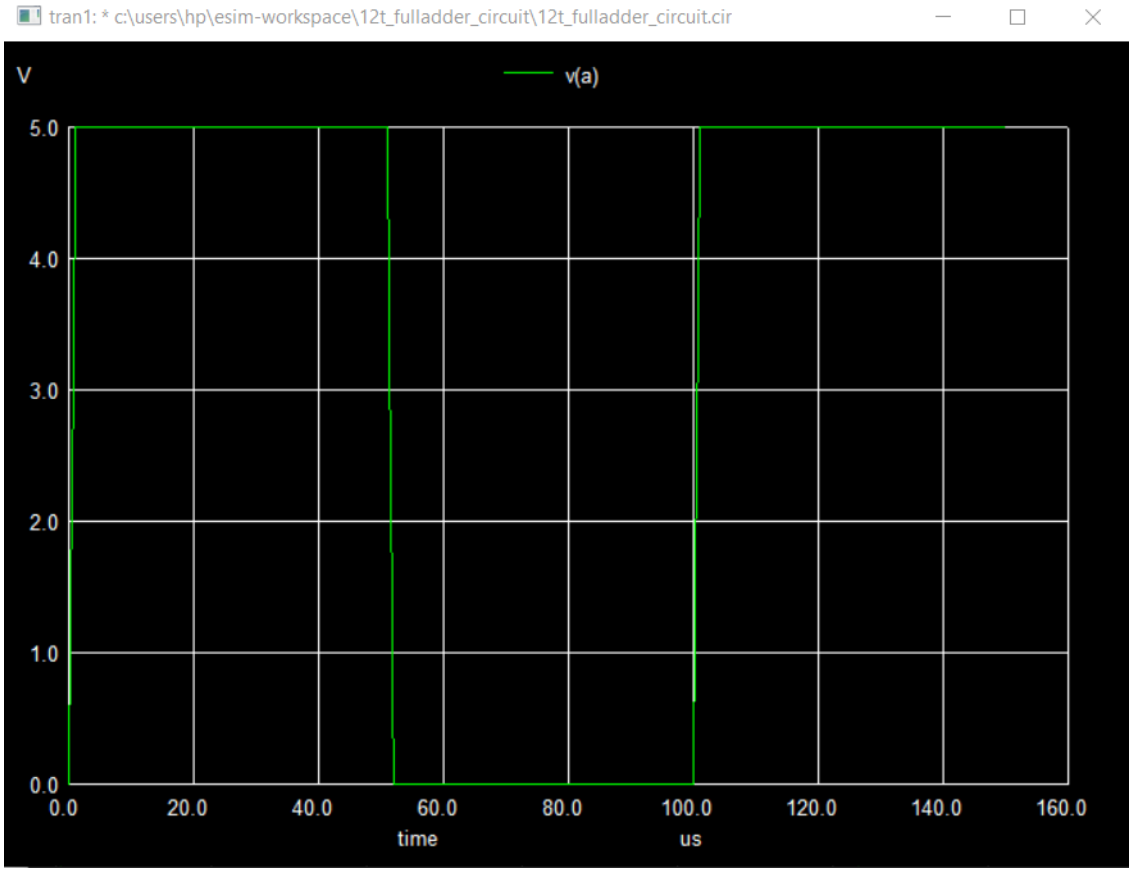


Figure 2: Ngspice plot Input a

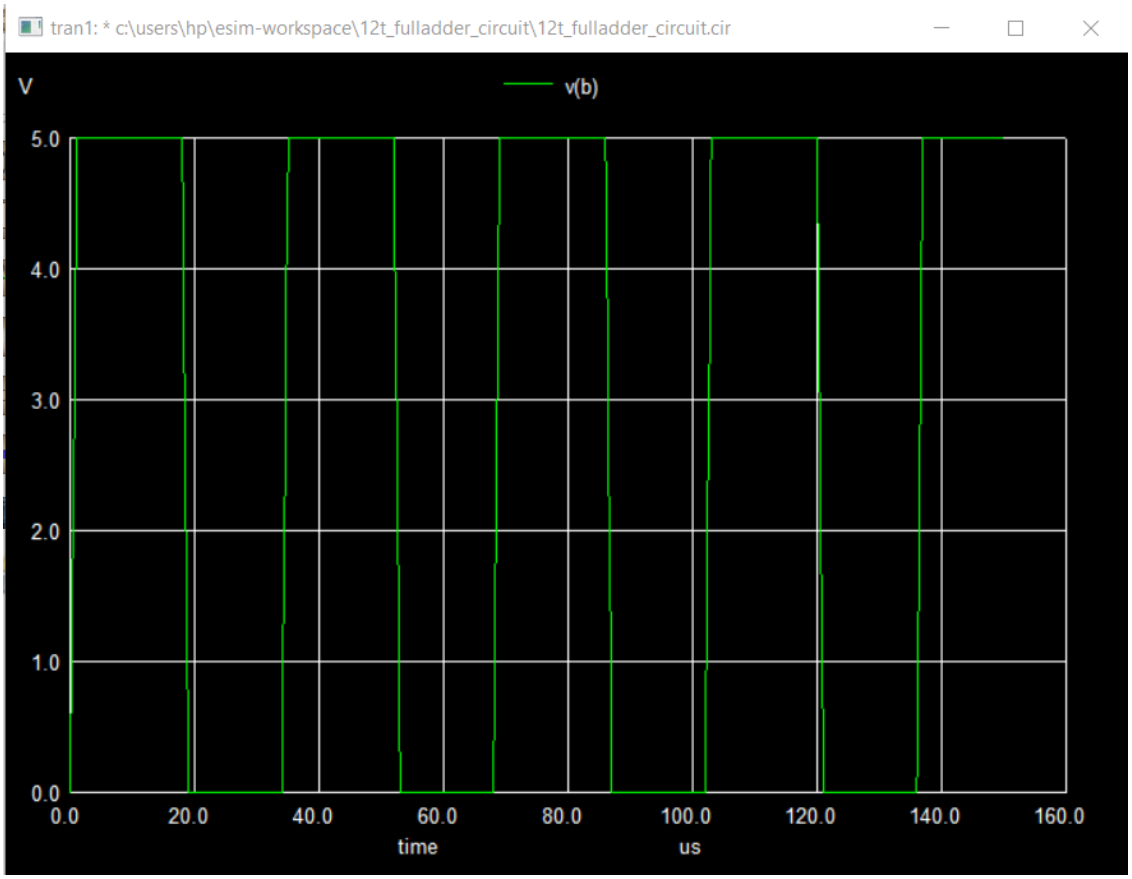


Figure 3: Ngspice plot Input b

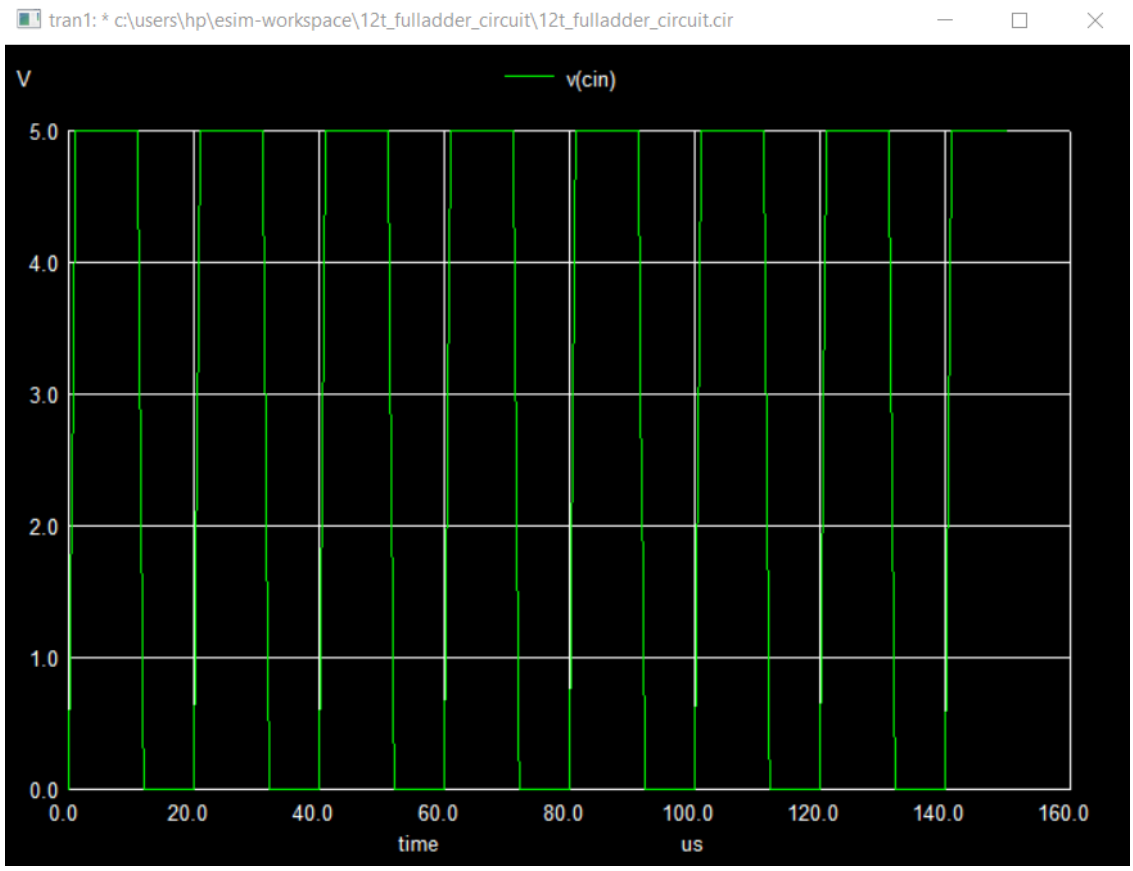


Figure 4: Ngspice plot Input Cin

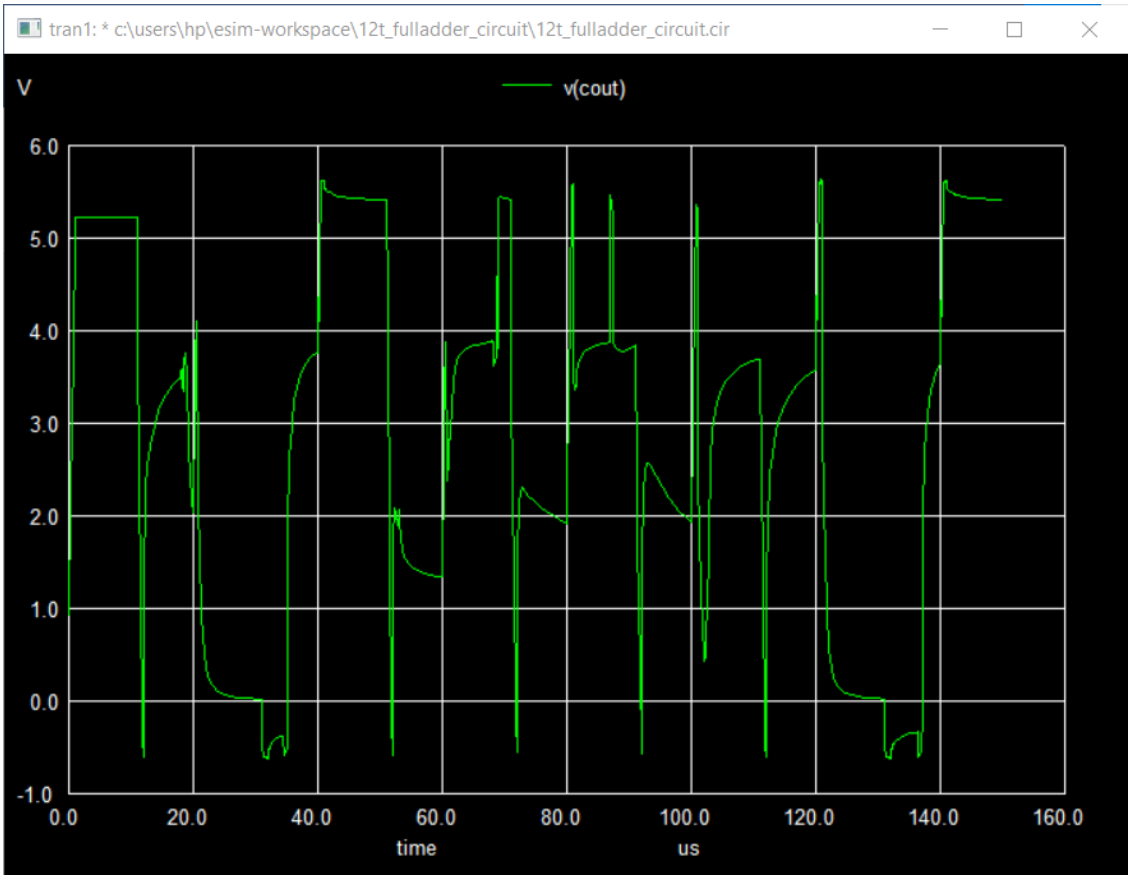


Figure 5: Ngspice plot Output Cout

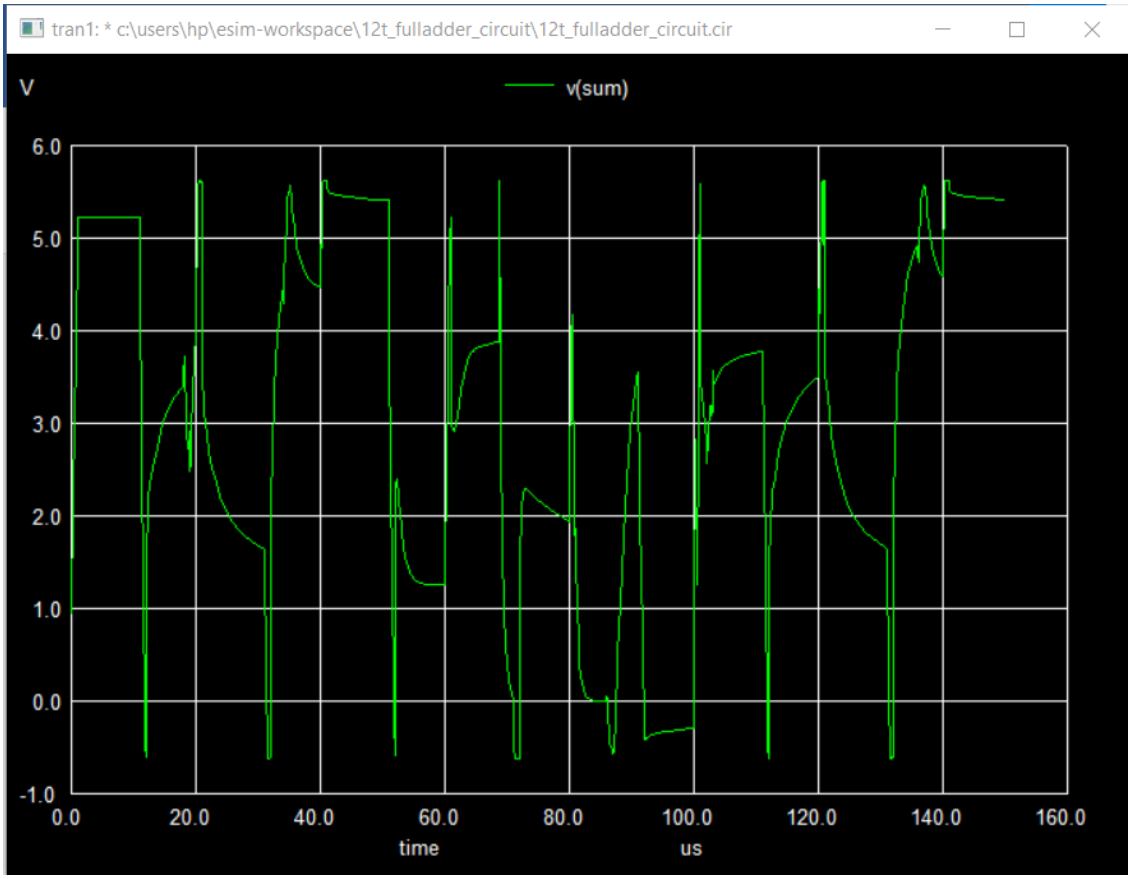


Figure 6: Ngspice plot Output Sum

## 2. Python Plots:

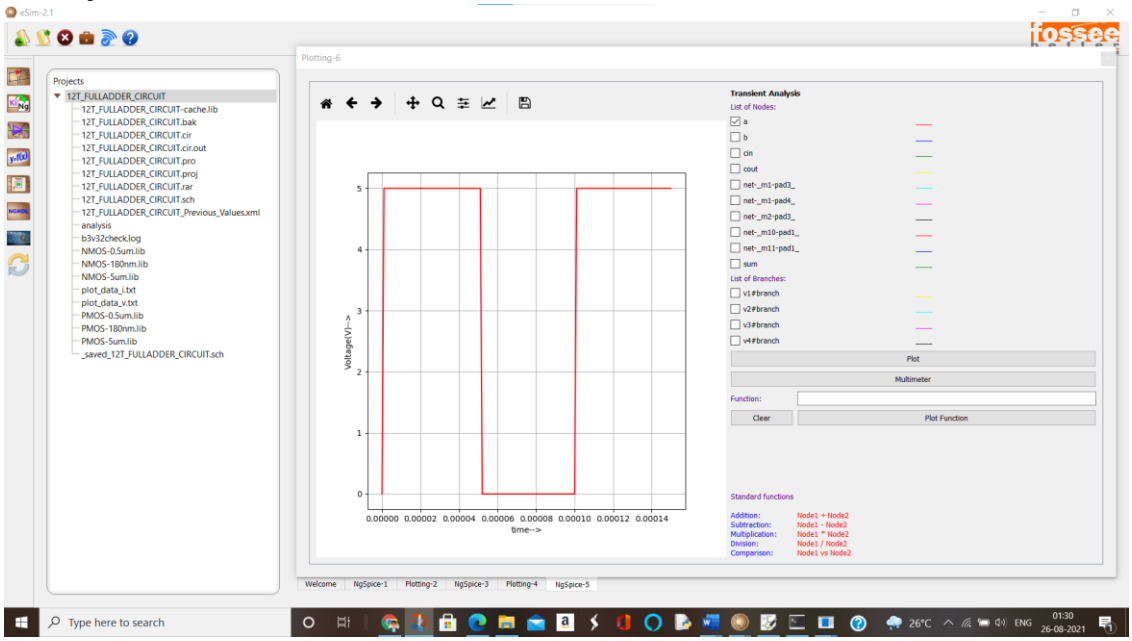


Figure 7: Python Plot Input a

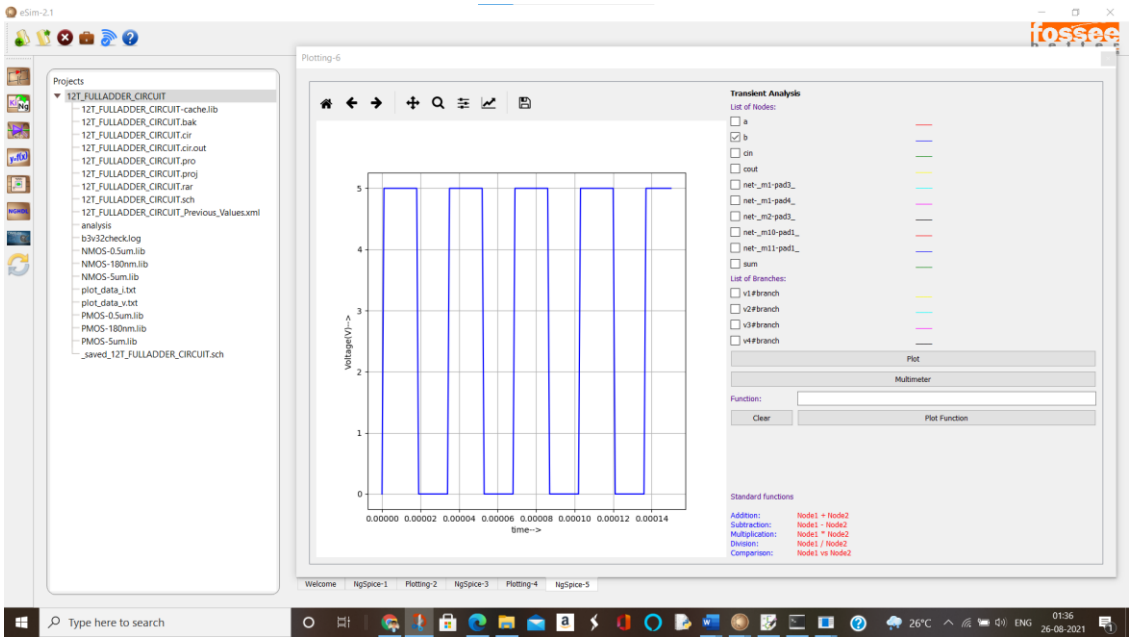


Figure 8: Python Plot Input b

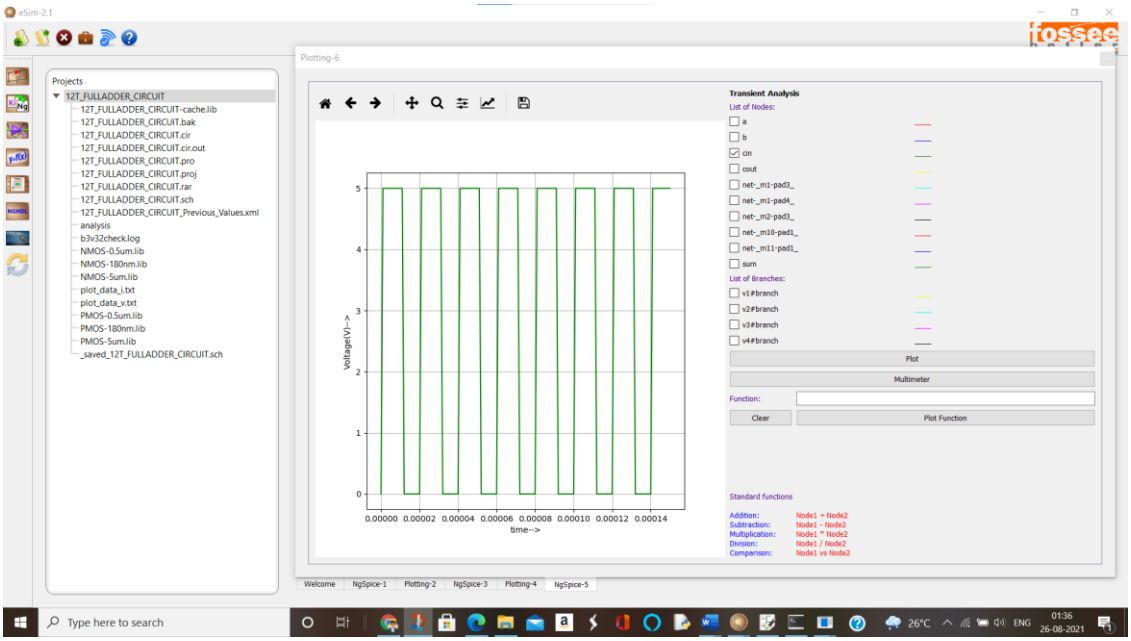


Figure 9: Python Plot input Cin

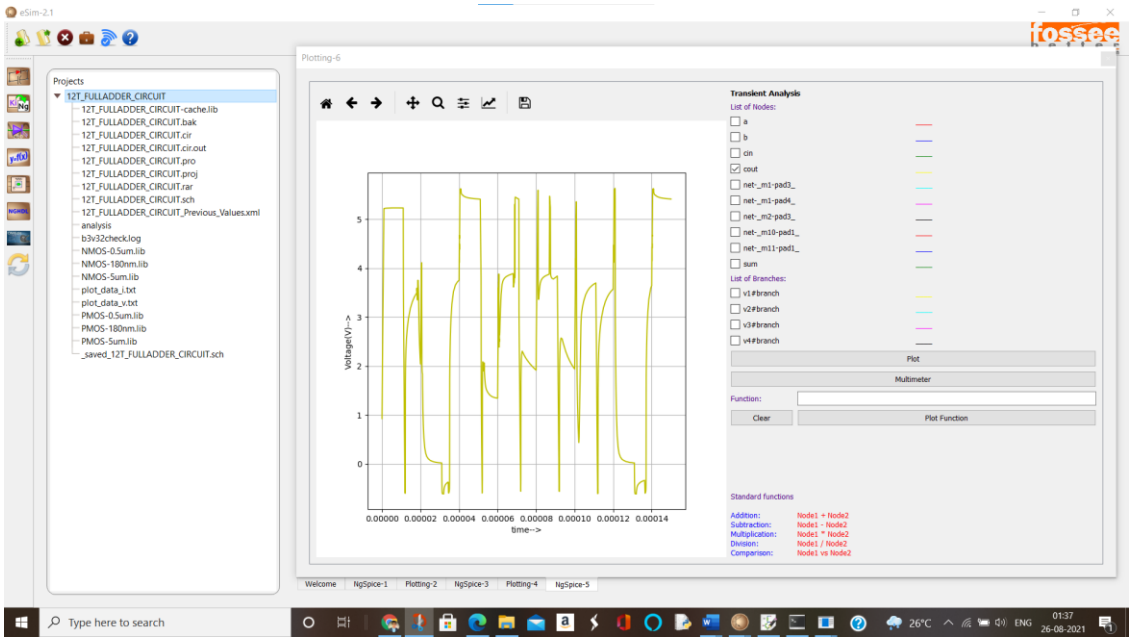


Figure 10: Python Plot Output Cout

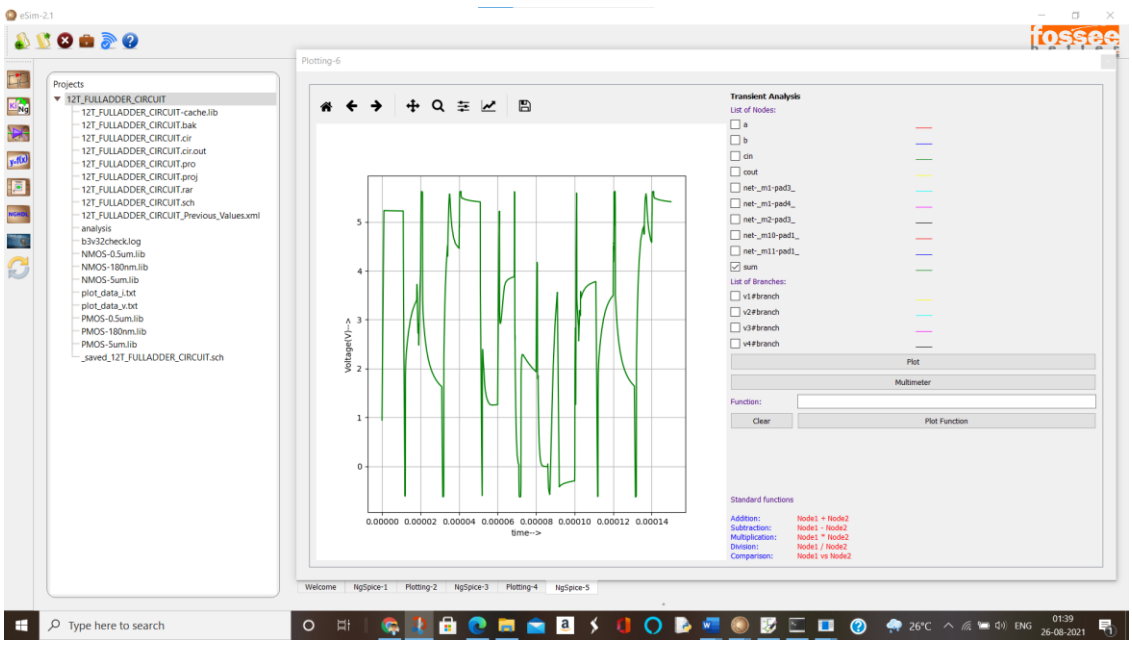


Figure 11: Python Plot Output Sum

## Conclusion:

Thus, we have simulated the 12T Full Adder design using eSim and we get the appropriate waveforms.

## References:


https://ieeexplore.ieee.org/document/126534.

Low-power CMOS digital design | IEEE Journals & Magazine | IEEE Xplore