FOSSEE CIRCUIT SIMULATION PROJECT

Title: 4-Bit Right Barrel Shifter Using 2x1 Multiplexers

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Theory/Description:

Barrel shifters are used to shift a block of data by a desired number of bits, either as left shift or right shift or bi-directional shift, without the need of any sequential logic. In this project, a 4-bit right barrel shifter is designed using the integrated tool, 'eSim' with circuit schematics on KiCAD, and its functionality is observed from NgSpice plots. The barrel shifter is designed with the help of 2X1 multiplexers. Through different combinations of the Select Lines of the Multiplexers, the input bits are shifted by different number of bits. The multiplexer sub-circuit is designed with the help of MOSFETs, using Transmission Gate (TG) logic. 180nm technology is used for MOSFET modelling. For a given 4-bit input, the right shifted output bits are obtained for all combinations of select lines.

The Truth Table for Output of 4-Bit Right Barrel Shifter is as follows:

S1	S0	Y3	Y2	Y1	Y0
0	0	I3	I2	I1	I0
0	1	I0	I3	I2	I1
1	0	I1	I0	I3	I2
1	1	I2	I1	I0	I3

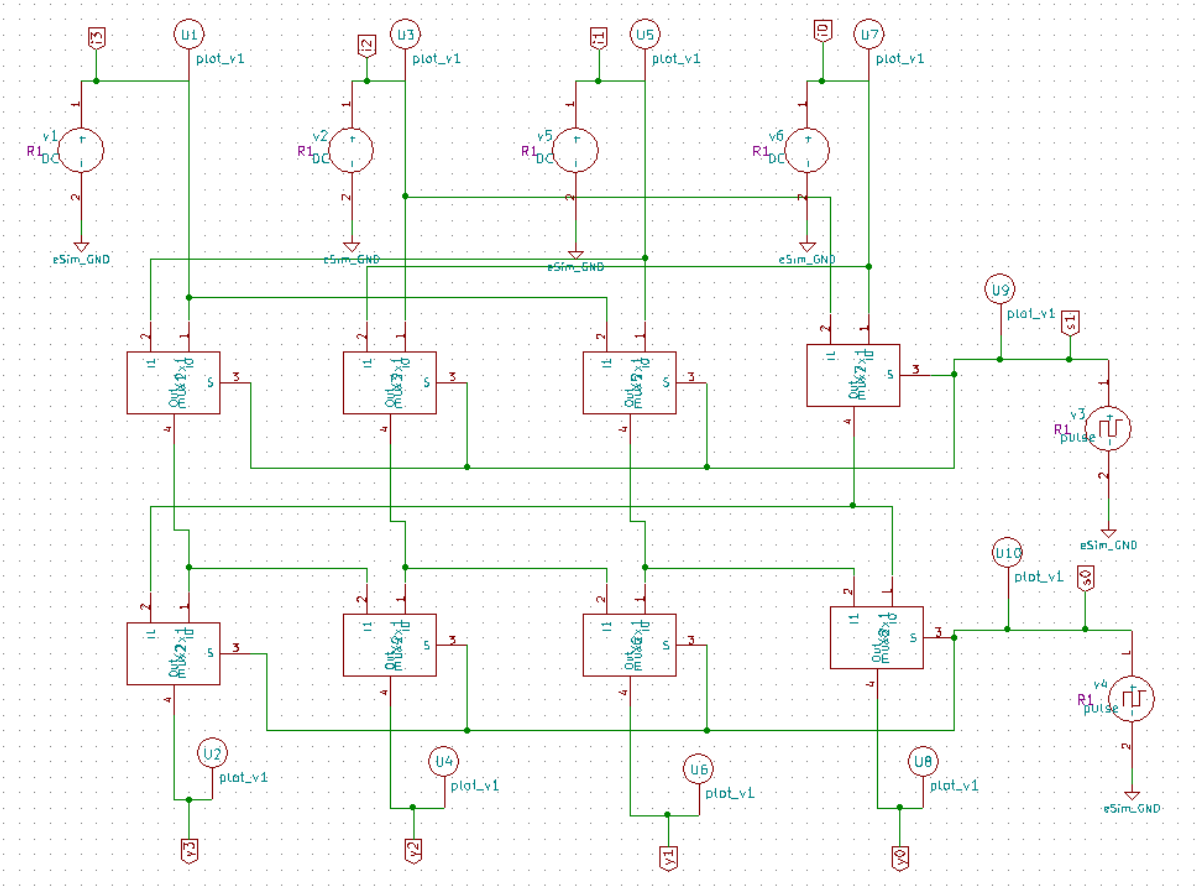
Where S1 and S0 are the Select Lines,

I3, I2, I1, I0 are the input bits, I3 being the MSB and I0 being the LSB,

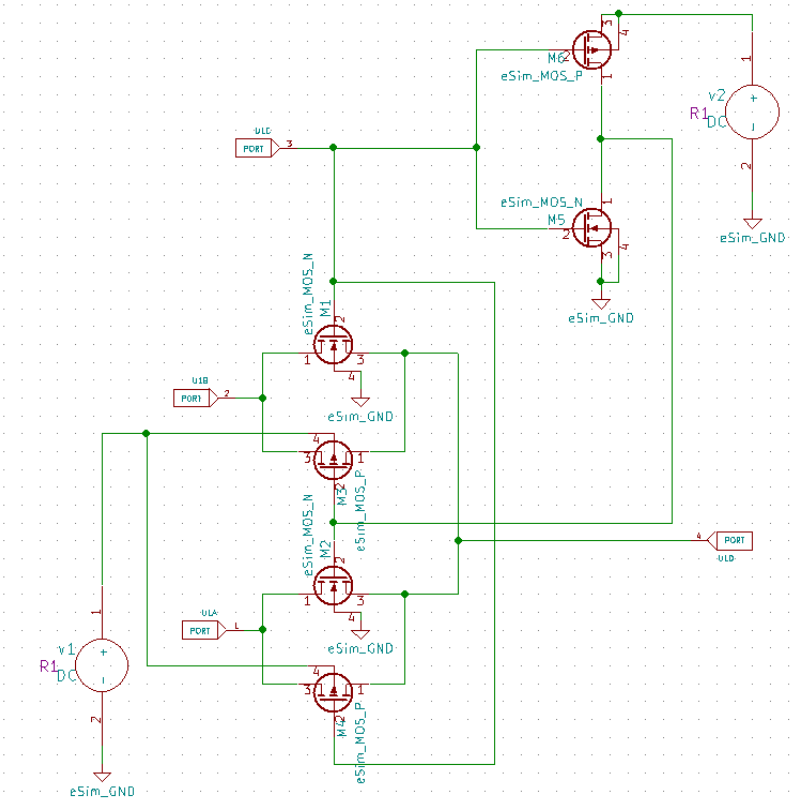
Y3, Y2, Y1, Y0 are the output bits, Y3 being the MSB and Y0 being the LSB.

The 4-bit input: 1 0 0 1 is taken for simulation purpose. From the NgSpice output plots, the 4 combinations of shifted bits are observed and these are cross-validated from the truth table to confirm the functionality of the circuit.

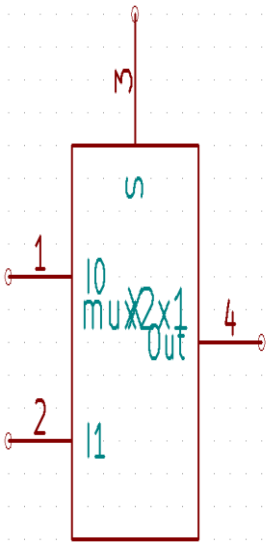
KiCAD Schematic for 4-bit Right Barrel Shifter:



Sub-Circuit Schematic for 2X1 Multiplexer:



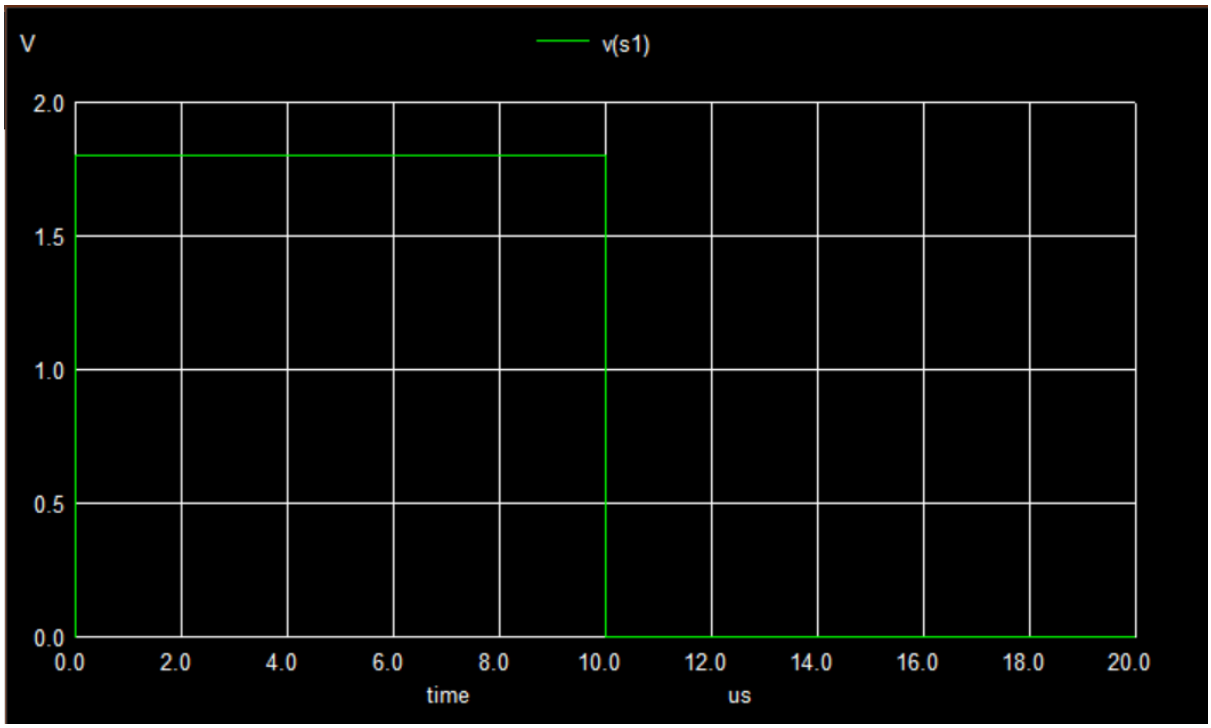
Symbol for 2X1 MUX:



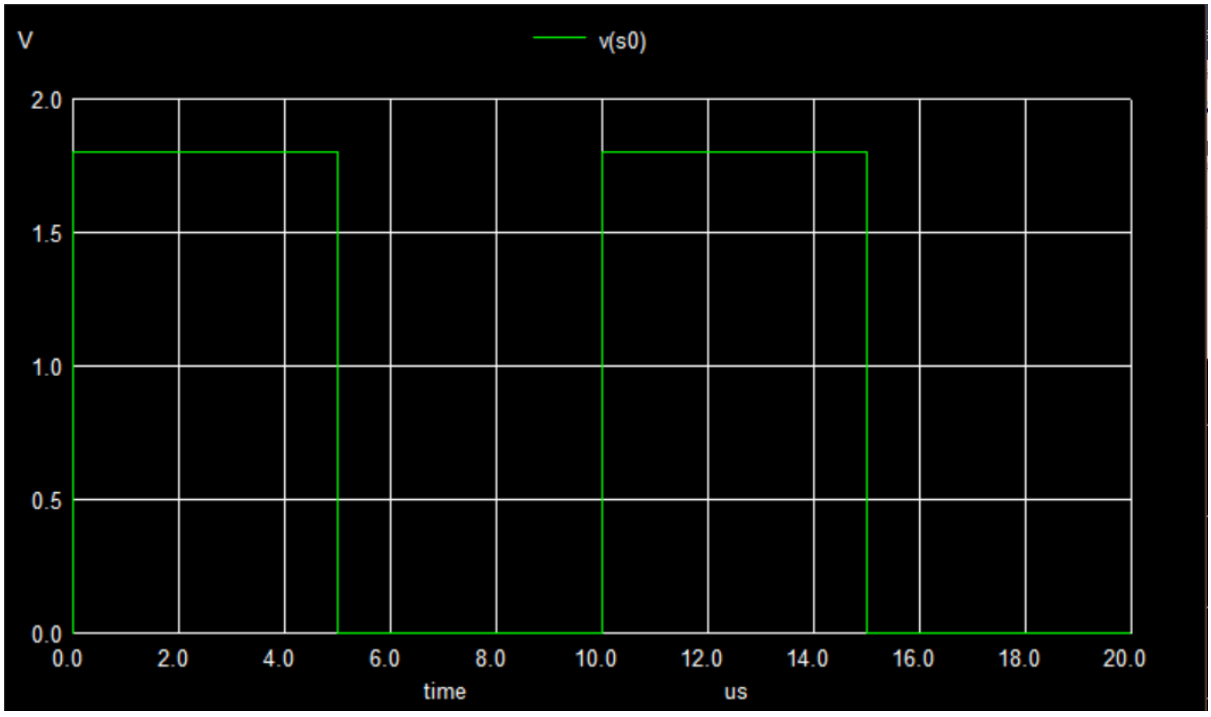
NgSpice Plots:

Select Lines for Multiplexers:

S1:

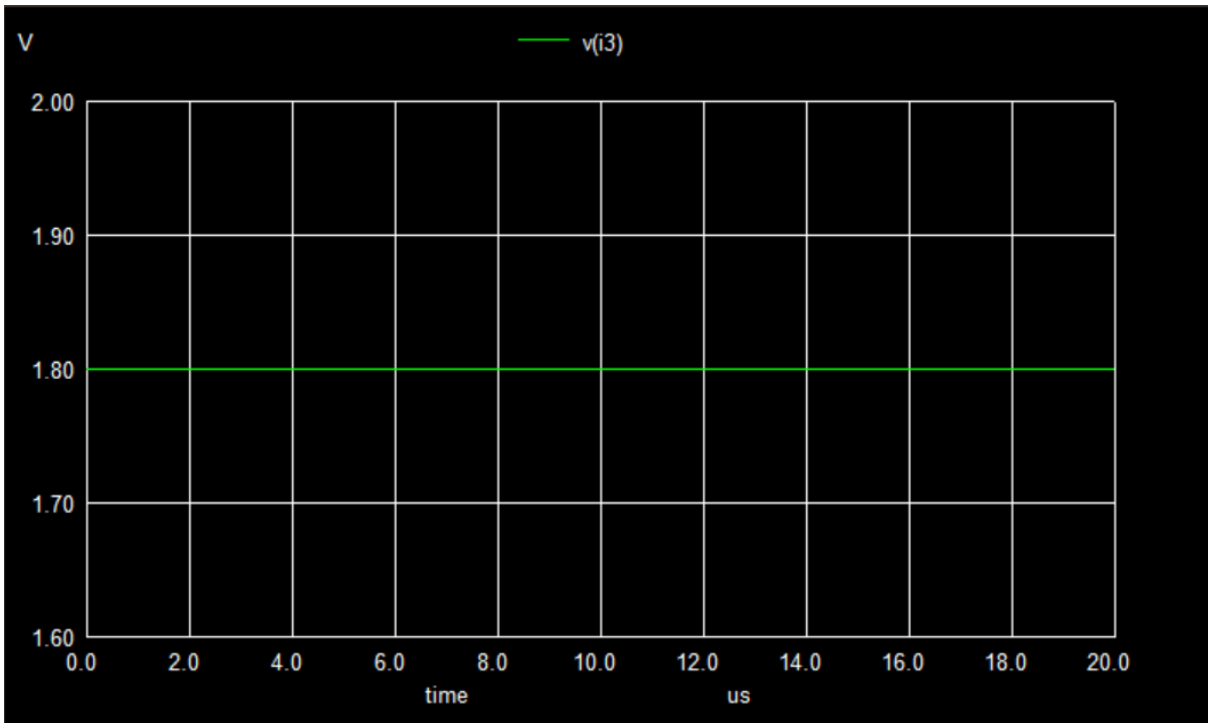


S0:

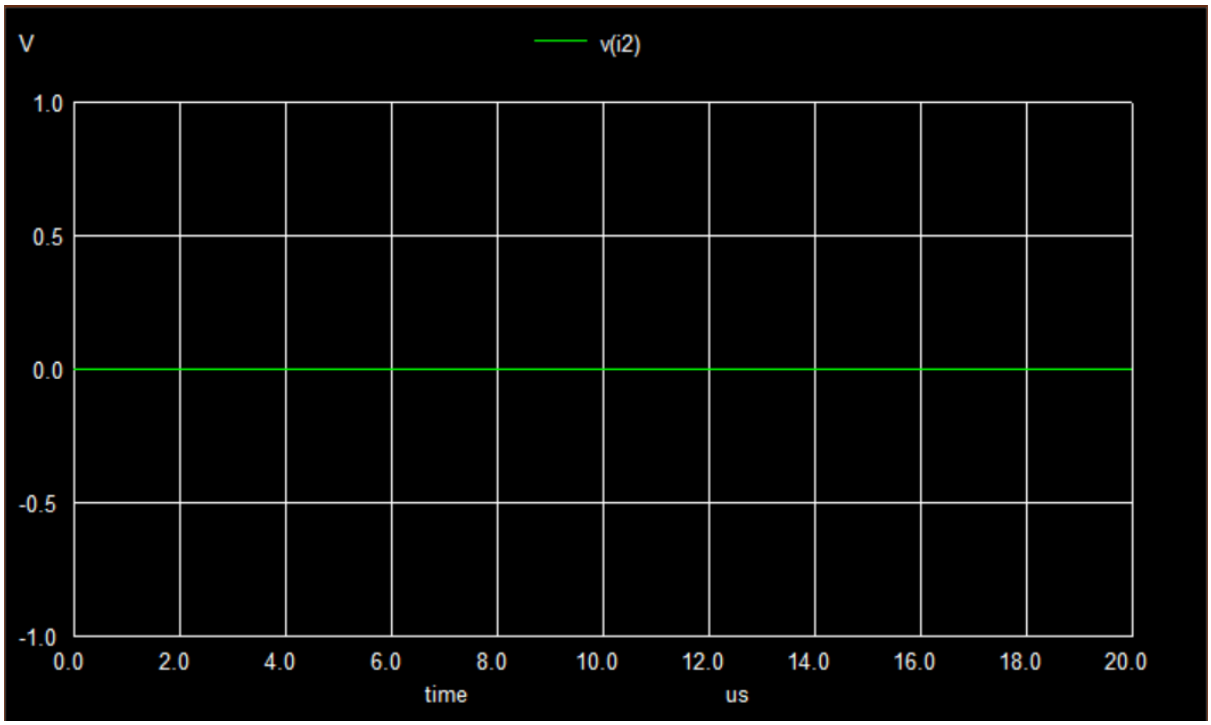


Input to Barrel Shifter: **I3 I2 I1 I0 = 1 0 0 1**

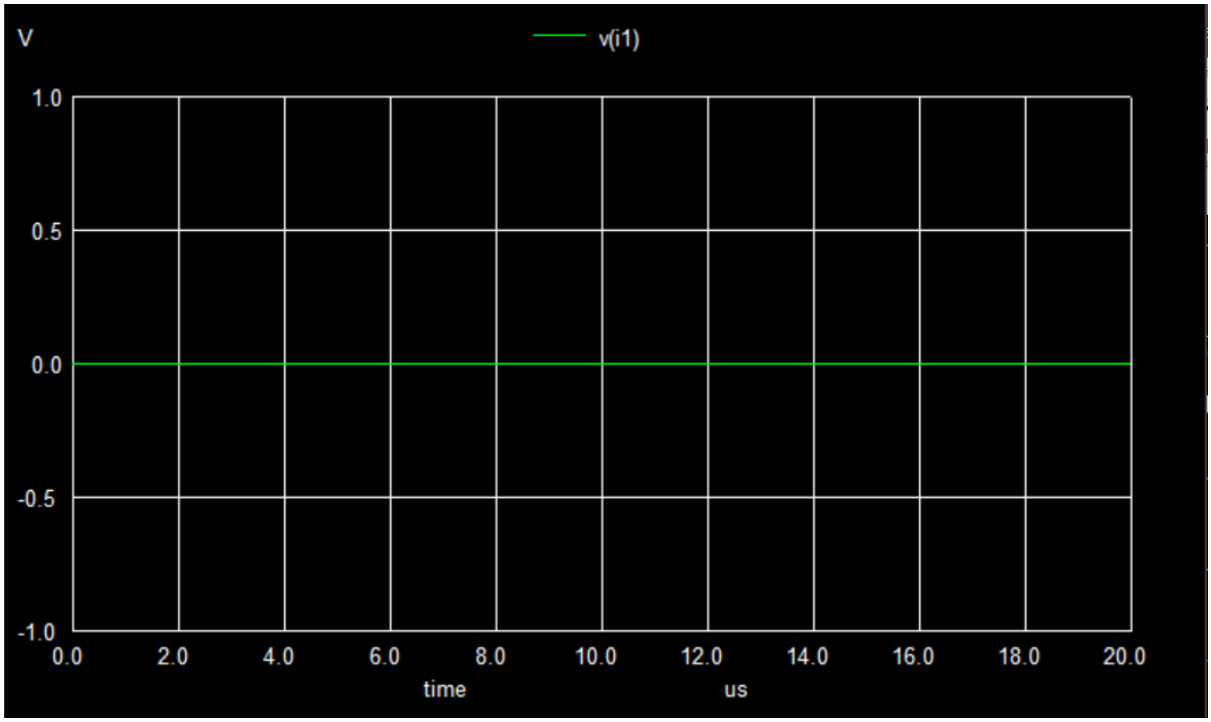
I3:



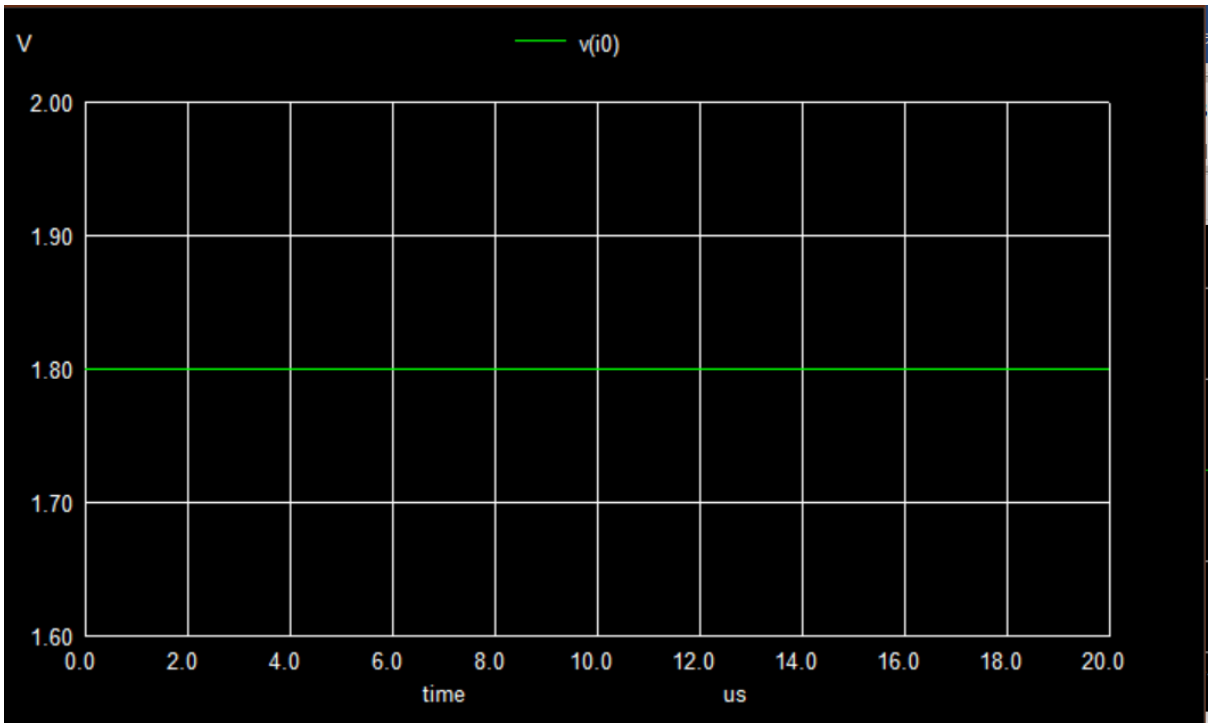
I2:



I1:

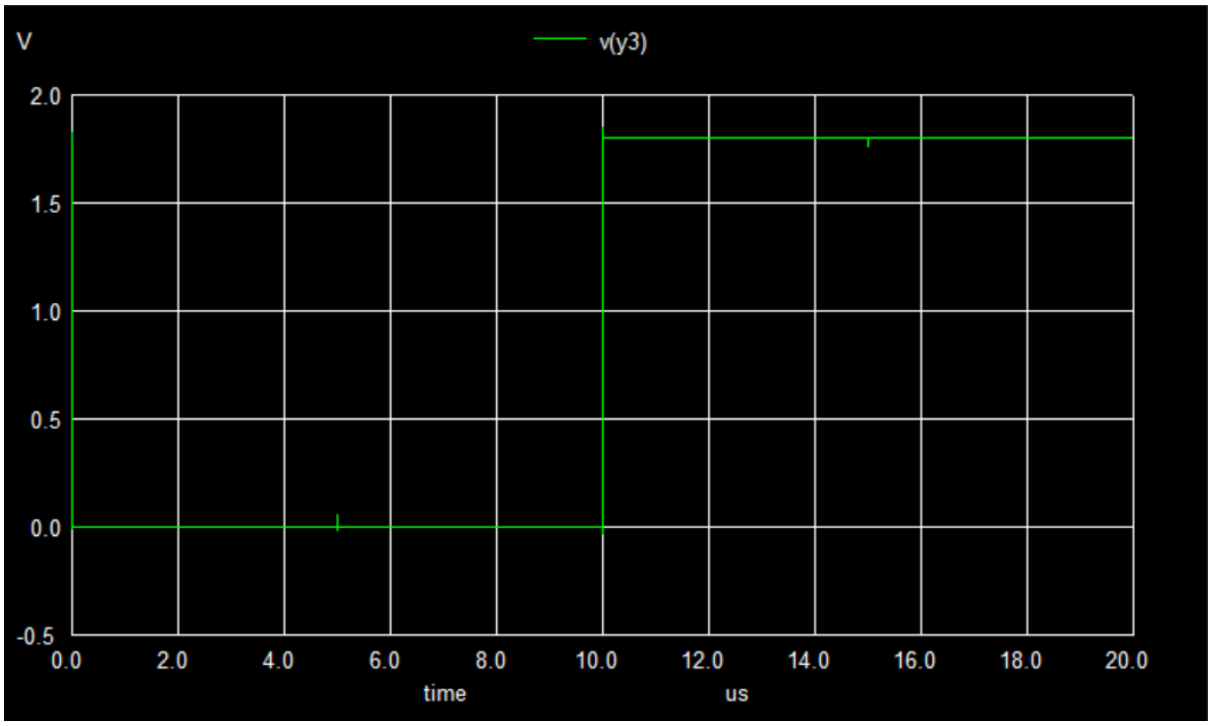

V
v(i1)
1.0
0.5
0.0
-0.5
-1.0
0.0
2.0
4.0
6.0
8.0
10.0
12.0
14.0
16.0
18.0
20.0
time
us

I0:

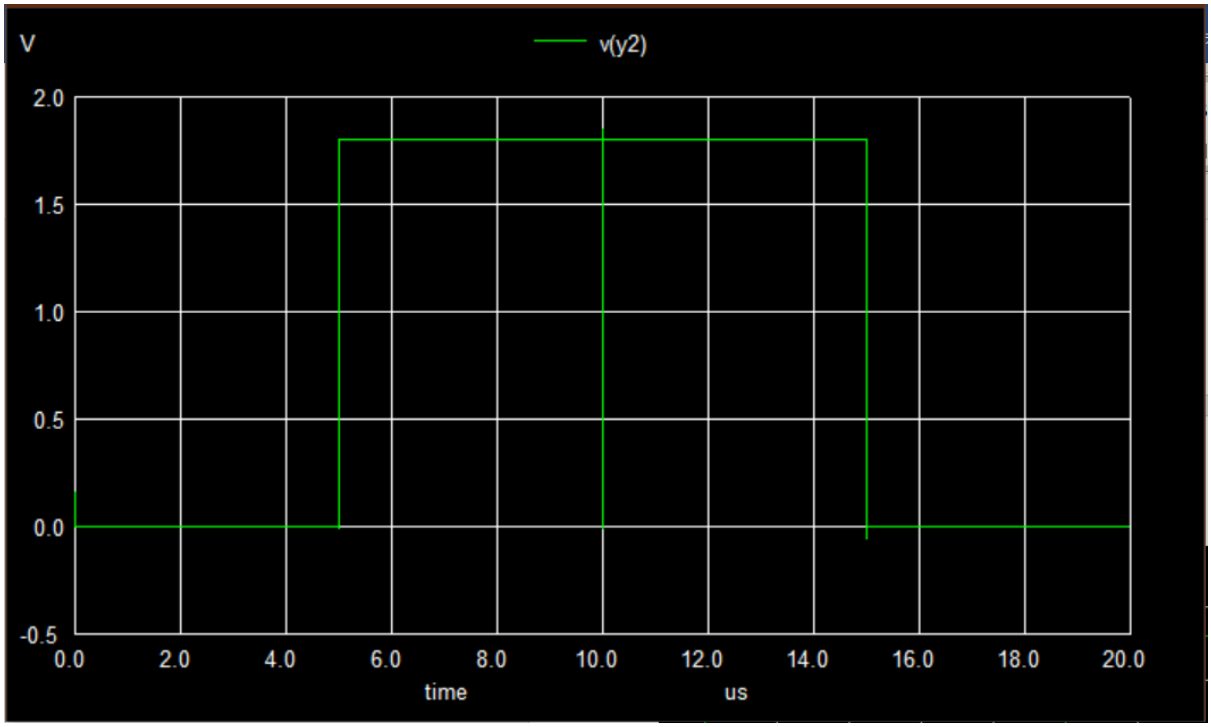

V
v(i0)
2.00
1.90
1.80
1.70
1.60
0.0
2.0
4.0
6.0
8.0
10.0
12.0
14.0
16.0
18.0
20.0
time
us

Output Bits of Right Barrel Shifter:

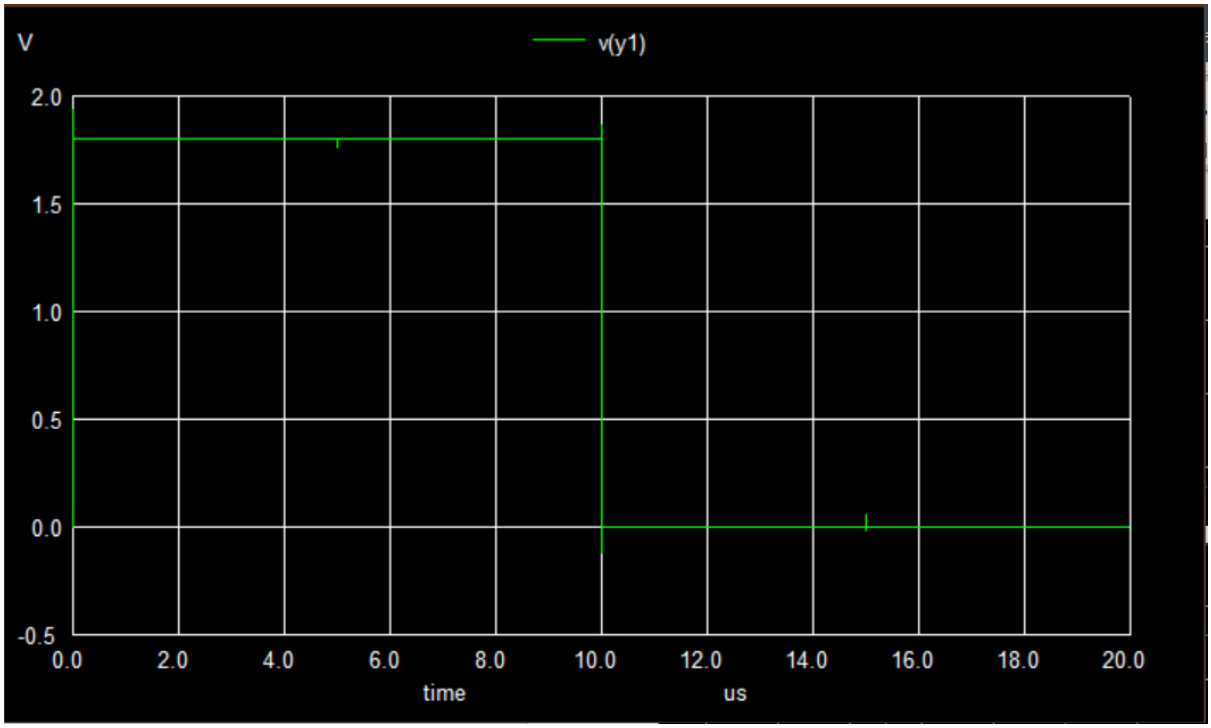
Y3:



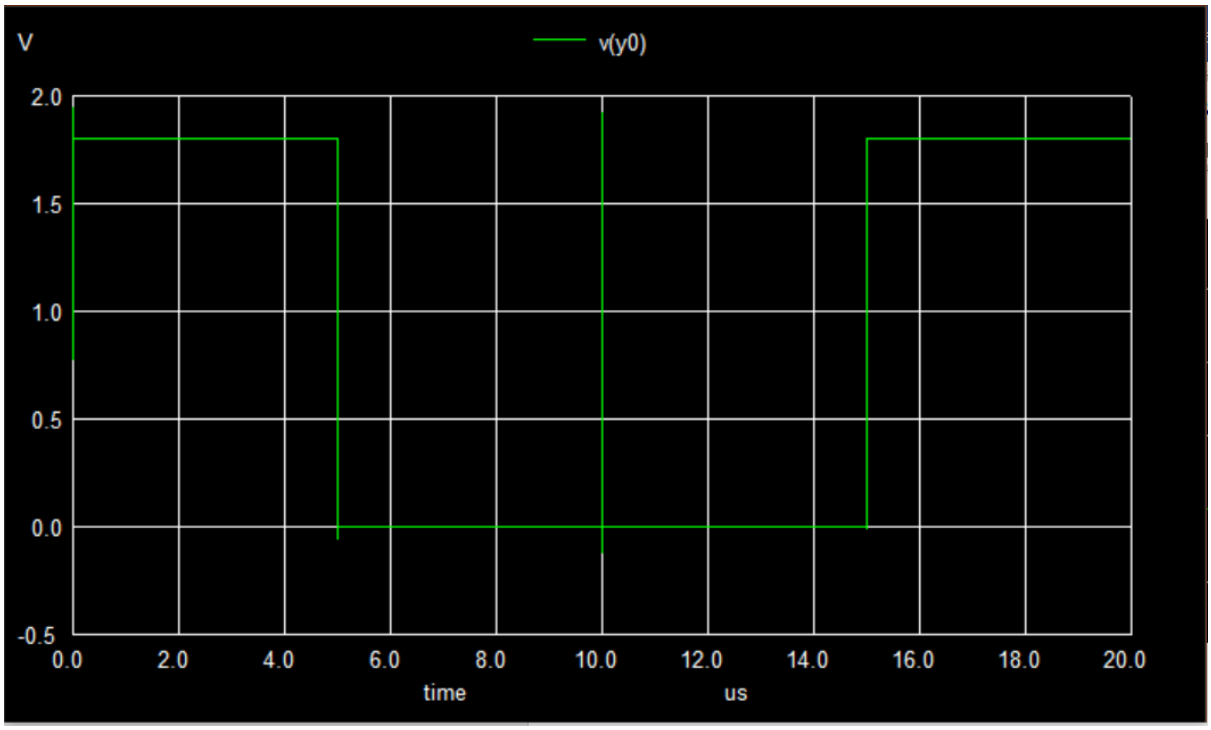
Y2:



Y1:


V
v(y1)
2.0
1.5
1.0
0.5
0.0
-0.5
0.0
2.0
4.0
6.0
8.0
10.0
12.0
14.0
16.0
18.0
20.0
time
us

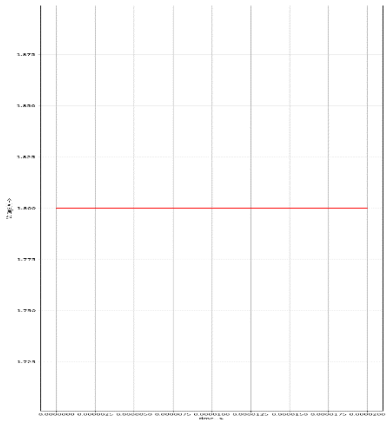
Y0:


V
v(y0)
2.0
1.5
1.0
0.5
0.0
-0.5
0.0
2.0
4.0
6.0
8.0
10.0
12.0
14.0
16.0
18.0
20.0
time
us

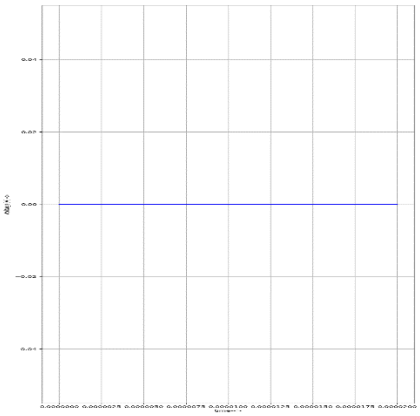
Python Plots:

Input Bits to Barrel Shifter:

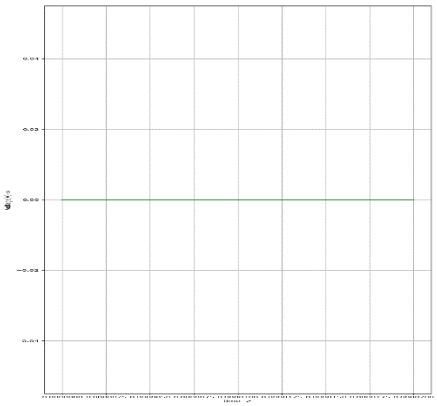
I3:



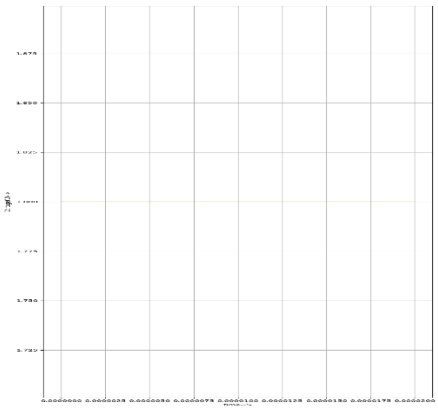
I1:



I1:

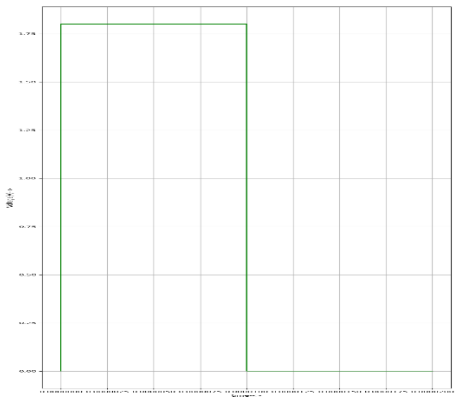


I0:

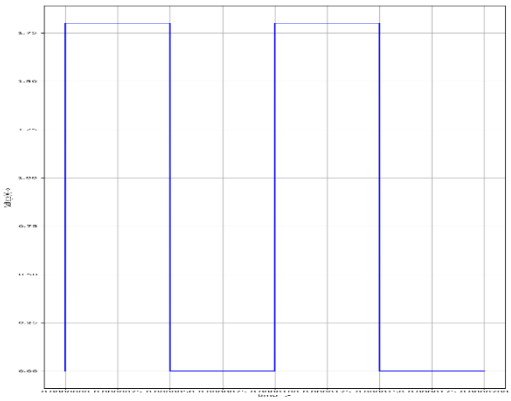


SELECT LINES OF MULTIPLEXERS:

S1:

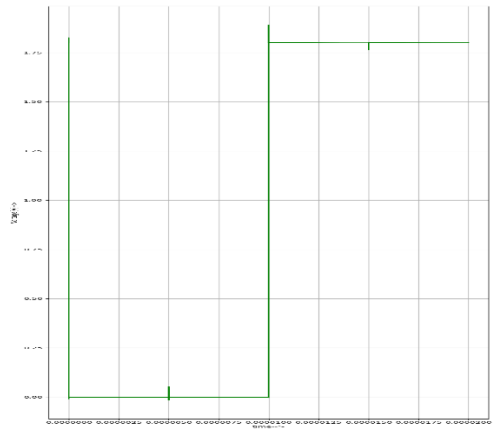


S0:

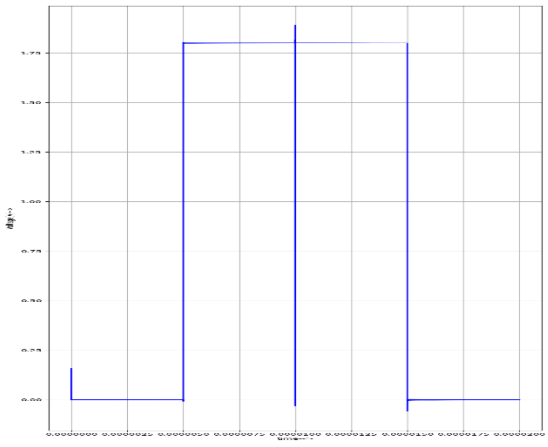


OUTPUT BITS OF BARREL SHIFTER:

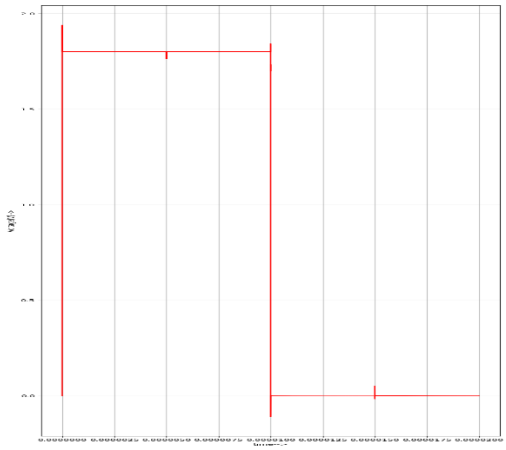
Y3:



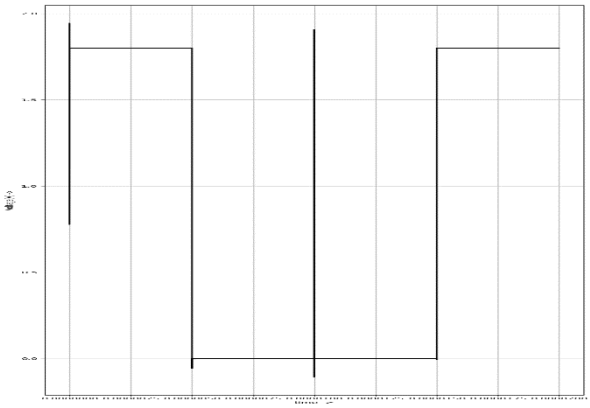
Y2:



Y1:



Y0:



Conclusion:

We conclude that the 4-bit right barrel shifter was designed and simulated successfully using eSim. The output bits for all combinations of Select Lines are corresponding to the Truth table values. Hence the functionality of the circuit is verified.

References:

1. http://www.barrywatson.se/dd/dd_shifter_barrel.html
2. http://troindia.in/journal/ijcesr/vol5iss4/350-354.pdf