Title of the Experiment : --

RTL of FULL ADDER USING BJT

DESIGN AND SIMULATION using eSim

Theory : --

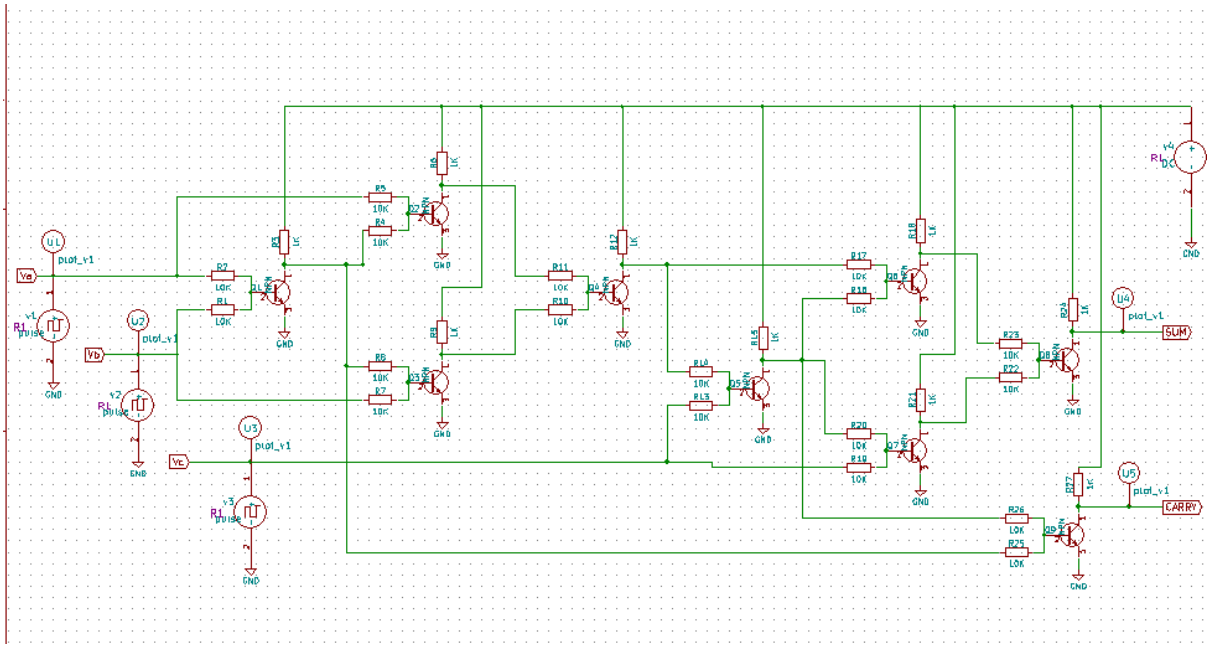
Full adder is the combinational circuit which is use to add three inputs and give the two outputs which is sum or carry. A **full adder** logic is designed in such a manner that can take eight inputs together to create a byte-wide adder and cascade the carry bit from one adder to the another.

It is possible to construct a circuit that performs both addition and subtraction at the same time.

We can make Full Adder using half adder. In this process we are use two half adder and one OR Gate.

Schematic Diagram:

The circuit schematic of RTL of FULL ADDER USING BJT-DESIGN AND SIMULATION on eSim is as shown below:



Simulation Results :-

1.Ngspice Plots

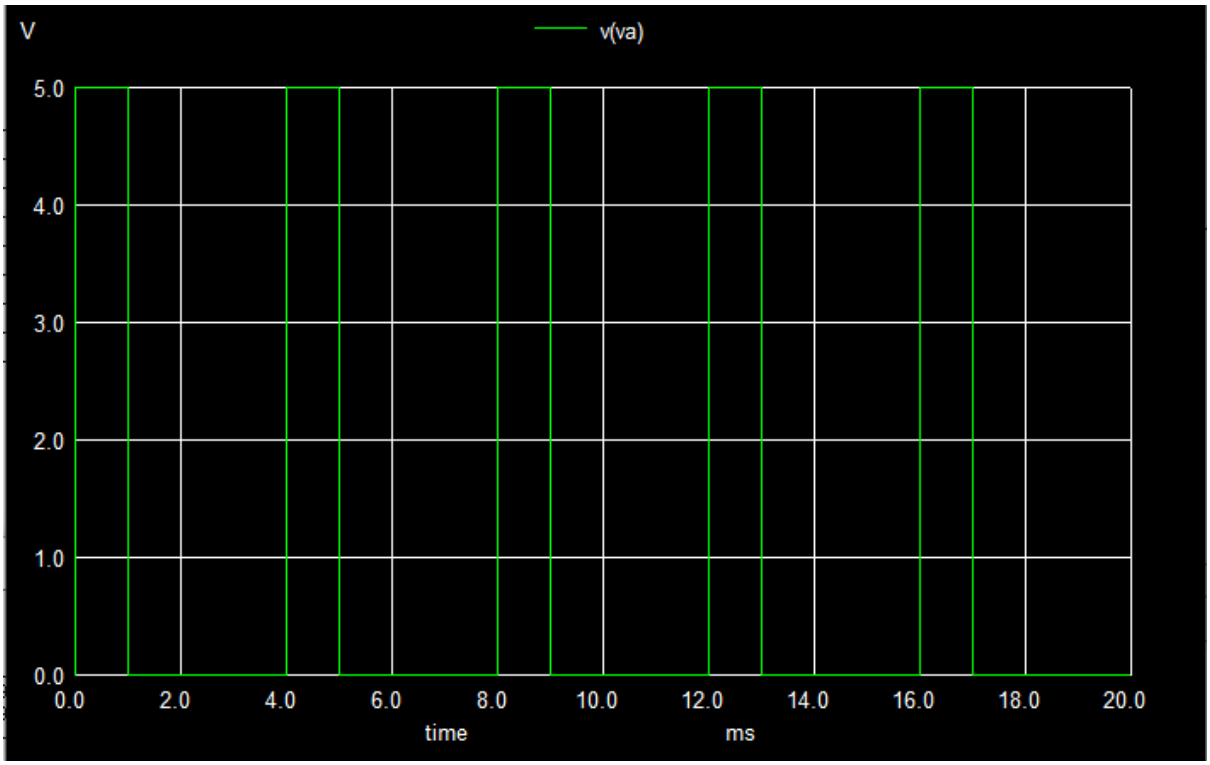


Fig : Ngspice Input plot(Va)

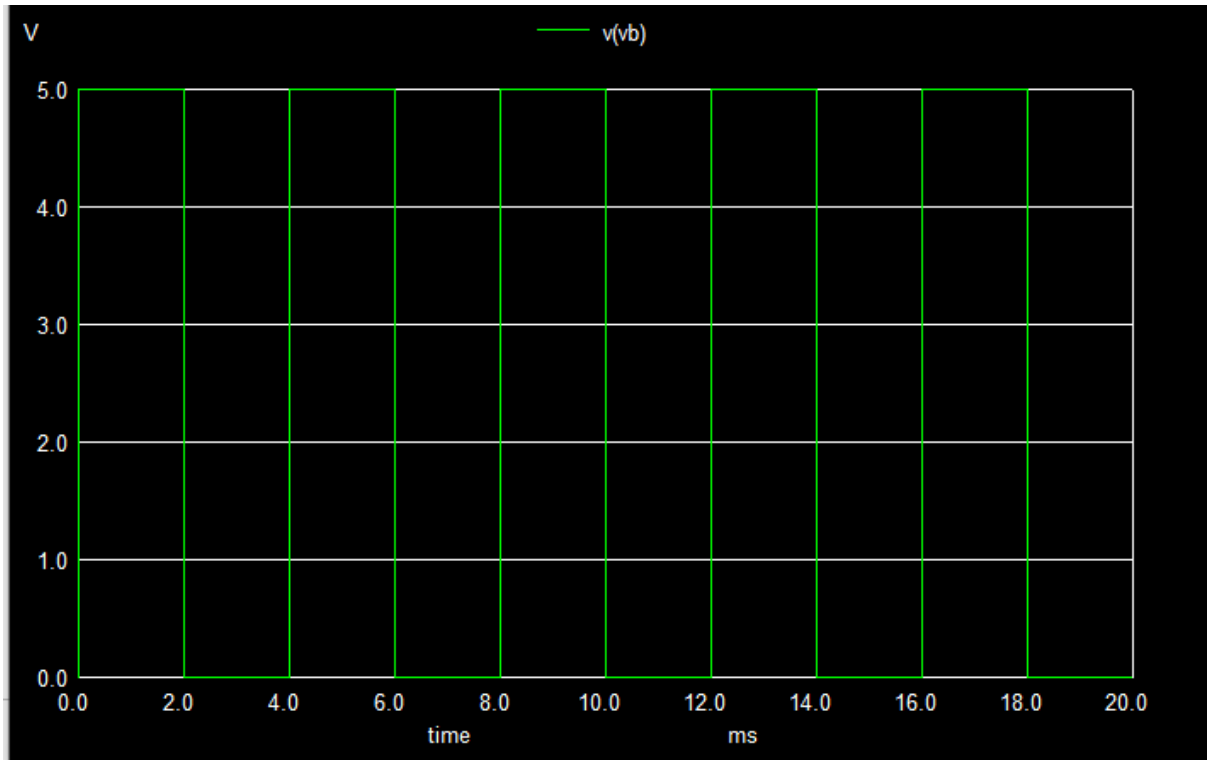


Fig : Ngspice Input plot(Vb)

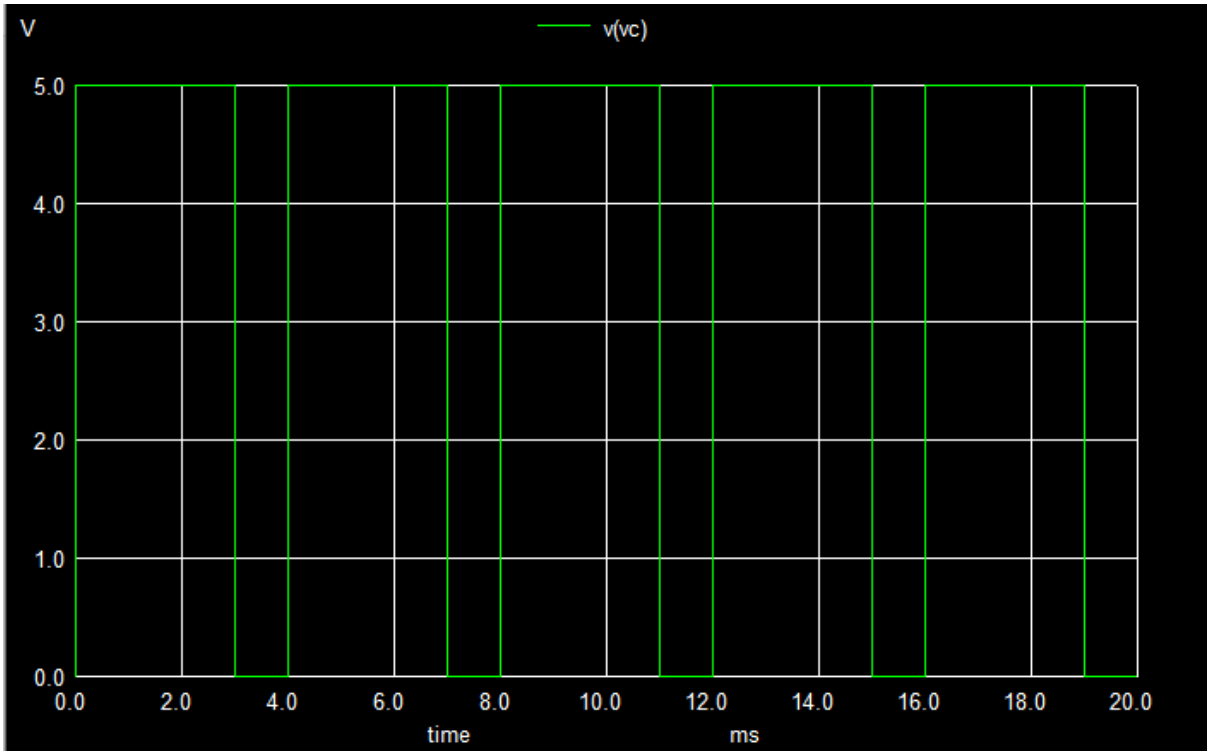


Fig : Ngspice Input plot(Vc)

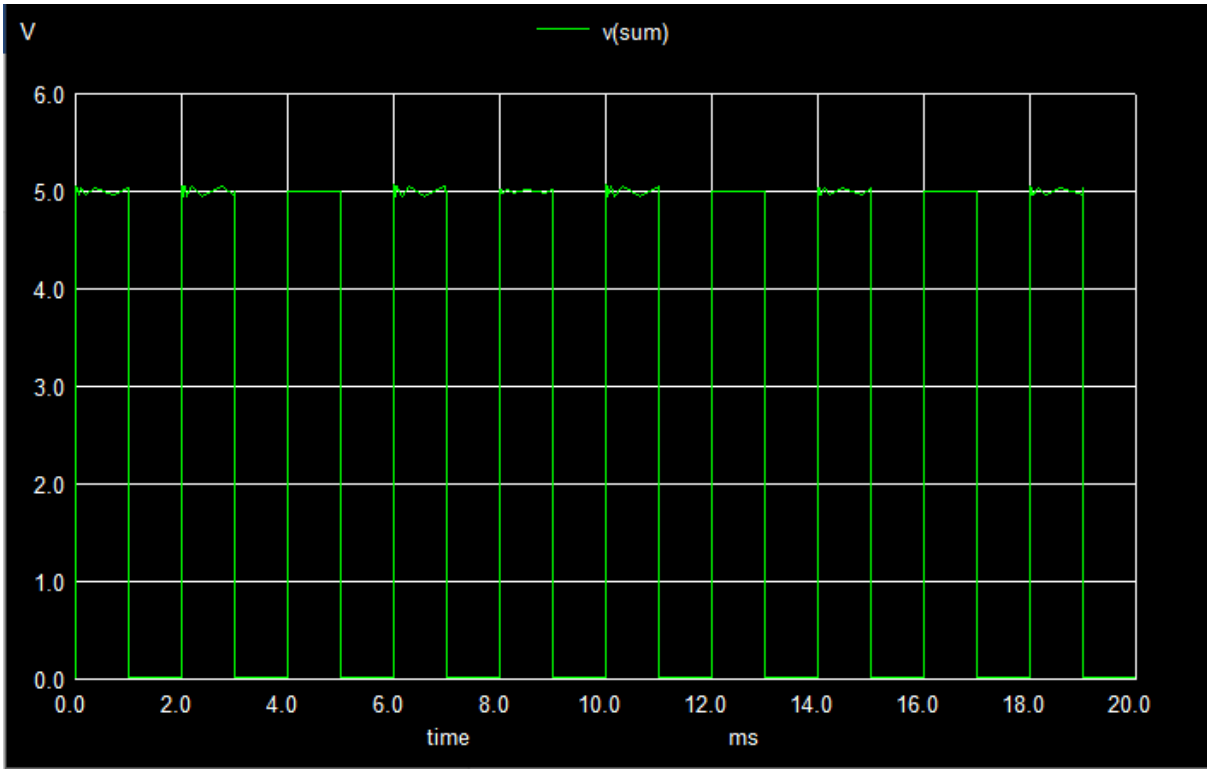


Fig : Ngspice Output plot(Sum).

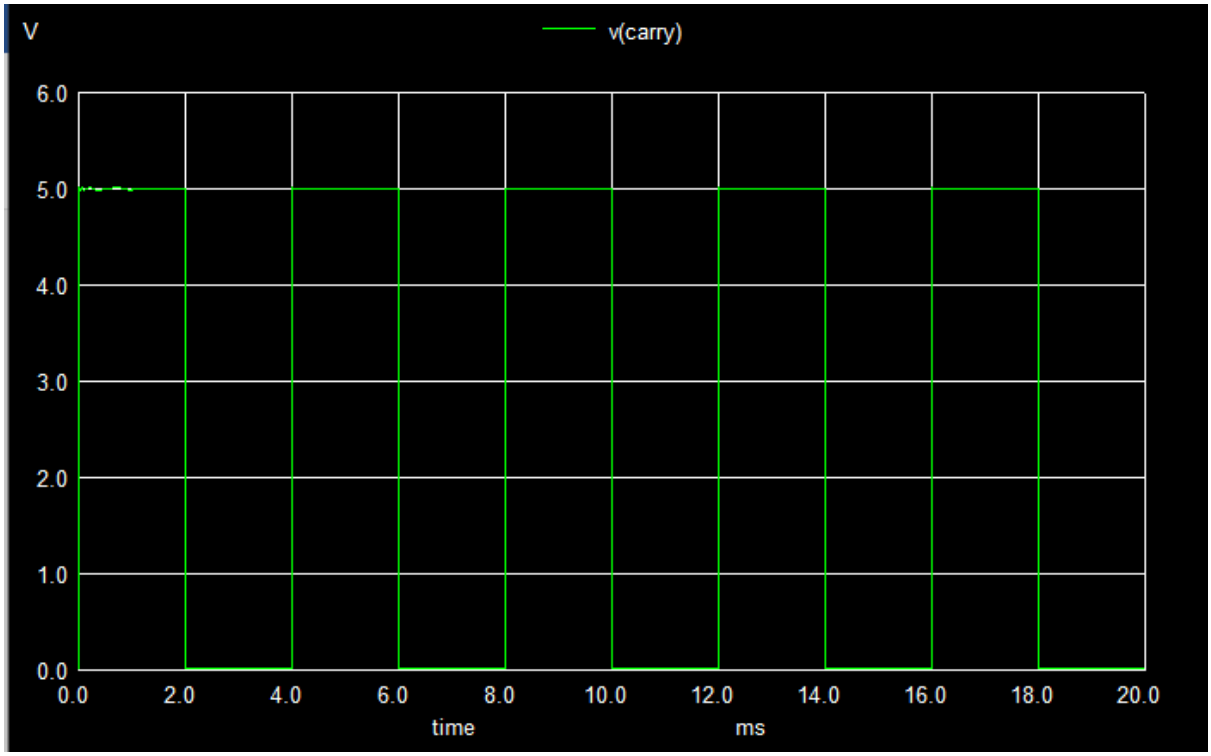


Fig ： Ngspice Output plot(Carry).

2.**Python Plots**

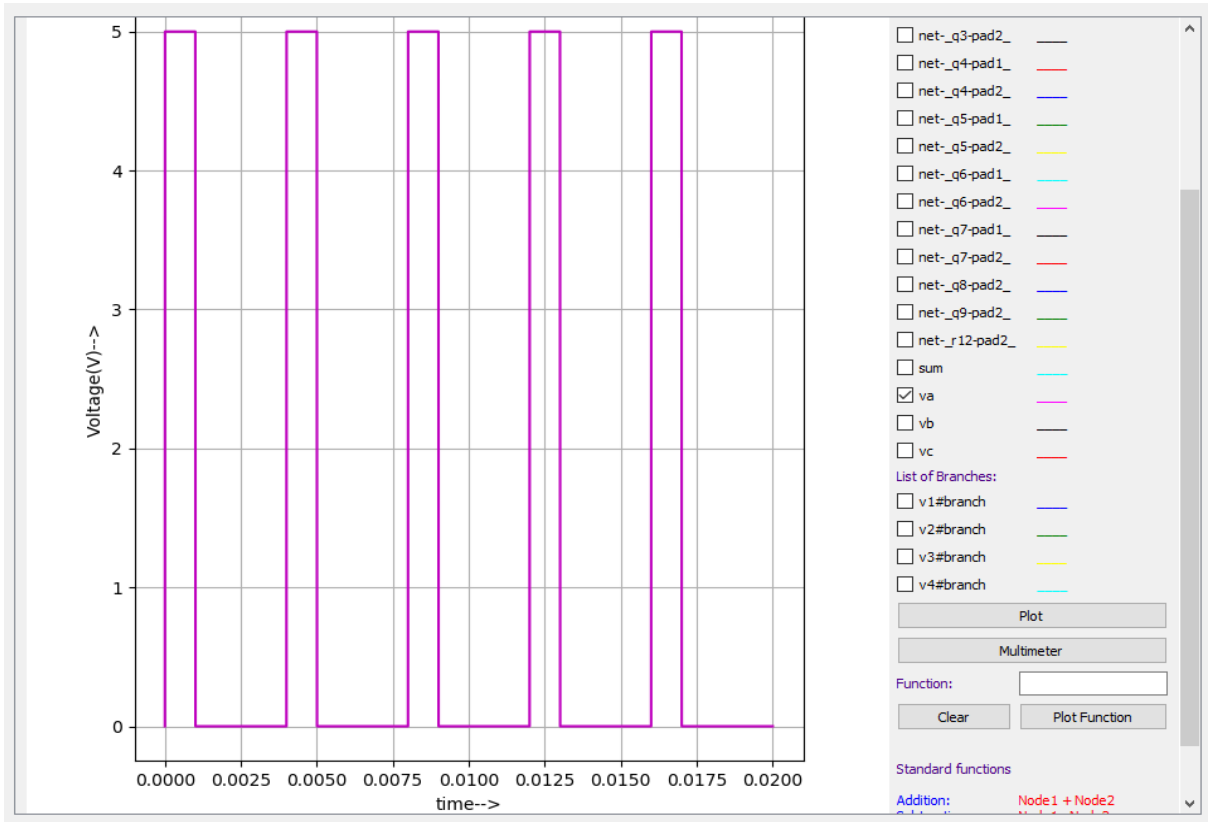


Fig. Python Plot Input (Va).

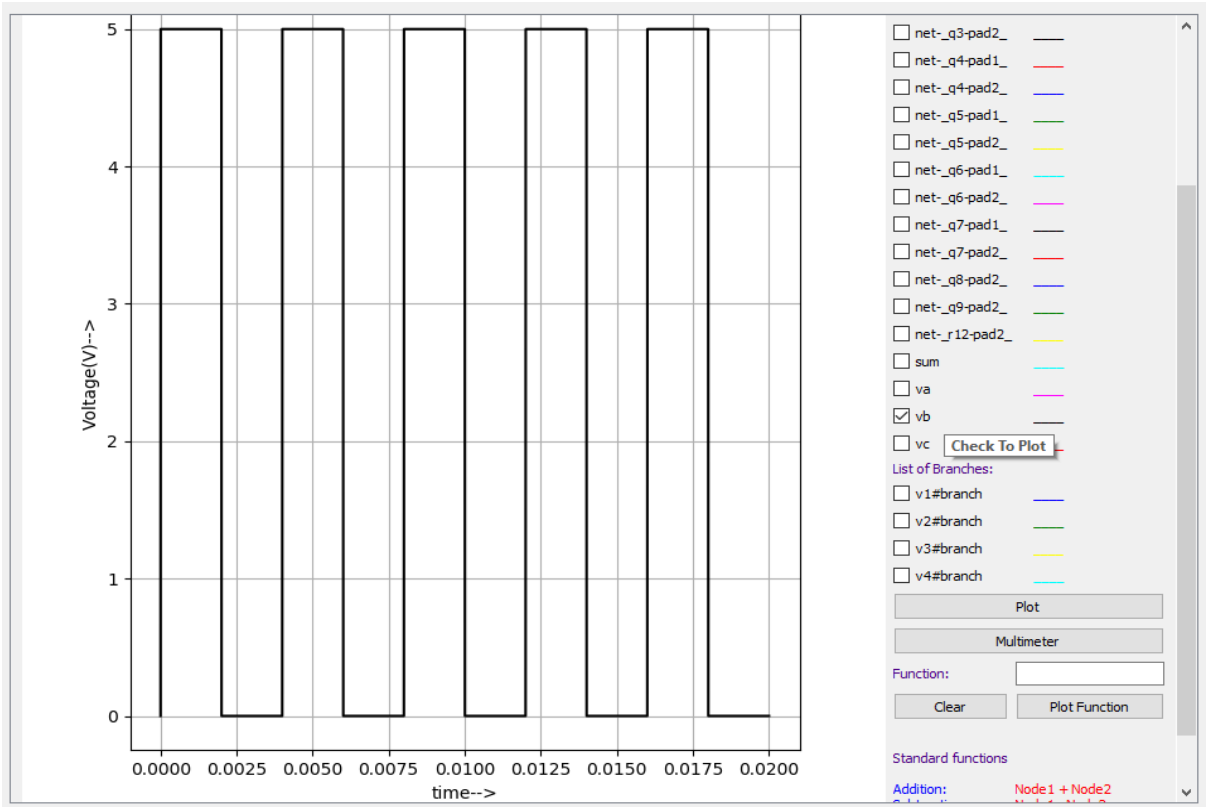


Fig. Python plot Input(Vb)

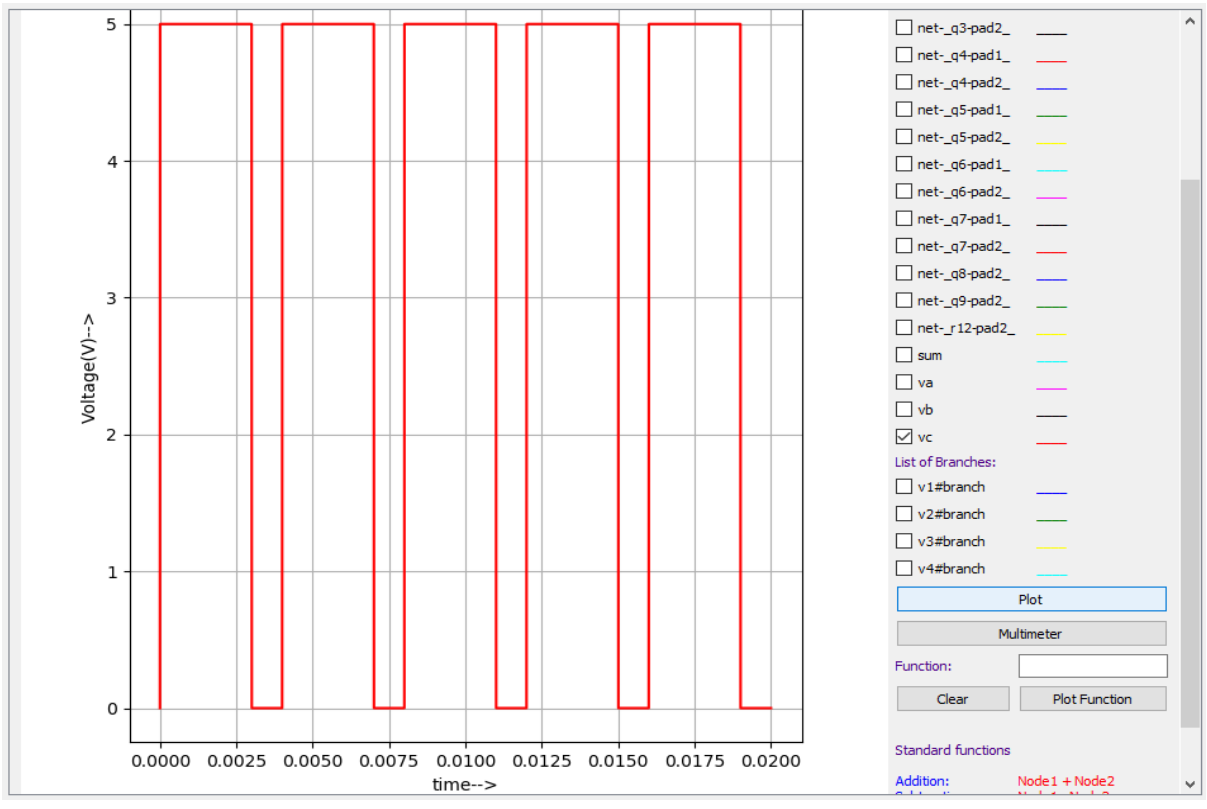


Fig. Python plot Input(Vc).

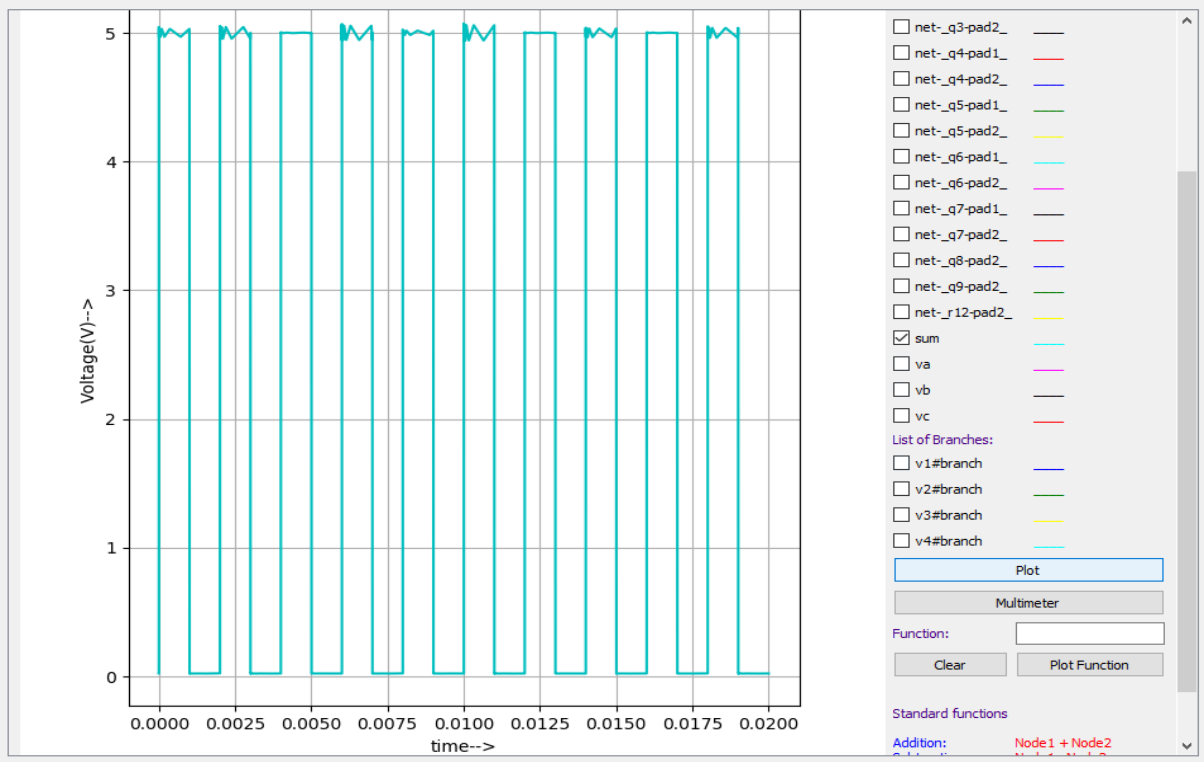


Fig. Python plot of Output(Sum).

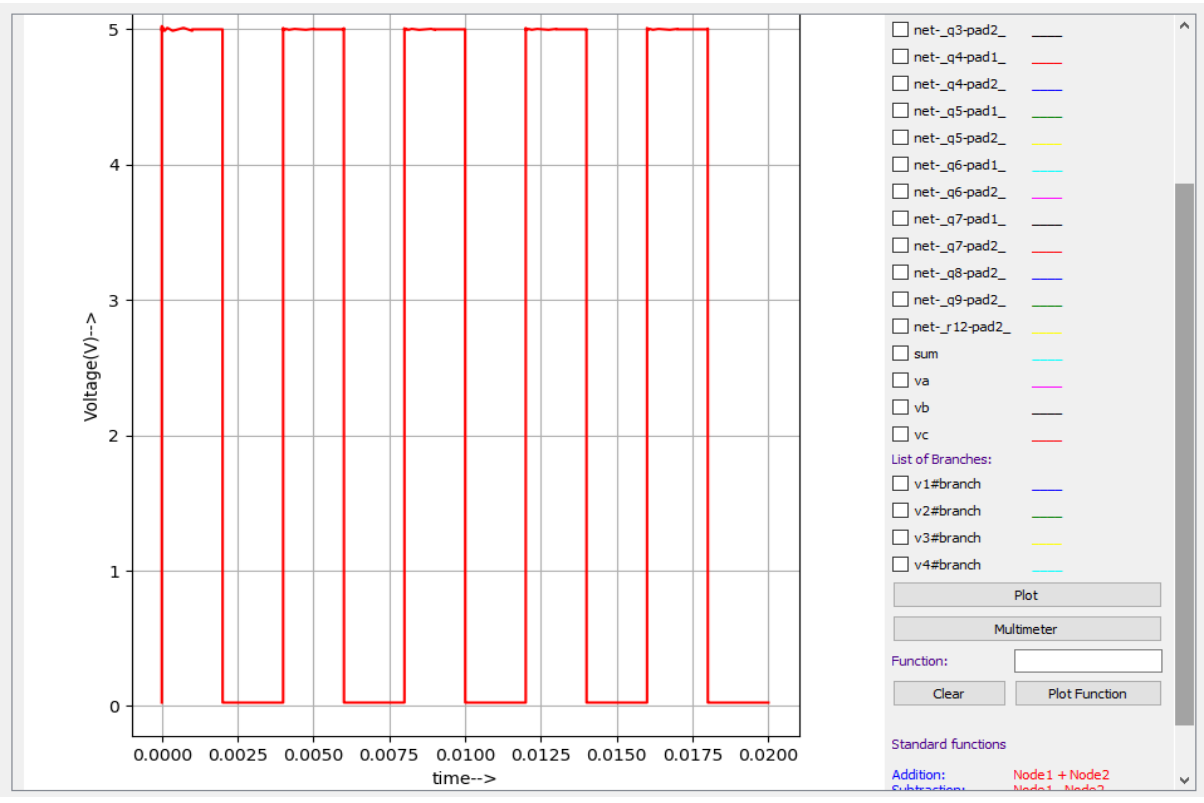


Fig. Python plot of Output(Carry).

Conclusion :

Thus, we have studied the RTL of FULL ADDER USING BJT-DESIGN AND SIMULATION using eSim and we get the appropriate waveforms.

References :

https://electronics.stackexchange.com/questions/265567/building-a-full-adder-with-npn-bjt-transistors