Circuit Simulation Project

https://esim.fossee.in/circuit-simulation-project

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Project Guide: Dr. R. Maheswari

Title of the circuit: 3-Bit Even & Odd Parity Generator

Theory:

Parity is a very useful tool in information processing in digital computers to indicate any presence of error bit information. To indicate any occurrence of error, an extra bit is included with the message according to the total number of 1's in a set of data, which is called parity. If the extra bit is considered 0 if the total number of 1's is even and 1 for odd quantities of 1's in a set of data, then it is called even parity. On the other hand, if the even bit is 1 for even quantities of 1's and 0 for an odd number of 1's, then it is called odd parity.

The message including the parity is transmitted and then checked at the receiving end of errors. Error is detected if the parity doesn't correspond with the one transmitted.

A parity generator is a combination logic system to generate the parity bit at the transmitting side.

Project Description:

The project deals with design and simulation of a 3-Bit Even & Odd Parity Generator. While designing it, we have taken 3 inputs namely A, B and C and have dotted down their truth table and Boolean expression.

Truth Table:

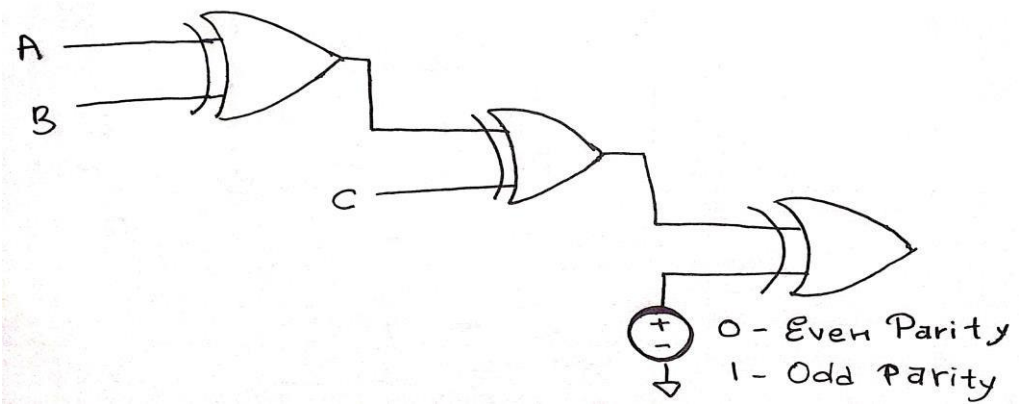
3	**BIT**	**Message**		
Input A	**Input B**	**Input C**	**Odd Parity Bit**	**Even Parity Bit**
0	**0**	**0**	**1**	**0**
0	**0**	**1**	**0**	**1**
0	**1**	**0**	**0**	**1**
0	**1**	**1**	**1**	**0**
1	**0**	**0**	**0**	**1**
1	**0**	**1**	**1**	**0**
1	**1**	**0**	**1**	**0**
1	**1**	**1**	**0**	**1**

After simplifying we get the expression as

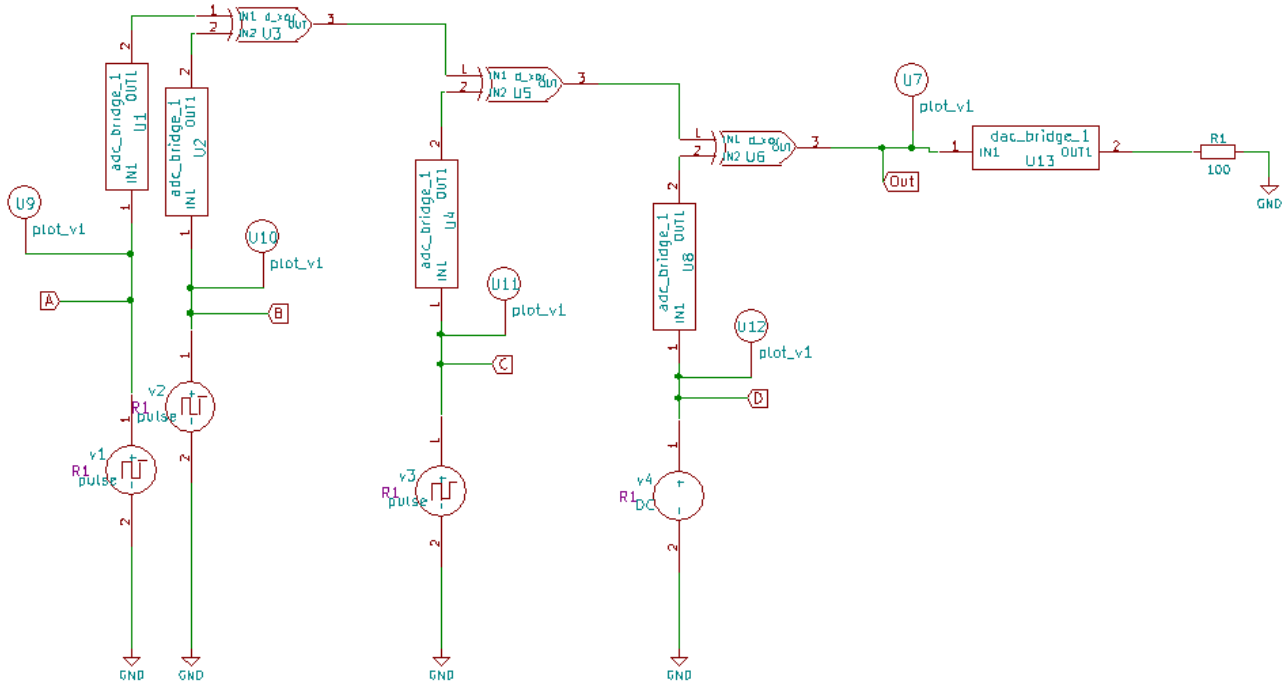
a) A xor B xor C for even parity
b) Not (A xor B xor C) for odd parity

Basically we need only two xor gates, but to have both even and odd parity analyzed easily in one circuit we are adding an extra xor gate. We are going to use the 3rd xor gate as control. We would also be using analog to digital and digital to analog converters.

Basic Diagram:

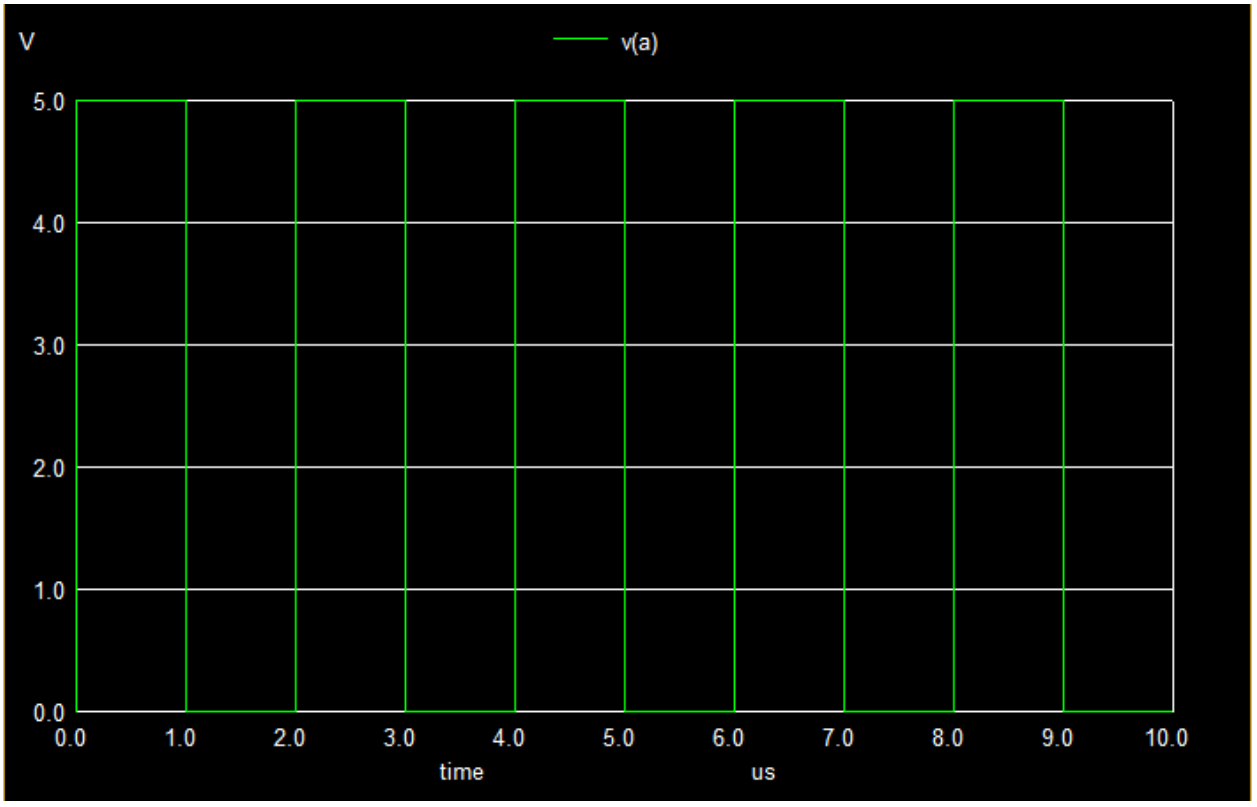


Circuit Diagram:

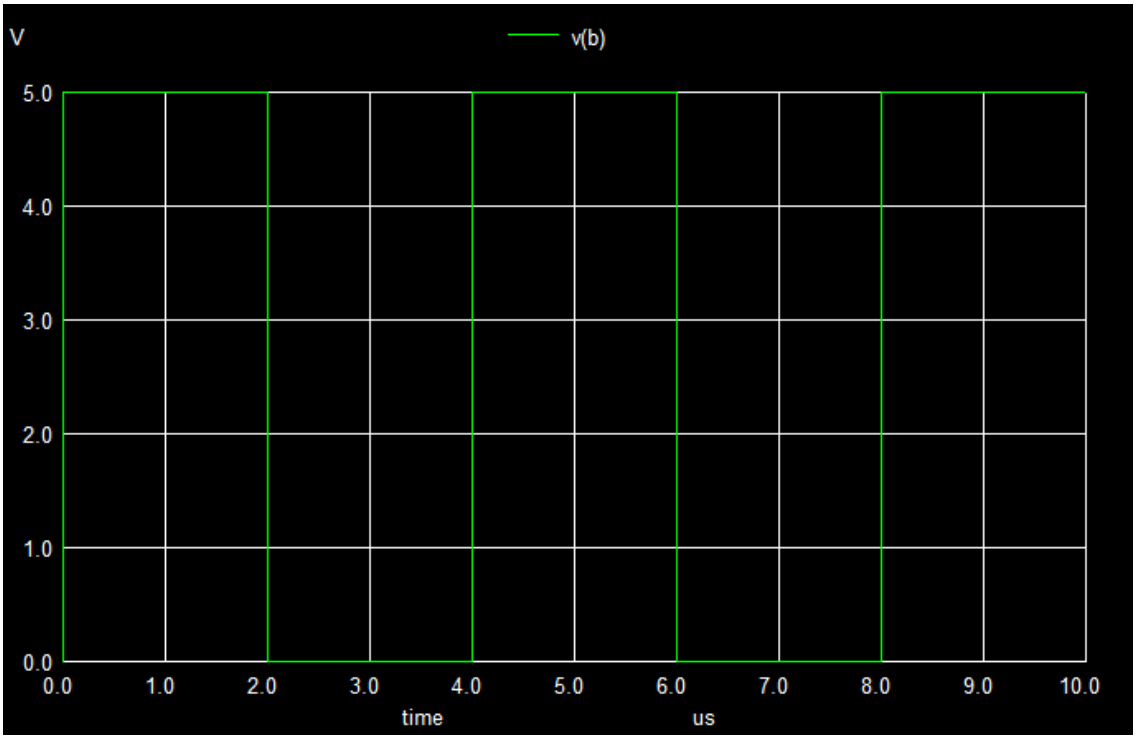


Inputs Ngspice plot:

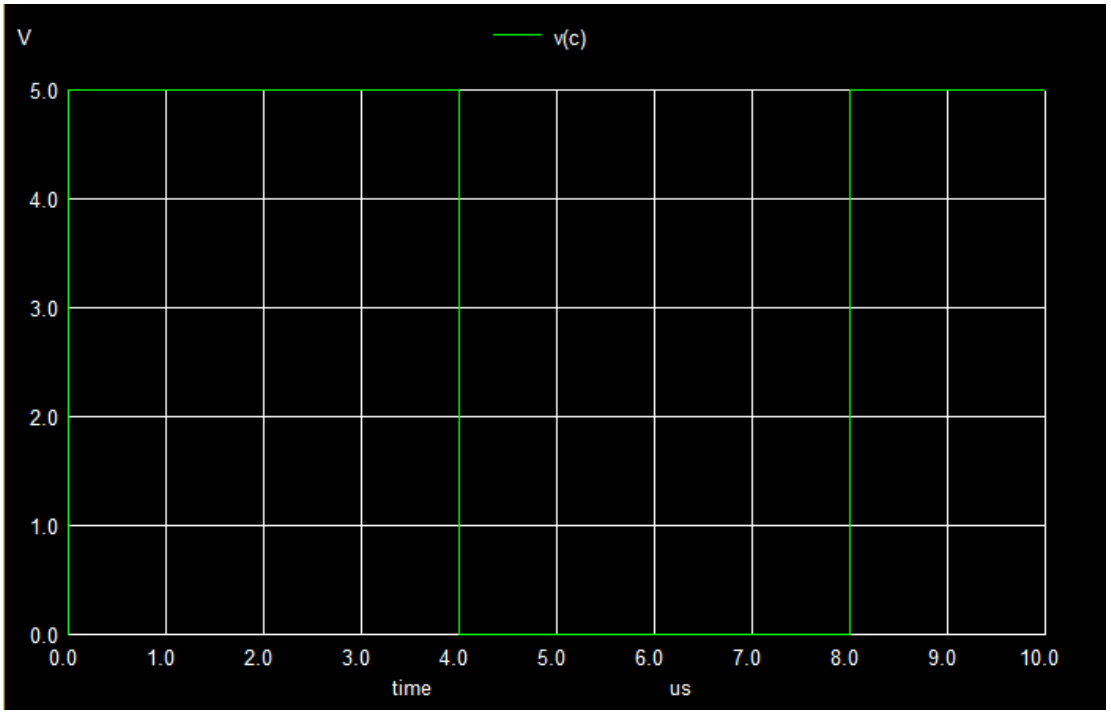
Input A (In analog form)-



Input B (In analog form)-



Input C (In analog form)-

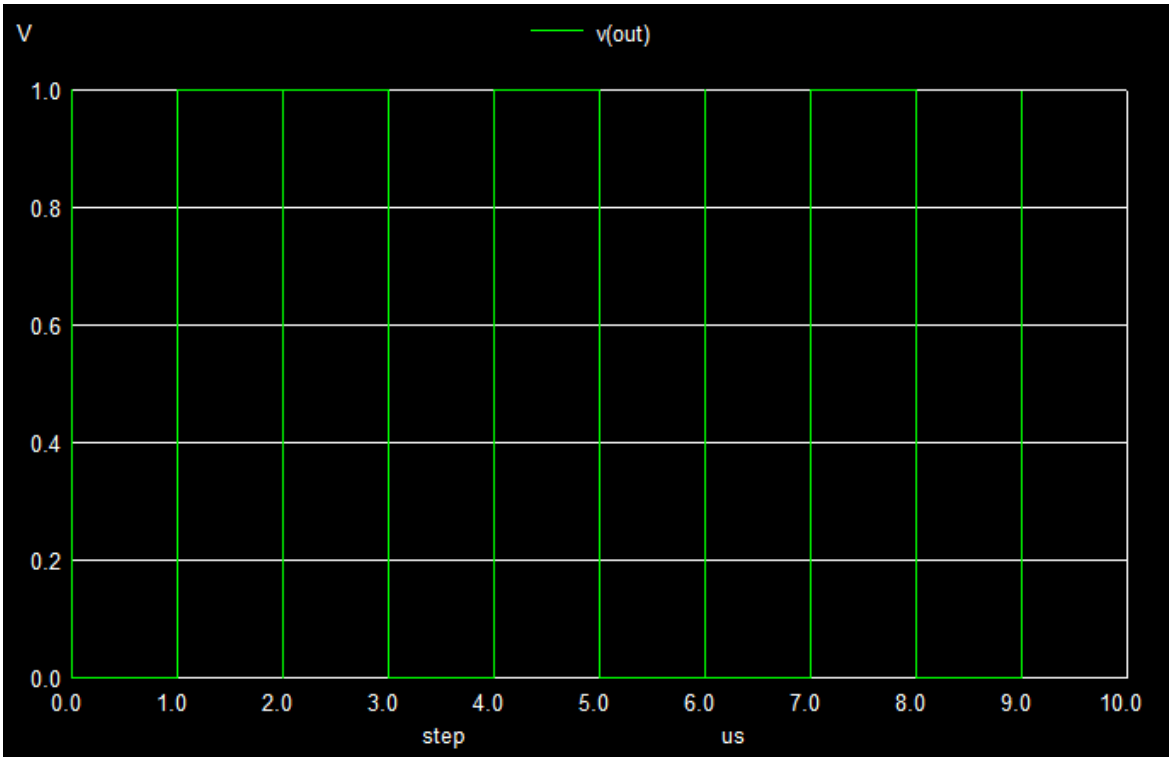


V4-

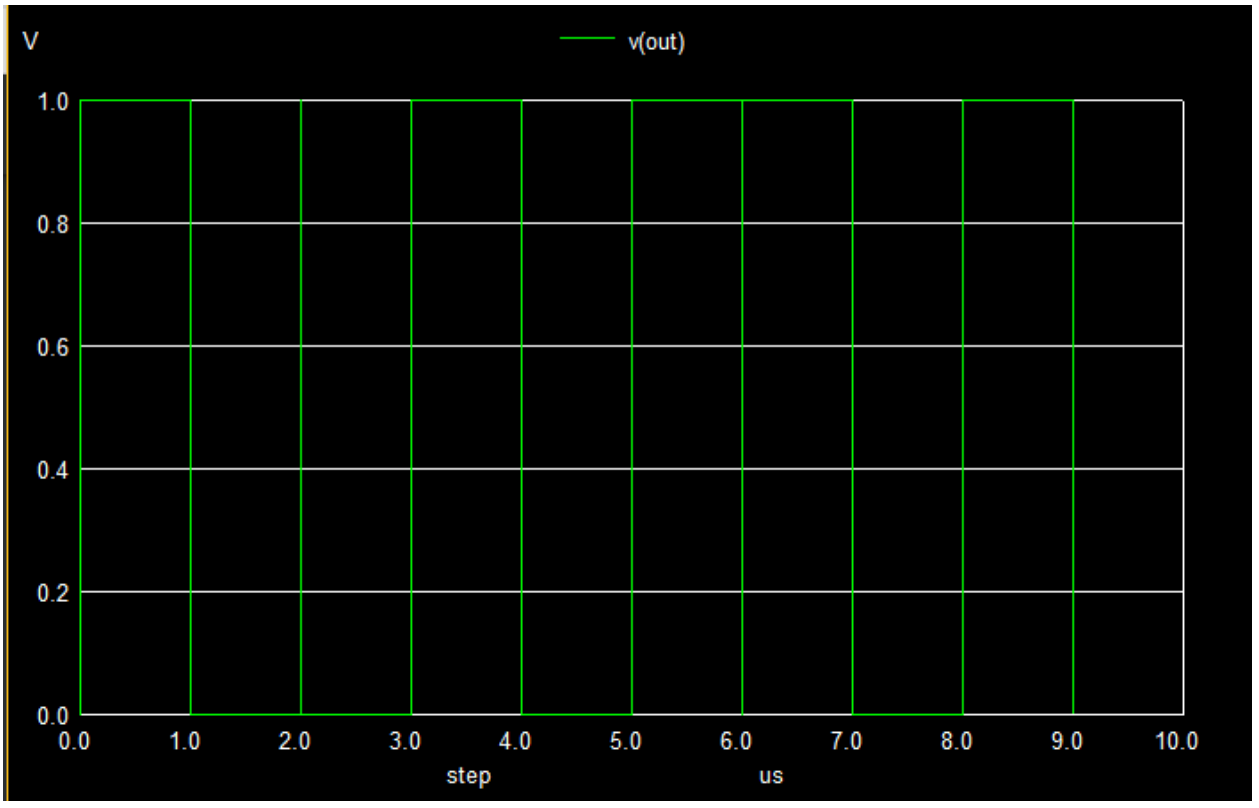
DC value is 0V for even parity generator and 5V for odd parity generator

Output (Digital form)

1) **When voltage = 5v (Odd parity generator output)**



2) **When voltage = 0v (Even parity generator output)**



Conclusion –

Both even and odd parity generator is simulated and outputs are obtained. Theoretical and simulated outputs are matched hence verifying the outputs are correct. Also, the characteristics of both even and odd parity generator are studied and analyzed.

It is also observed here that how by changing the V4 i.e DC voltage value we can transform the circuit to either even or odd parity generator.

Source/Reference(s):

https://www.electrical4u.com/parity- generator/

https://www.youtube.com/playlist?li st=PLlsls0FaKVbJ_59K5muC9ZFh WOHo4frGs

https://youtu.be/Au0BHHRhcUU

https://en.wikipedia.org/wiki/XOR_g ate