



Circuit Simulation Project

https://esim.fossee.in/circuit-simulation-project

Design of 4-Bit Braun Multiplier using Kogge-Stone Adder

by

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THEORY/DESCRIPTION :

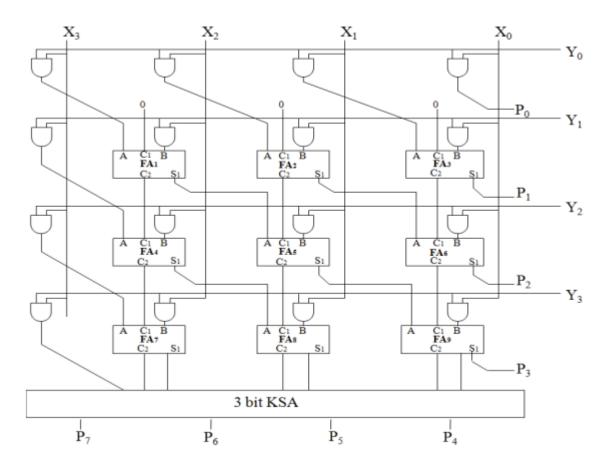
Multiplication is an important fundamental arithmetic operation. It is commonly used in digital signal processing applications and contributes to significant amount of delay. A multiplier is a basic block of any processor that achieves multiplication and a huge boost in performance can be achieved by enhancing the performance of a multiplier.

Over time, computational needs have increased and hence the demand for a parallel array multiplier that can achieve high speed and meet the performance demands has also increased.

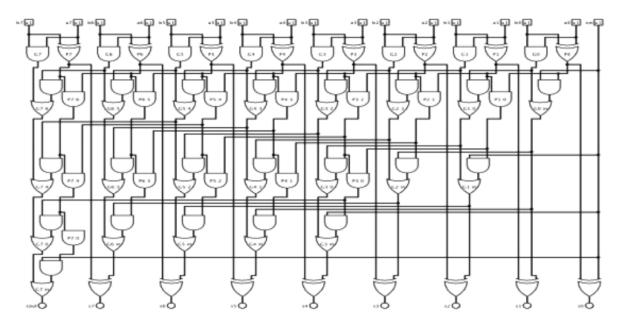
Braun multiplier is a type of parallel array multiplier that meets the above mentioned needs. This architecture can be further enhanced by using a very fast parallel prefix adder like Kogge-Stone instead of a ripple carry adder. This enables reduced delay and faster performance. Kogge-Stone adder belongs to the family of parallel prefix adders.

An n bit Braun multiplier requires $(n-1)^2$ full adders, n^2 AND gates and (n-1) bit Kogge Stone Adder. Each partial product is added to the sum of previous partial product.

CIRCUIT DIAGRAM(S) :



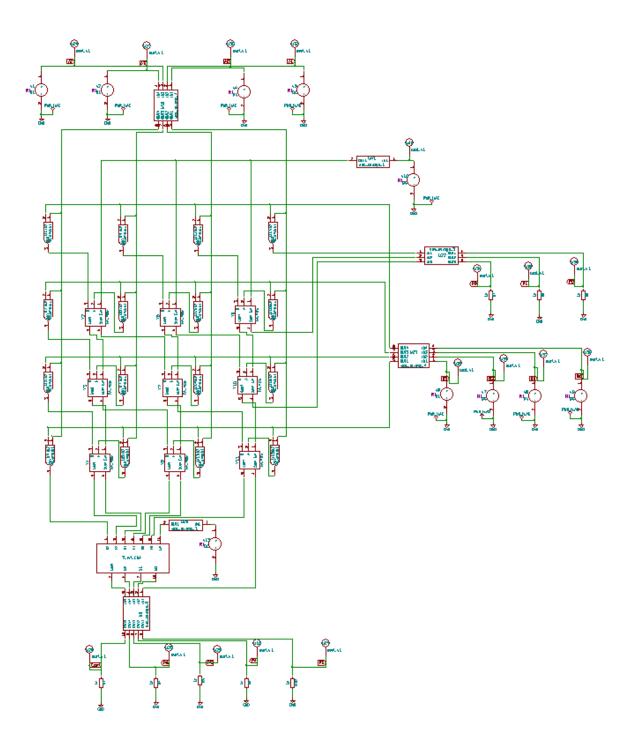
Braun multiplier with KSA



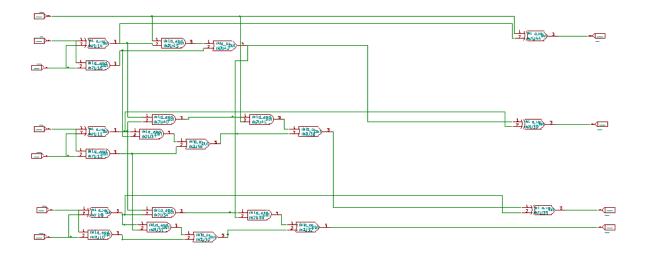
8 bit Kogge-Stone Adder

SCHEMATIC:

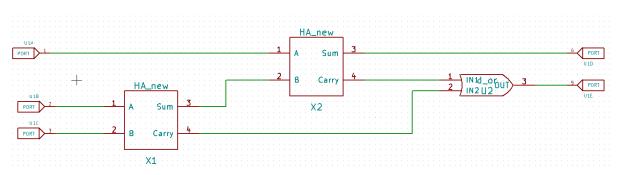
4 bit Braun multiplier using Kogge-Stone adder



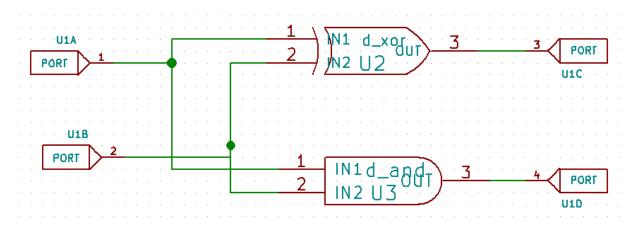
3 bit Kogge-Stone Adder



Full Adder



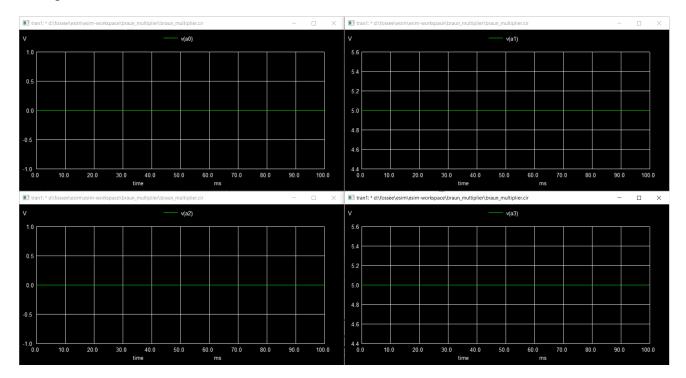
Half Adder



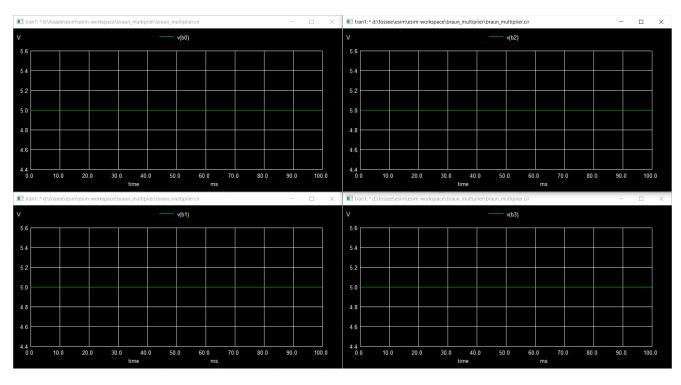
RESULTS:

Ngspice plots

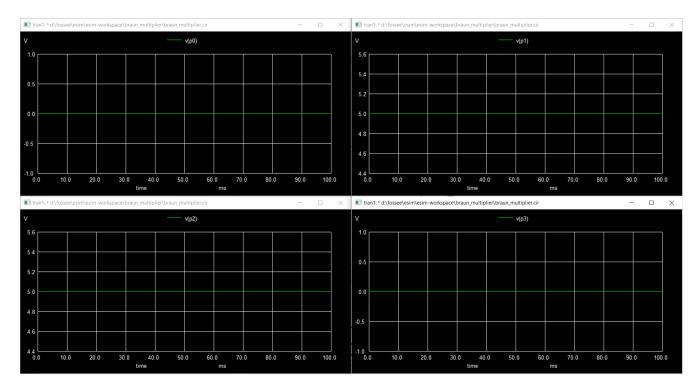
For inputs A = 1010 & B = 1111



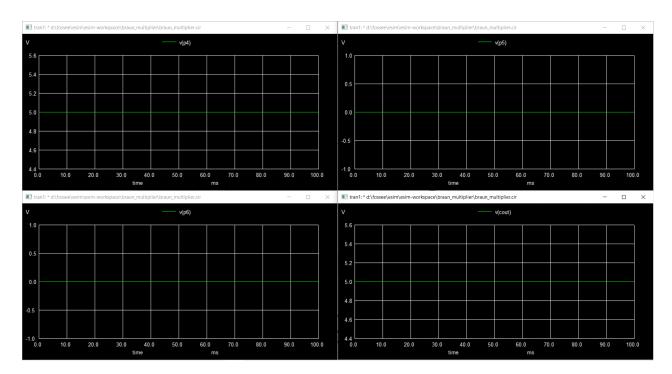
Inputs A (A0, A1, A2, A3)



Inputs B (B0, B1, B2, B3)

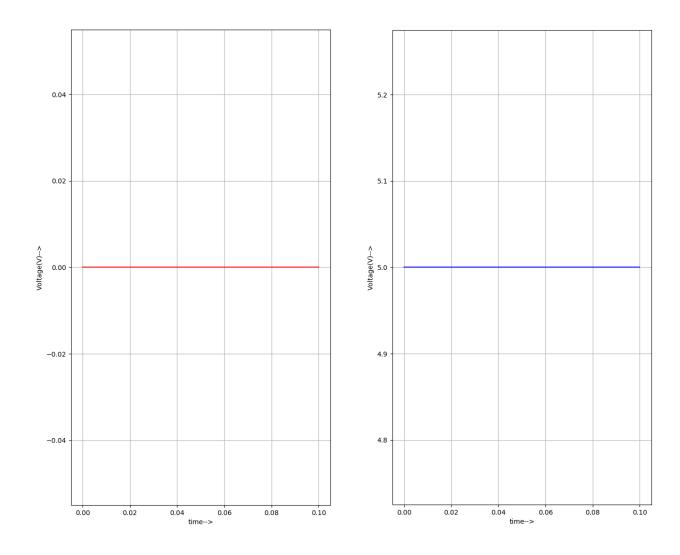






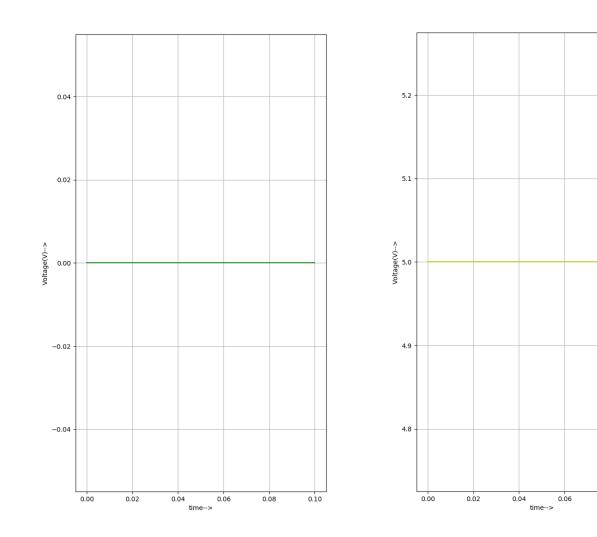
Outputs (P4, P5, P6, Cout)

Python plots



A0

A1

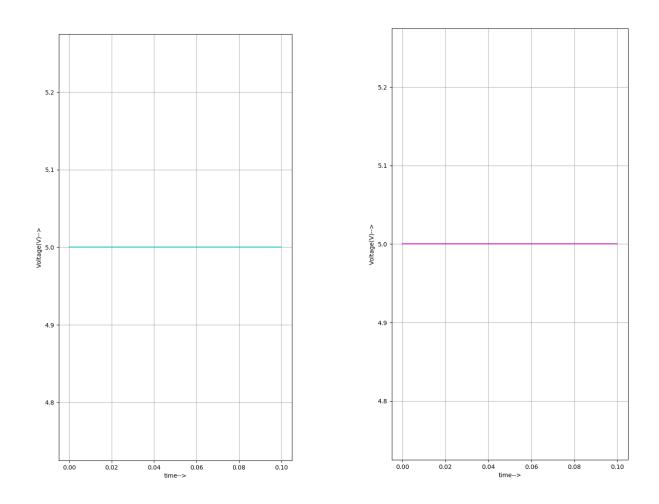


A2

A3

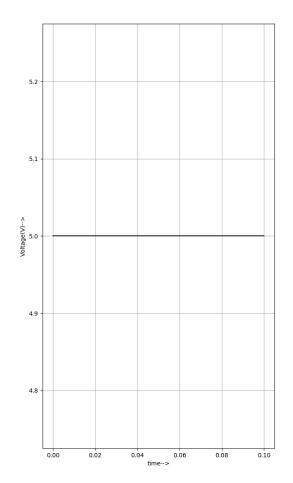
0.08

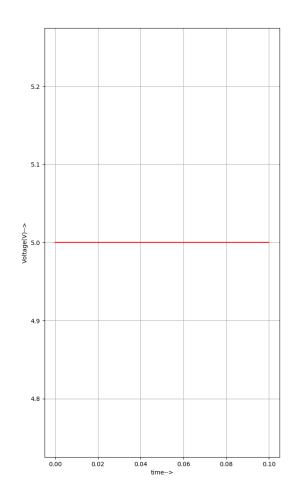
0.10



BO

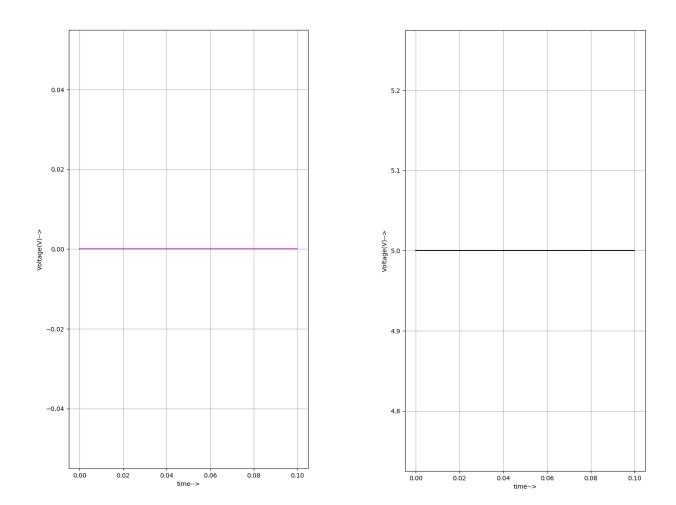






B2

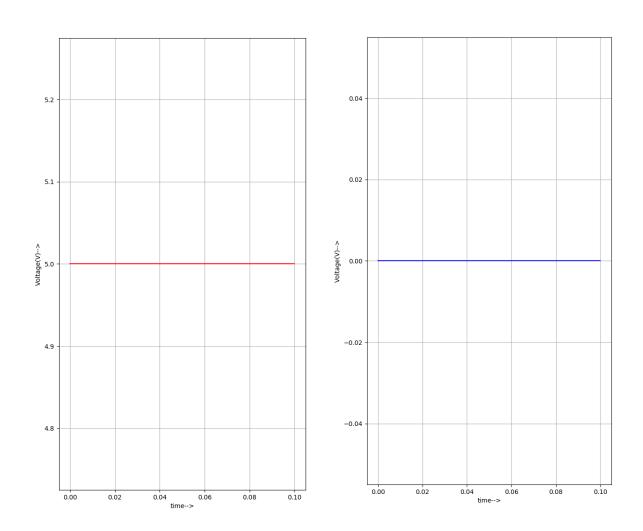




PO

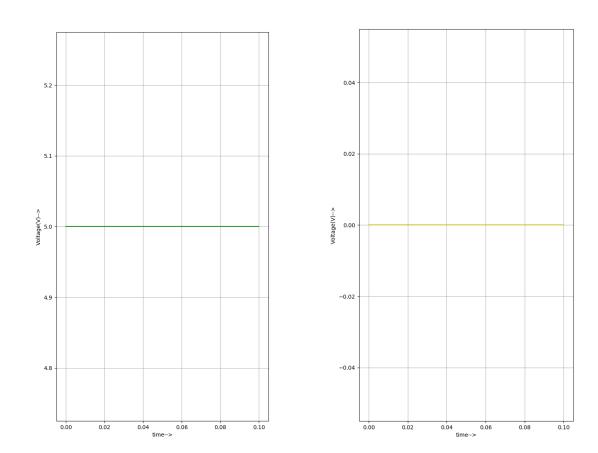


U



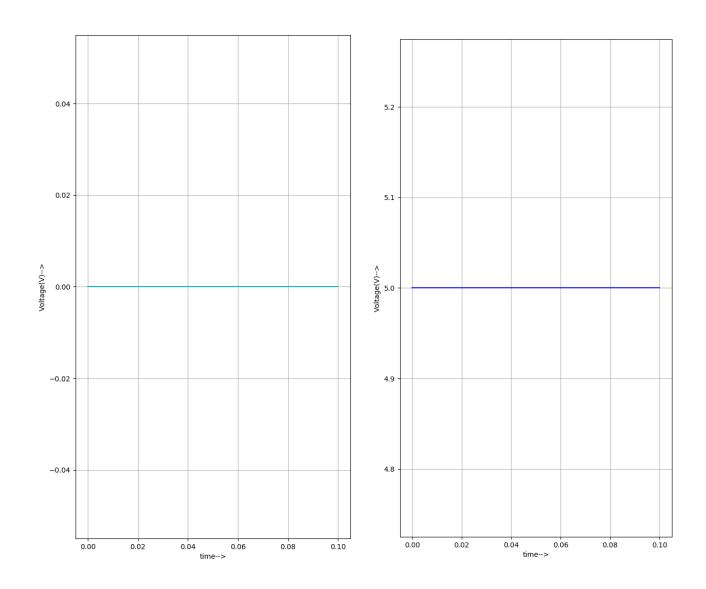
P2

P3



P4

P5



P6

Cout

В				Α				Product							
B3	B2	B1	B0	A3	A2	A1	A0	Cout	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1	0	0	0	0	0	0	1	0
0	0	1	0	0	0	1	0	0	0	0	0	0	1	0	0
0	0	1	1	0	0	1	1	0	0	0	0	0	1	1	0
0	1	0	0	0	1	0	0	0	0	0	0	1	0	0	0
0	1	0	1	0	1	0	1	0	0	0	0	1	0	1	0
0	1	1	0	0	1	1	0	0	0	0	0	1	1	0	0
0	1	1	1	0	1	1	1	0	0	0	0	1	1	1	0
1	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0
1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	1

The following table displays a list of some of the possible inputs along with the obtained outputs.

REFERENCES:

- Design and performance analysis of multipliers using Kogge Stone Adder : <u>https://ieeexplore.ieee.org/document/8389113</u>
- Modeling, Design and Performance Analysis of Various 8-bit Adders for Embedded Applications - Kunjan D. Shinde and Jayashree C. Nidagundi : https://www.researchgate.net/publication/303997659_Modeling_Design_and_Performance_Analysis_of_Various_8-bit_Adders_for_Embedded_Applications
- Kogge-Stone Adder : <u>https://en.wikipedia.org/wiki/Kogge%E2%80%93Stone_adder</u>