Dr.Maheswari.R

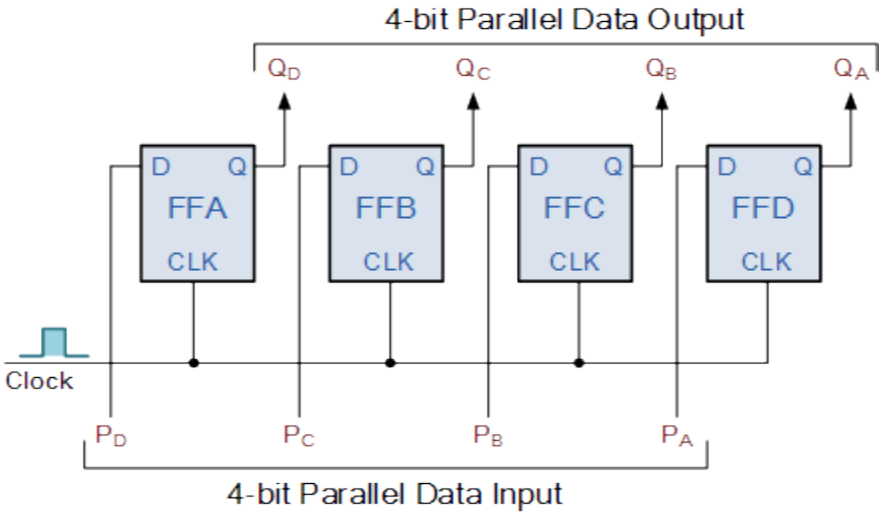
TITLE OF THE EXPERIMENT -

4 BIT SYNCHRONOUS PARALLEL IN PARALLEL OUT (PIPO) REGISTER

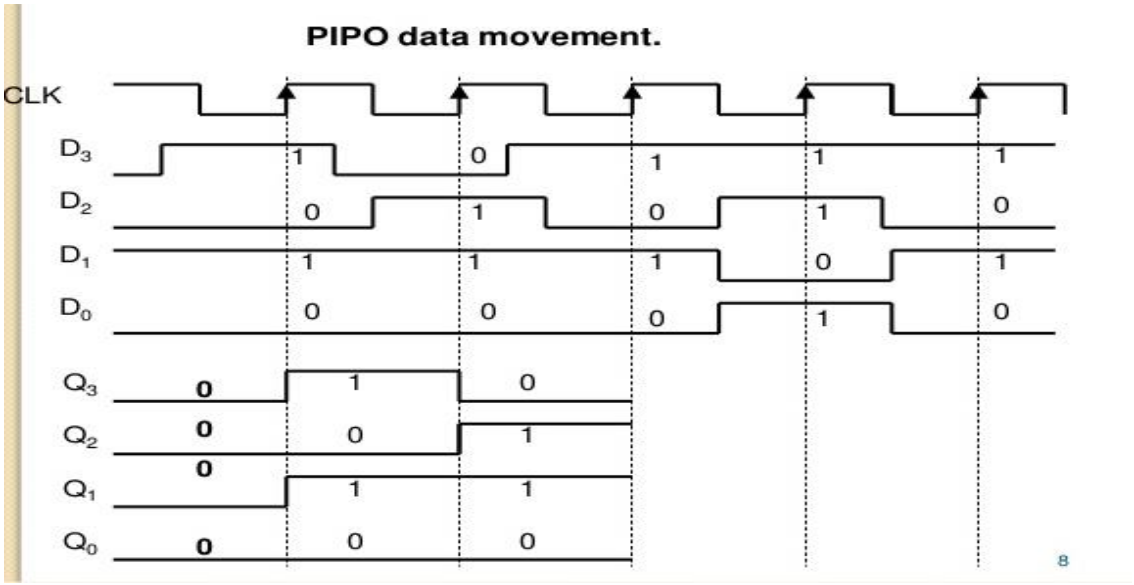
Abstract:

Parallel In Parallel Out (PIPO) registers are the type of storage devices in which both data loading as well as data retrieval processes occur in parallel mode. In PIPO the parallel data is loaded simultaneously into the register, and transferred together to their respective outputs by the same clock pulse. This type of shift register also acts as a temporary storage device or as a time delay device, with the amount of time delay being varied by the frequency of the clock pulses. The data is presented in a parallel format to the parallel input pins P_A to P_D and then transferred together directly to their respective output pins Q_A to Q_D by the same clock pulse. Then one clock pulse loads and unloads the register. This arrangement for parallel loading and unloading is shown below figure. in this type of register there are no interconnections between the individual flip-flops since no serial shifting of the data is required.

Circuit Diagram:



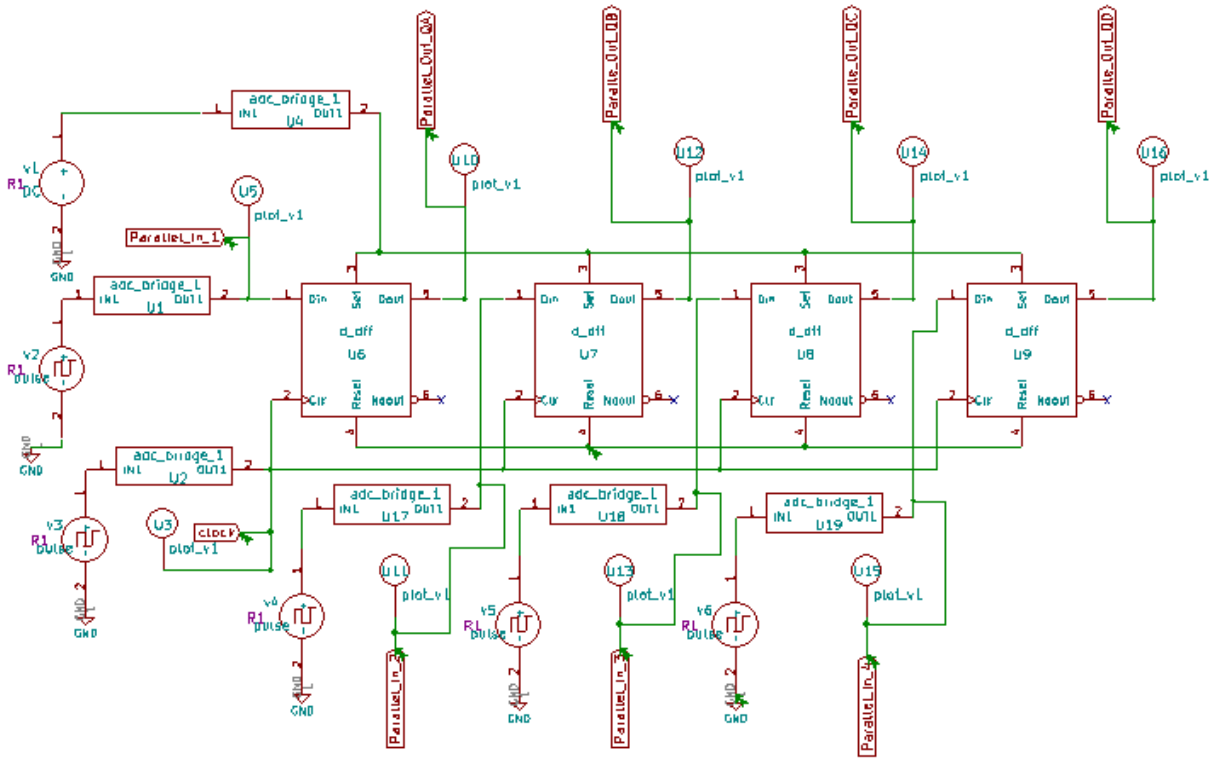
Timing Diagram:



eSim Required Components :

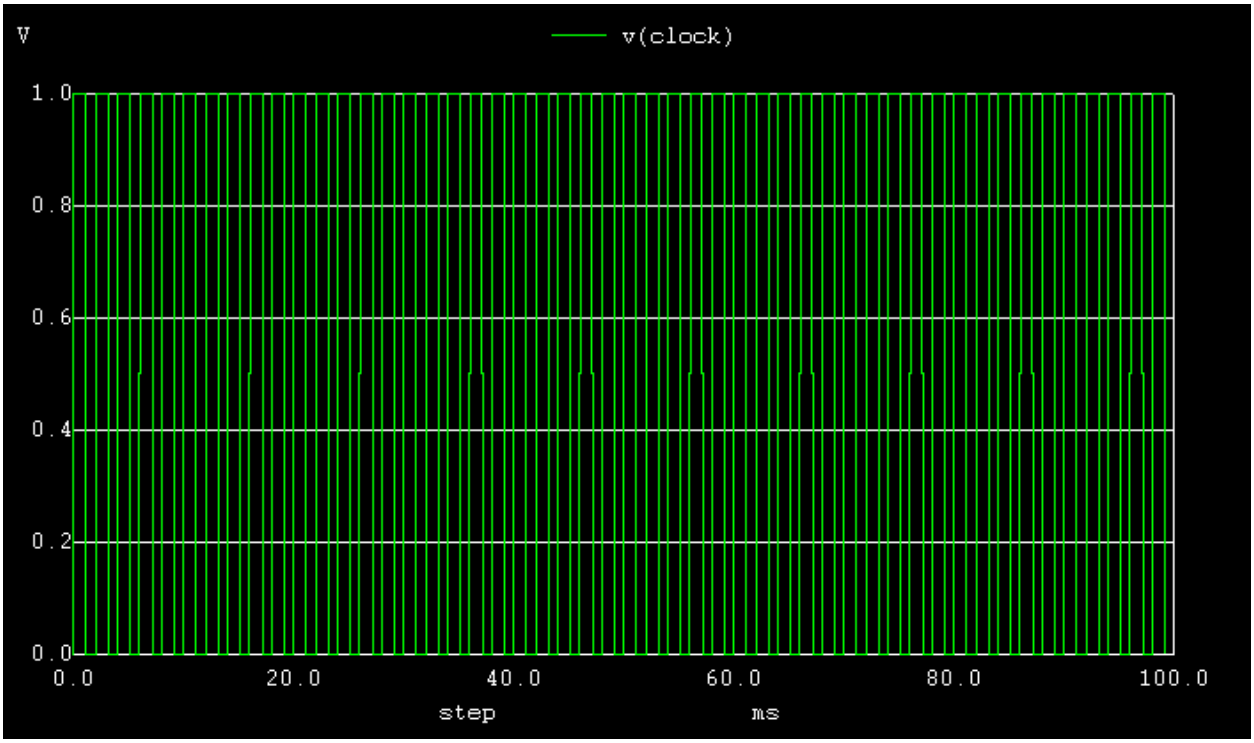
Synchronous up counter	
Component Name	**Type**
d_dff	d flip flop
clock	clock input
DC	dc voltage source for logic 1

ESIM Circuit design snapshot:

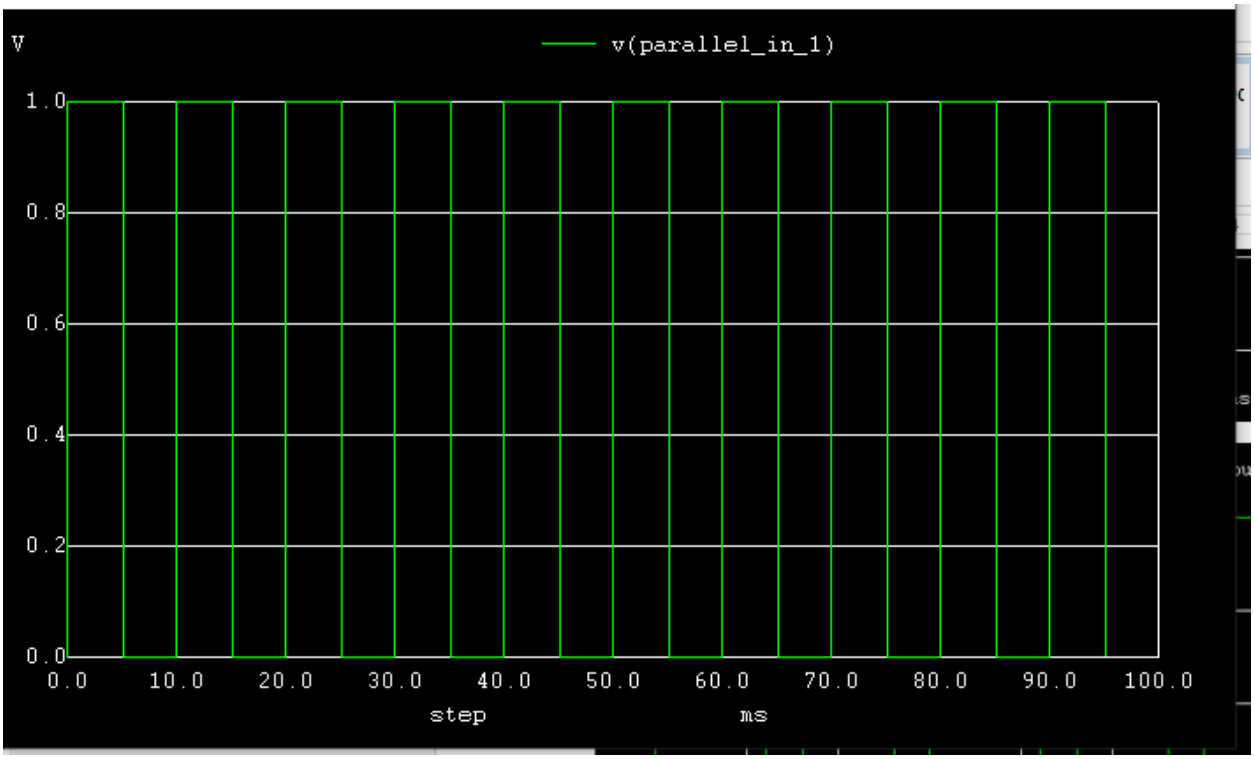


OUTPUT –

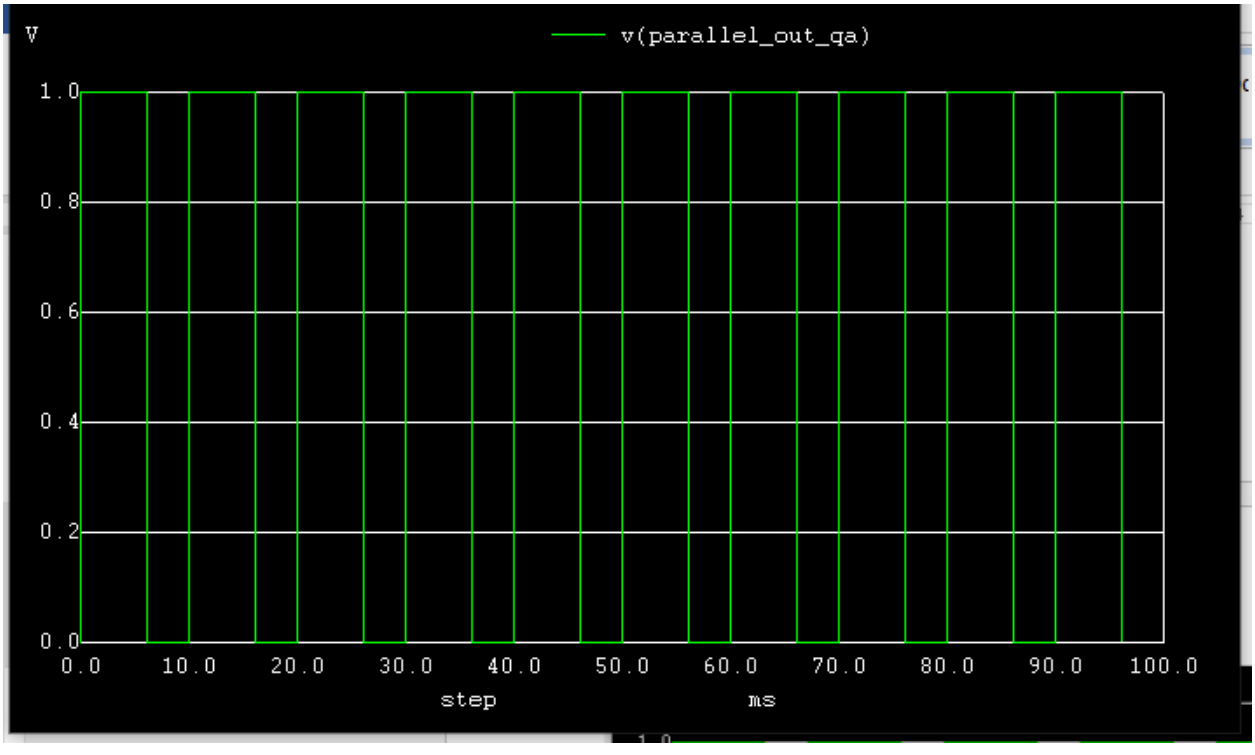
Clock:



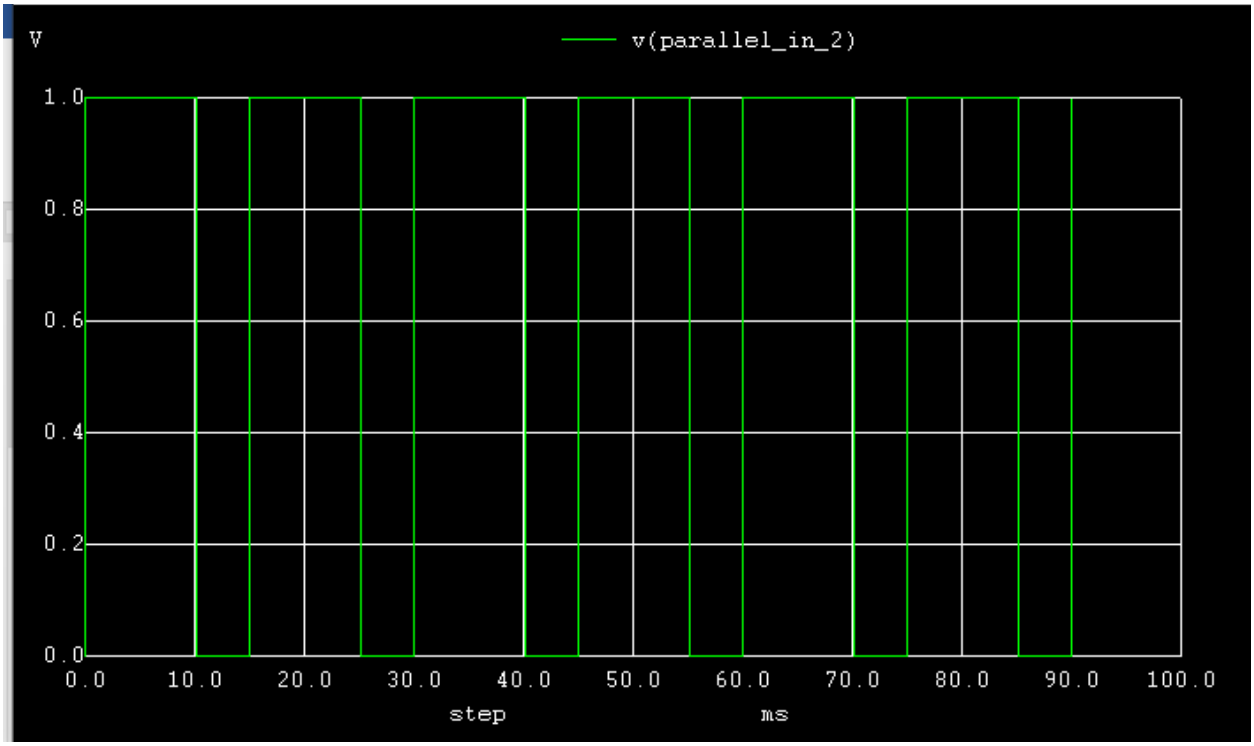
Parallel In 1 (FFA):



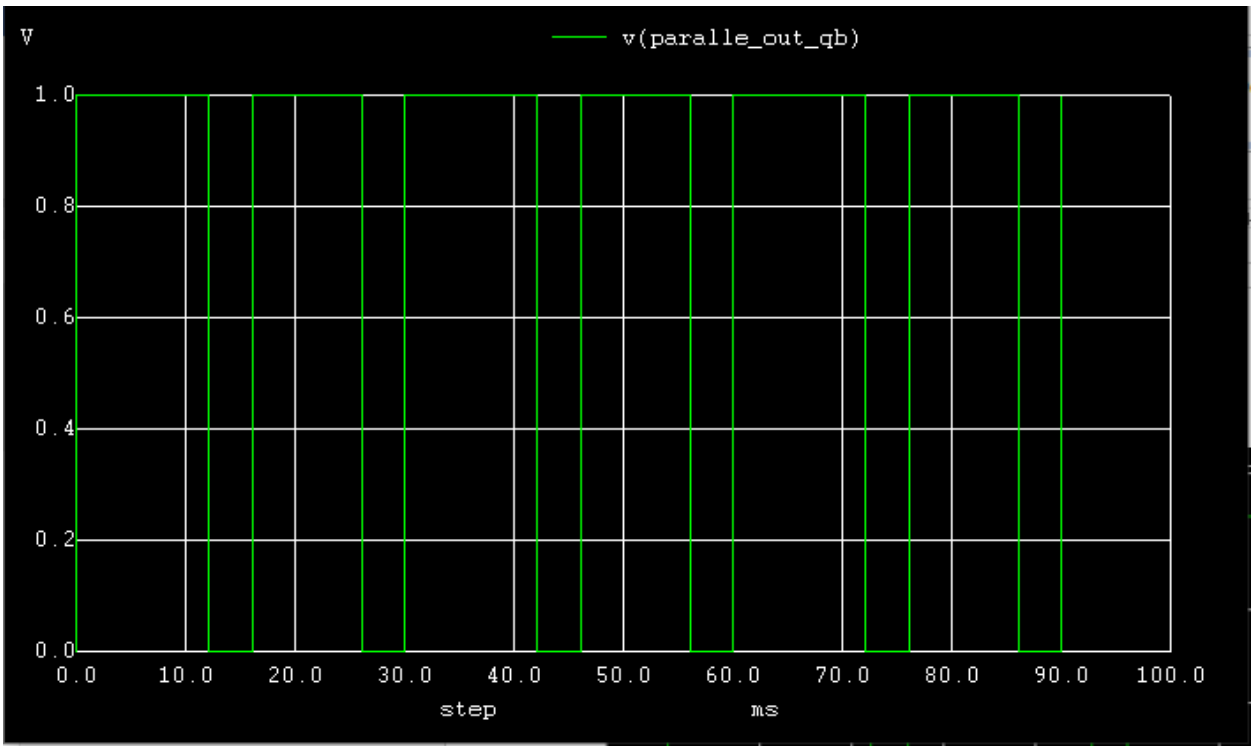
Parallel Out A (FFA):



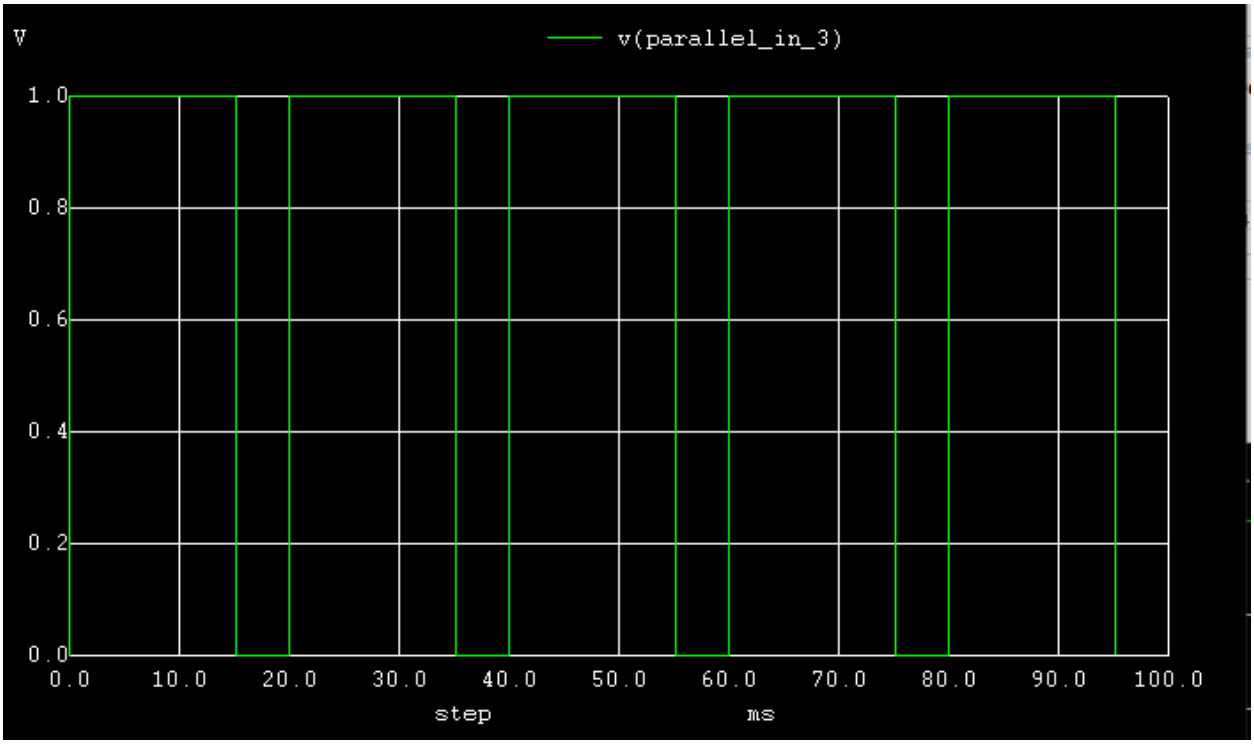
Parallel In 2 (FFB):



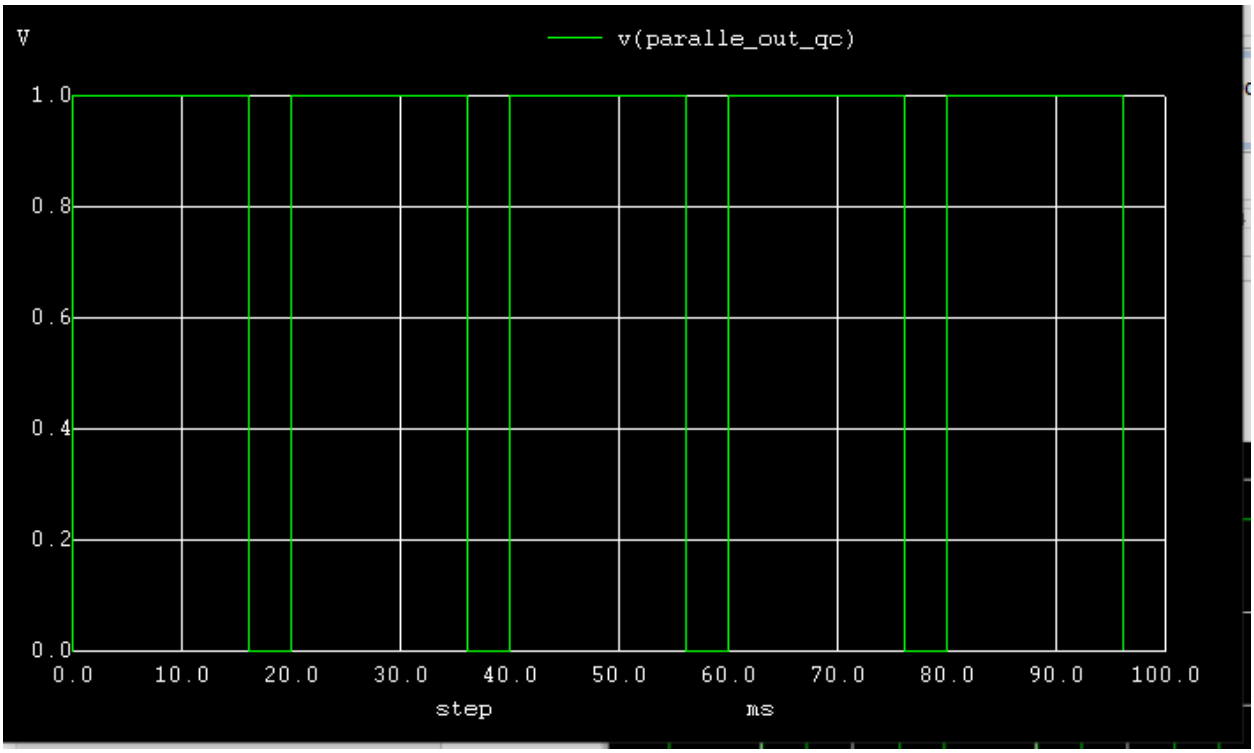
Parallel Out B (FFB):



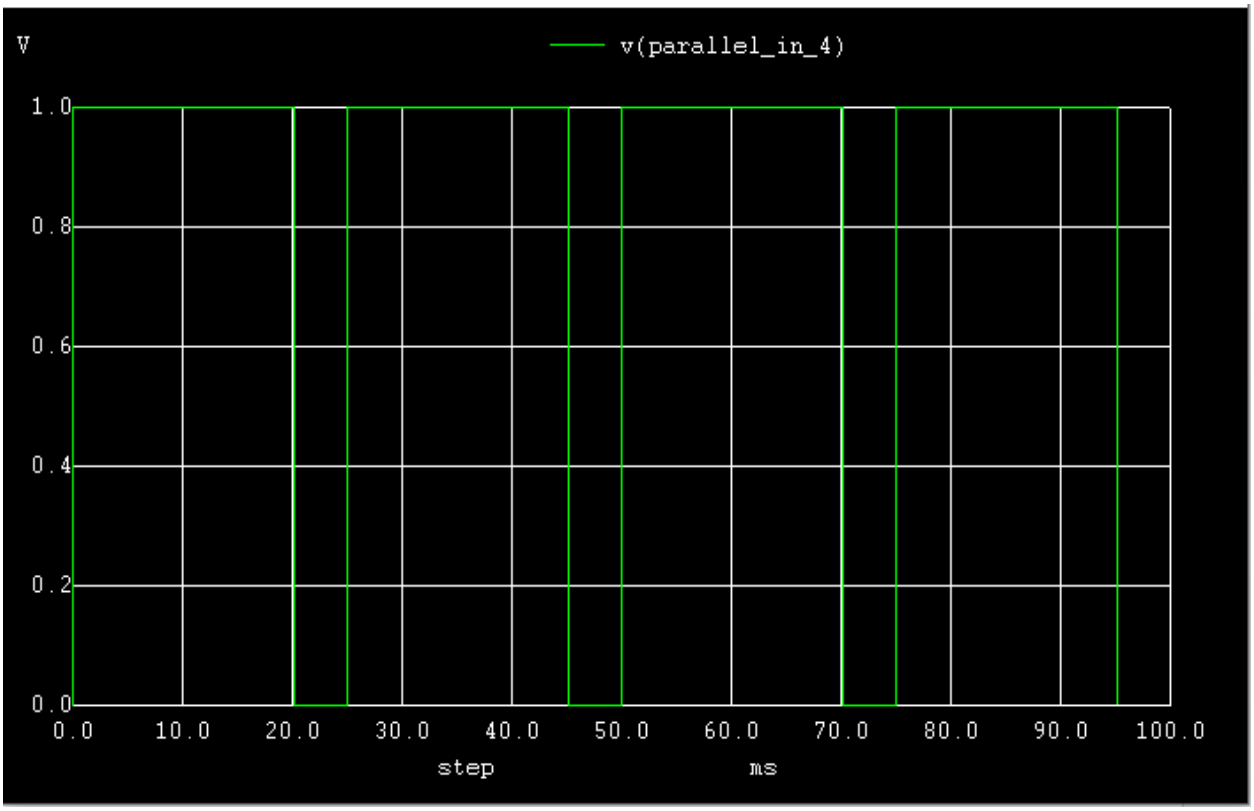
Parallel In 3 (FFC):



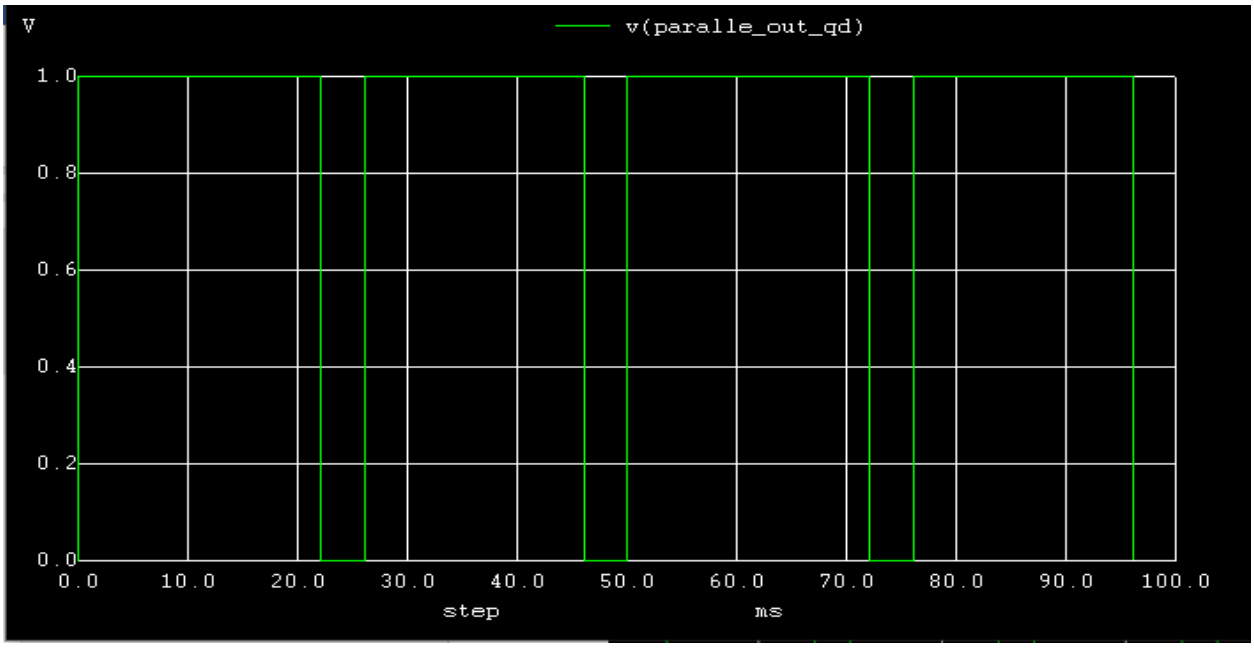
Parallel Out C(FFC):



Parallel In 4 (FFD):



Parallel Out D (FFD):



References:

- https://www.electronics-tutorials.ws/sequential/seq_5.html