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TITLE OF THE EXPERIMENT -

4 BIT SYNCHRONOUS SERIAL IN PARALLEL OUT SHIFT REGISTER

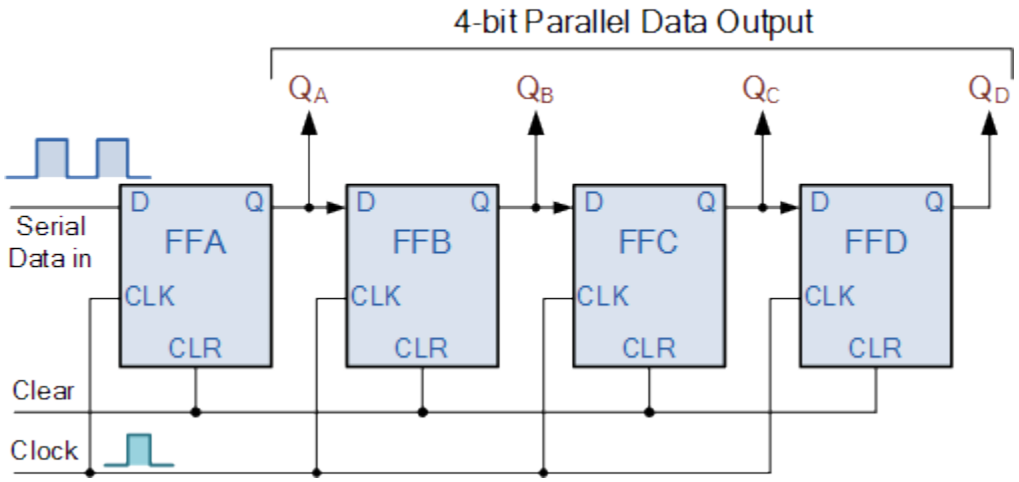
Abstract:

Shift Register is a sequential device which loads the data present on its inputs and then moves or “shifts” it to its output once every clock cycle. Serial-in Parallel-out (SIPO) the register is loaded with serial data, one bit at a time, with the stored data being available at the output in parallel form. If a logic “1” is connected to the DATA input pin of FFA then on the first clock pulse the output of FFA and therefore the resulting QA will be set HIGH to logic “1” with all the other outputs still remaining LOW at logic “0”. Assume now that the DATA input pin of FFA has returned LOW again to logic “0” giving us one data pulse or 0-1-0. The second clock pulse will change the output of FFA to logic “0” and the output of FFB and QB HIGH to logic “1” as its input D has the logic “1” level on it from QA. The logic “1” has now moved or been “shifted” one place along the register to the right as it is now at QA. When the third clock pulse arrives this logic “1” value moves to the output of FFC (QC) and so on until the arrival of the fifth clock pulse which sets all the outputs QA to QD back again to logic level “0” because the input to FFA has remained constant at logic level “0”.

The effect of each clock pulse is to shift the data contents of each stage one place to the right, and this is shown in the following table until the complete data value of 0-0-0-1 is stored in the register. This data value can now be read directly from the outputs of QA to QD. Then the data has been converted from a serial data input signal to a parallel data output. The truth table and following waveforms show the propagation of the logic “1” through the register from left to right as follows.

The circuit consists of four D flip-flops which are connected in a serial manner. All these flip-flops are synchronous with each other since the same clock signal is applied to each flip flop.

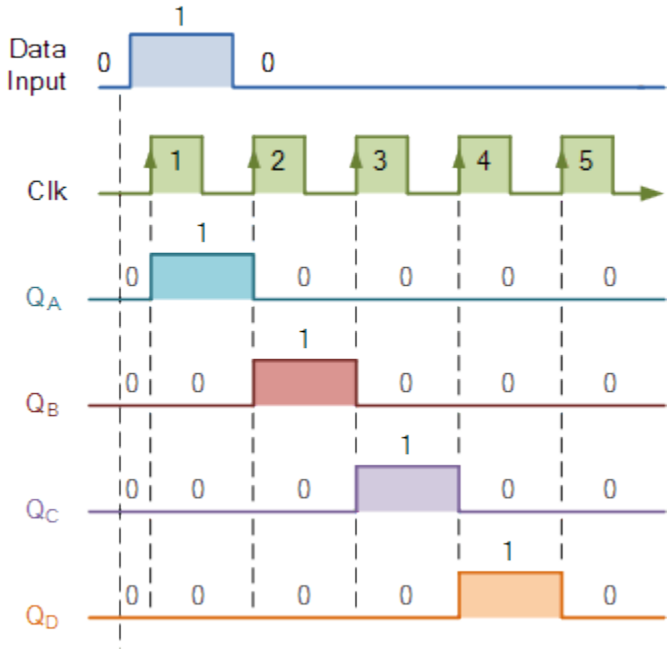
Circuit Diagram:



Truth Table:

Clock Pulse No	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	0	0	0	0

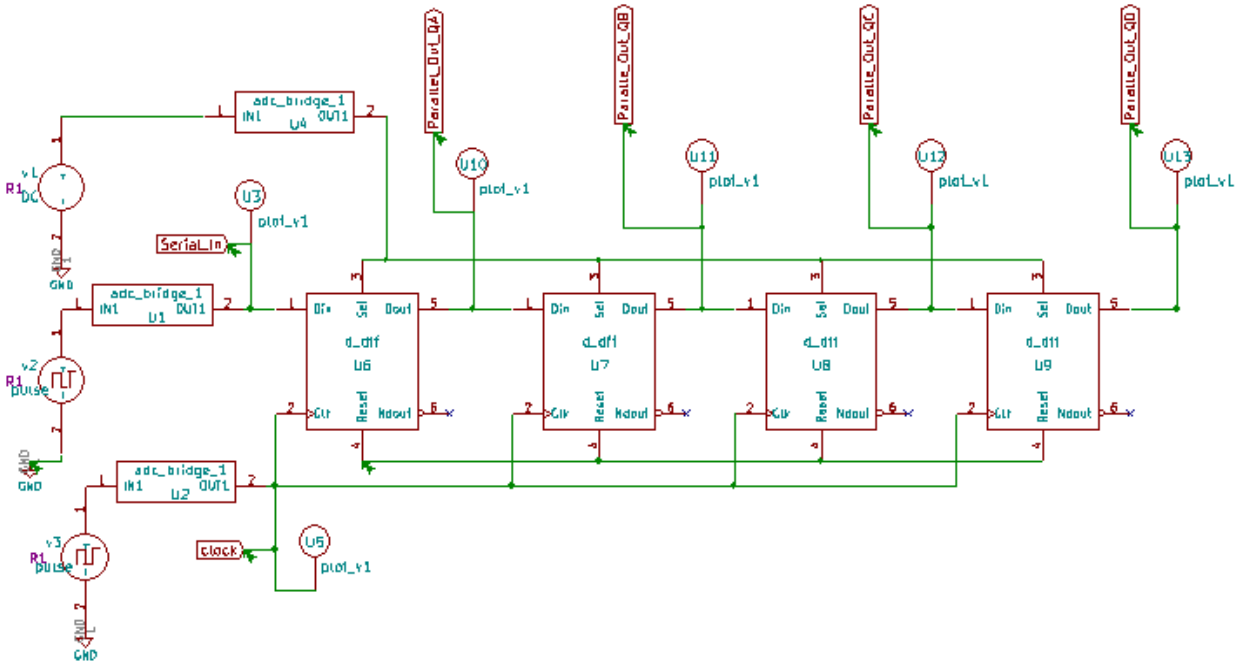
Timing Diagram:



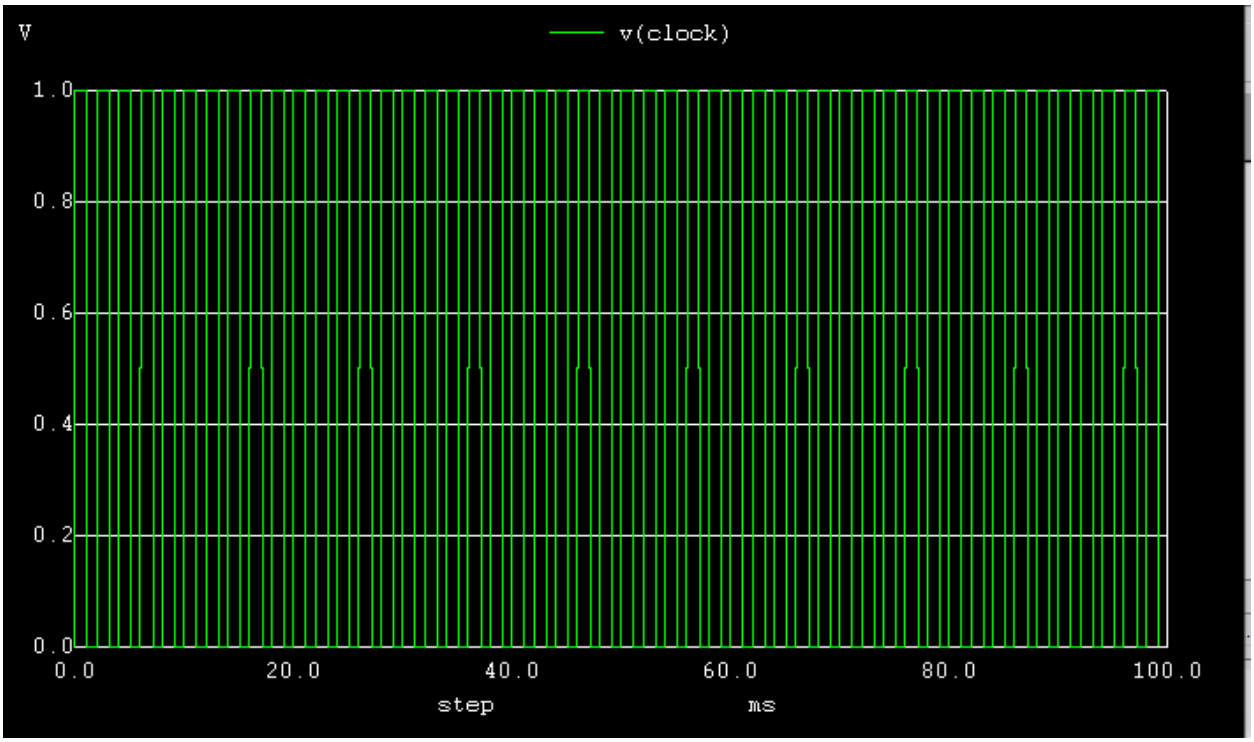
eSim Required Components :

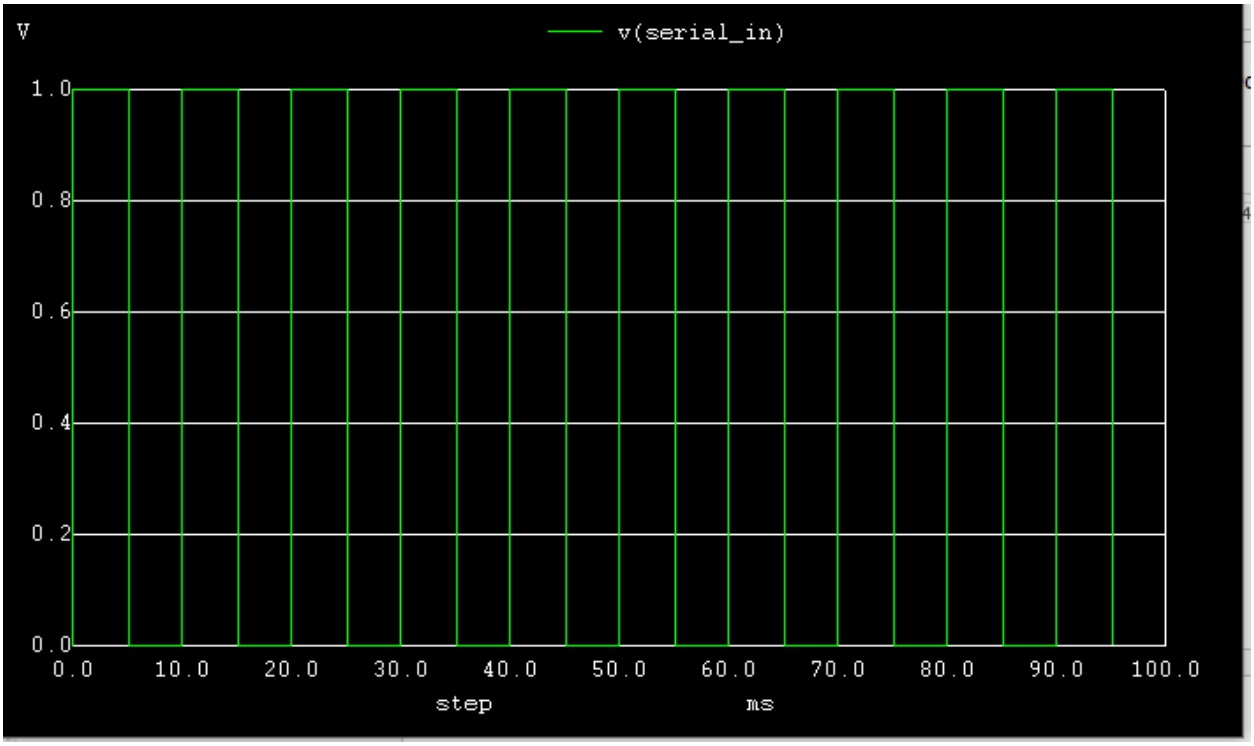
Synchronous up counter	
Component Name	**Type**
d_dff	d flip flop
clock	clock input
DC	dc voltage source for logic 1

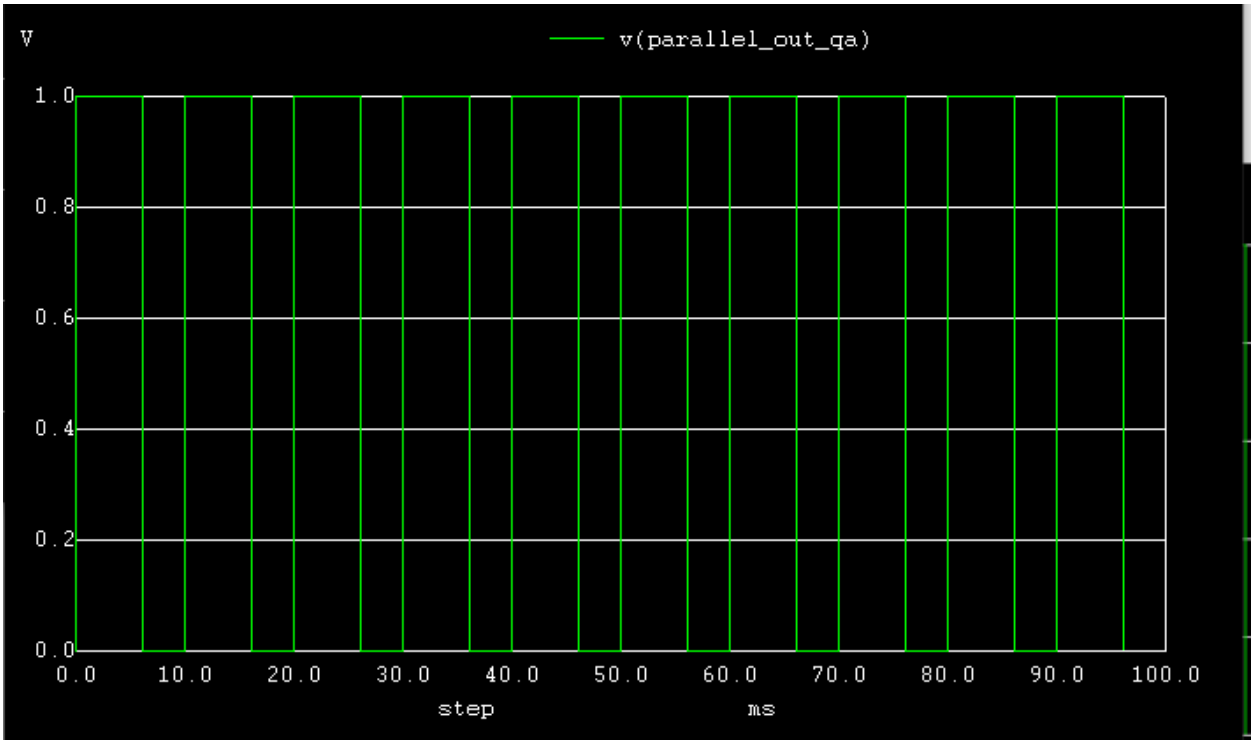
ESIM Circuit design snapshot:

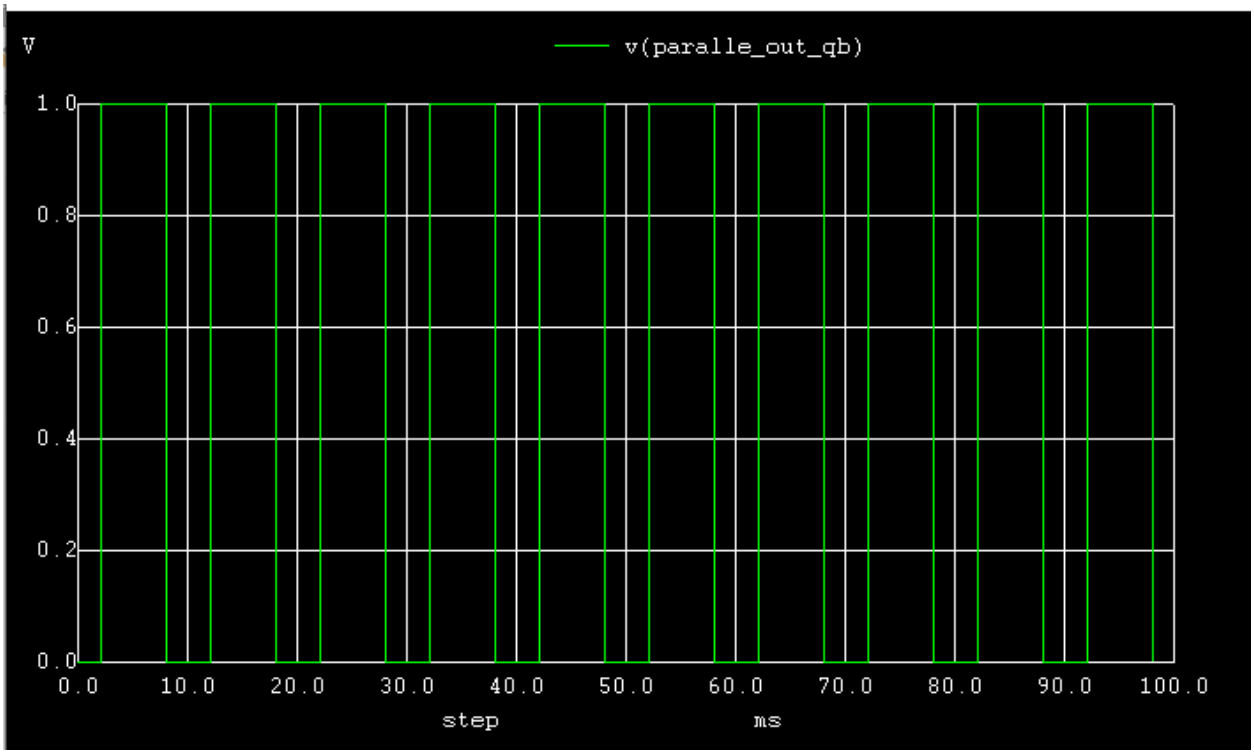


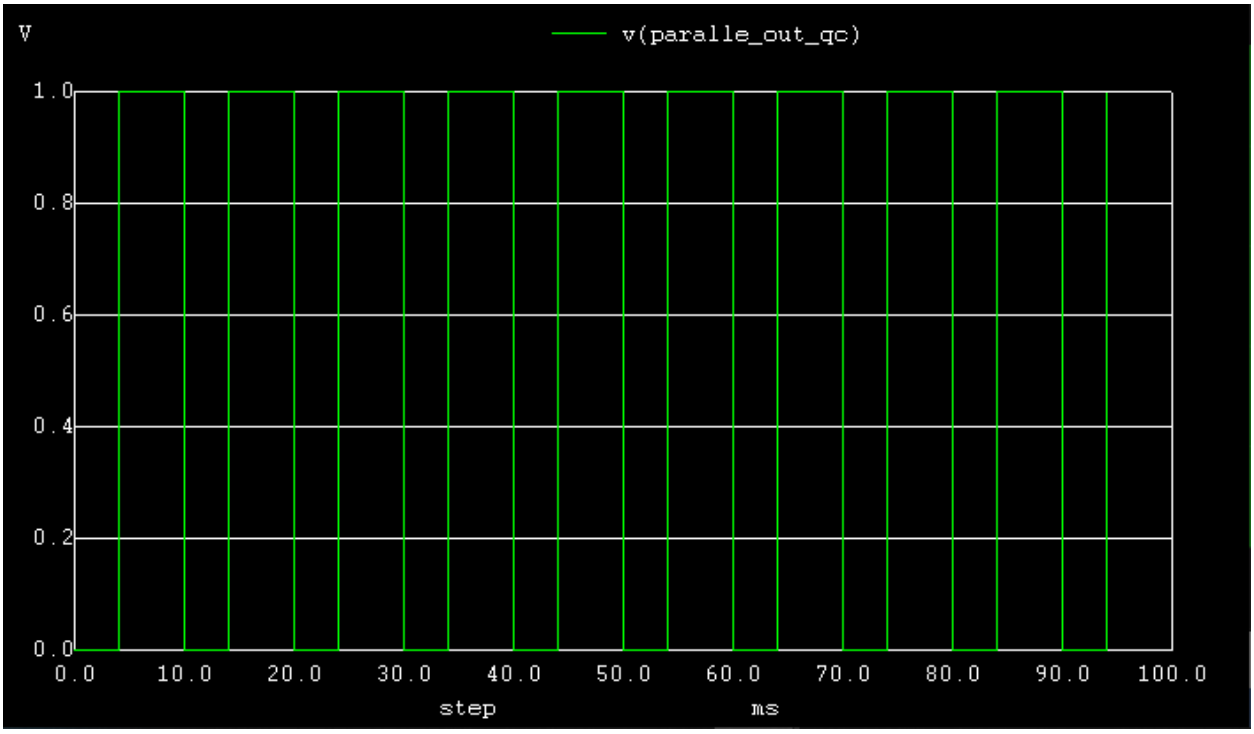
OUTPUT –

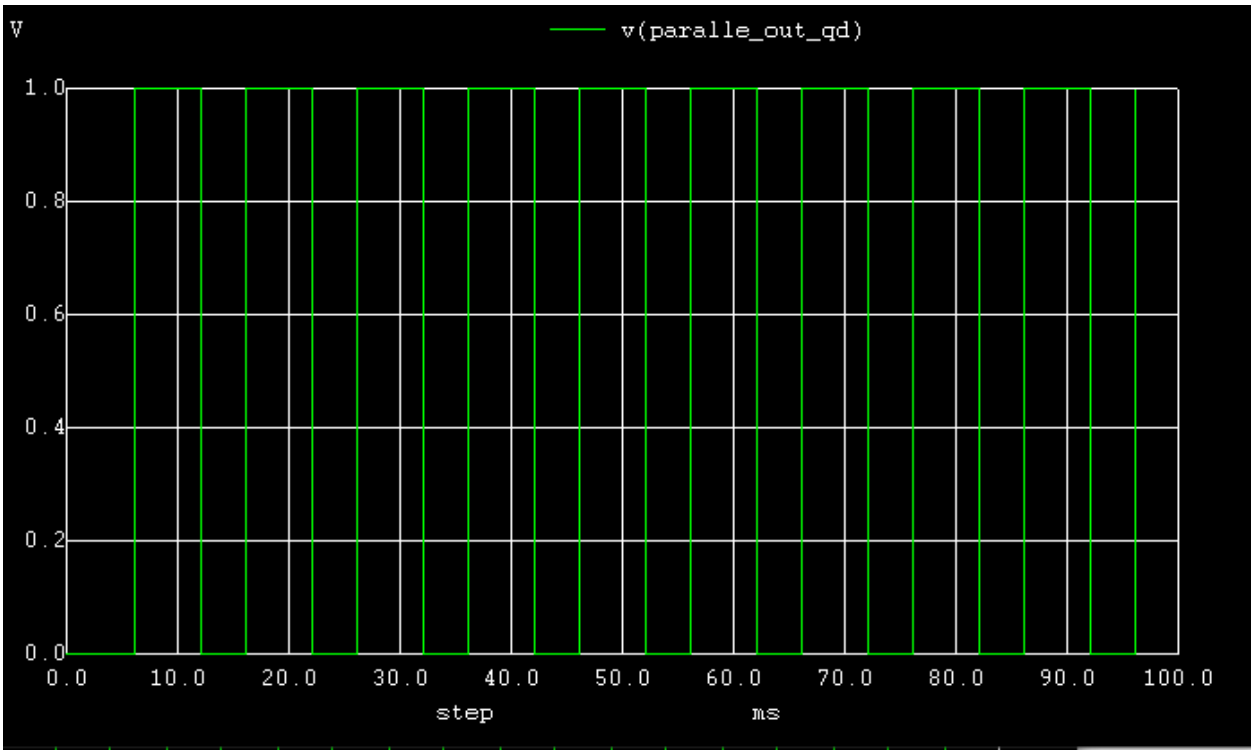



V
v(serial_in)
1.0
0.8
0.6
0.4
0.2
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
step
ms


V
v(parallel_out_qa)
1.0
0.8
0.6
0.4
0.2
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
step
ms


V
v(paralle_out_qb)
1.0
0.8
0.6
0.4
0.2
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
step
ms


V
v(paralle_out_qc)
1.0
0.8
0.6
0.4
0.2
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
step
ms



References:

- https://www.electronics-tutorials.ws/sequential/seq_5.html