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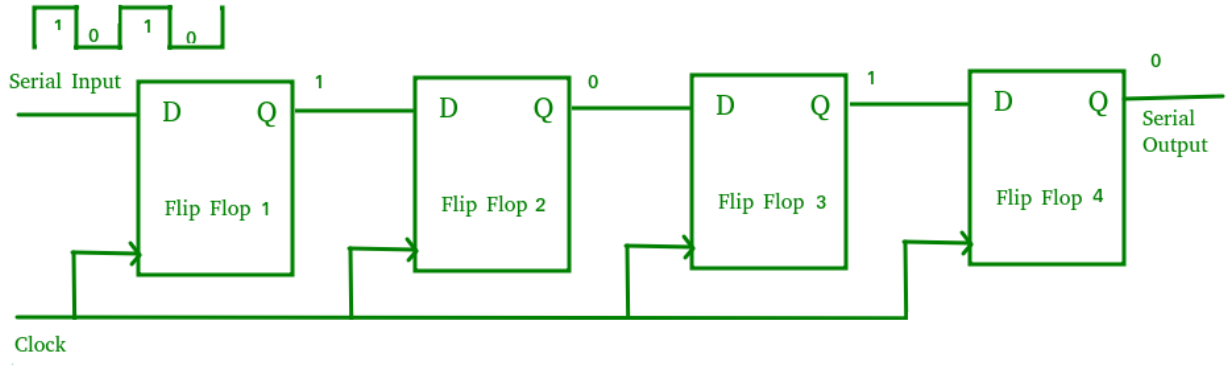
TITLE OF THE EXPERIMENT -

4 BIT SYNCHRONOUS SERIAL IN SERIAL OUT SHIFT REGISTER

Abstract:

Shift Register is a group of flip flops used to store / move multiple bits of data. In Serial-in to Serial-out (SISO) shift register the data is shifted serially "IN" and "OUT" of the register, one bit at a time in either a left or right direction under clock control. It allows serial input i.e. one bit after the other through a single data line and produces a serial output. There is only one output, the data leaves the shift register one bit at a time in a serial pattern. The circuit consists of four D flip-flops which are connected in a serial manner. All these flip-flops are synchronous with each other since the same clock signal is applied to each flip flop.

Circuit Diagram:

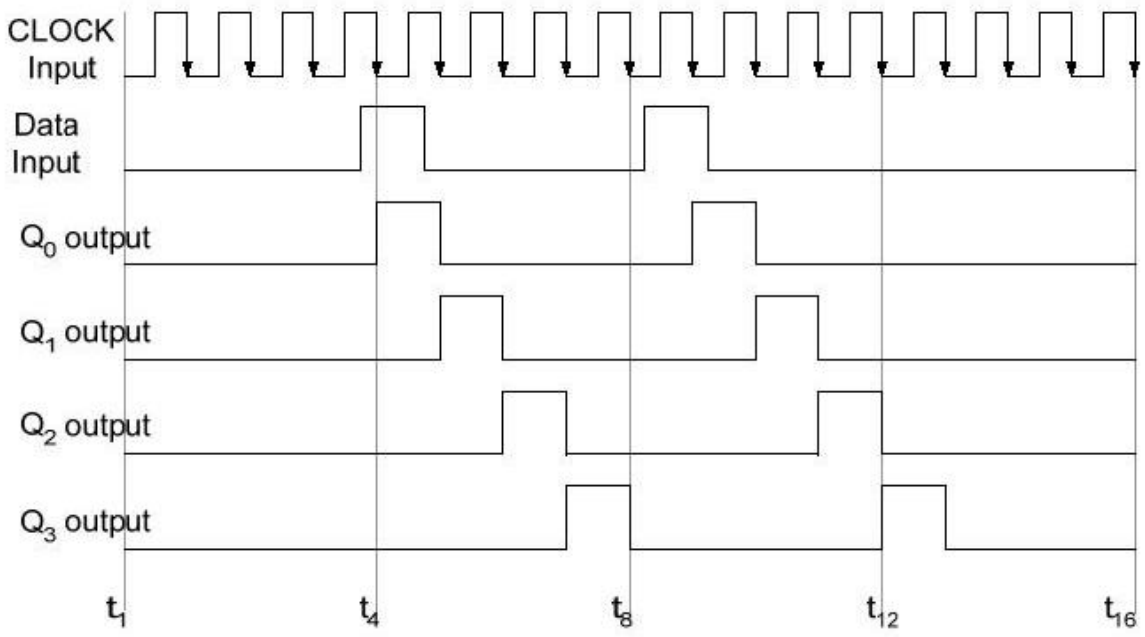


Truth Table:

Operation of the Shift-right Register

Timing pulse	Q_A	Q_B	Q_C	Q_D	*Serial output at* Q_D
Initial value	0	0	0	0	0
After 1st clock pulse	1	0	0	0	0
After 2nd clock pulse	1	1	0	0	0
After 3rd clock pulse	0	1	1	0	0
After 4th clock pulse	1	0	1	1	1

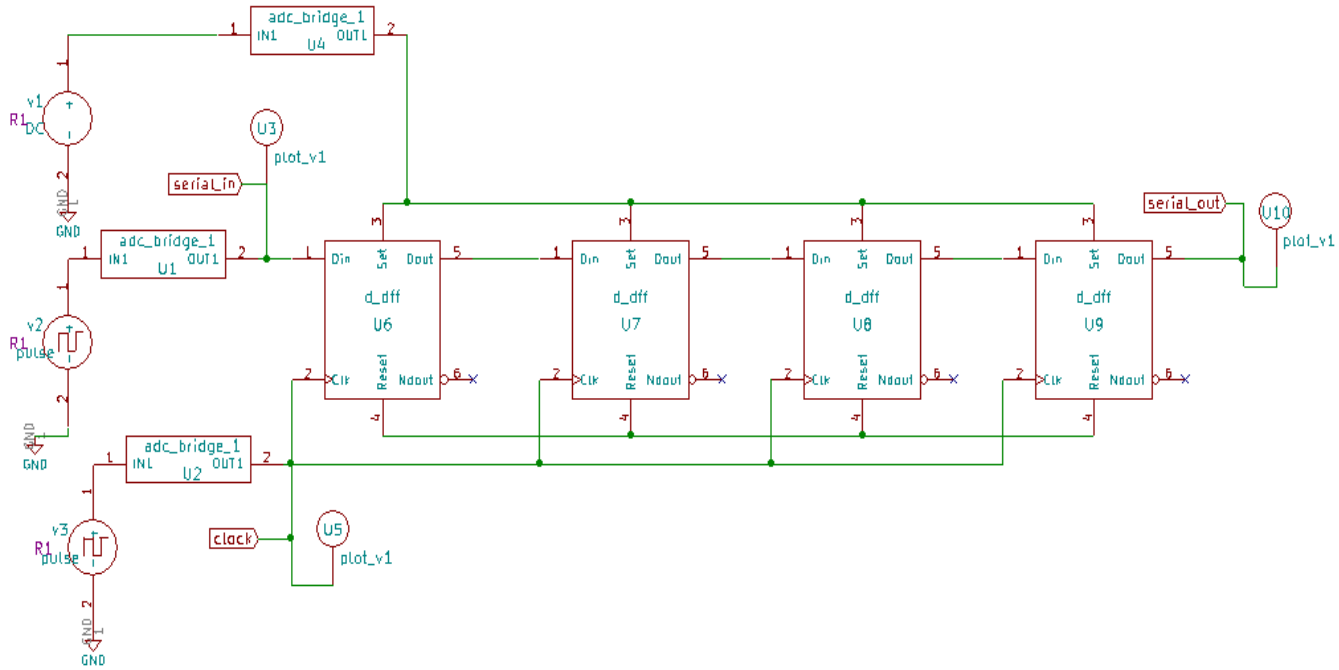
Timing Diagram:



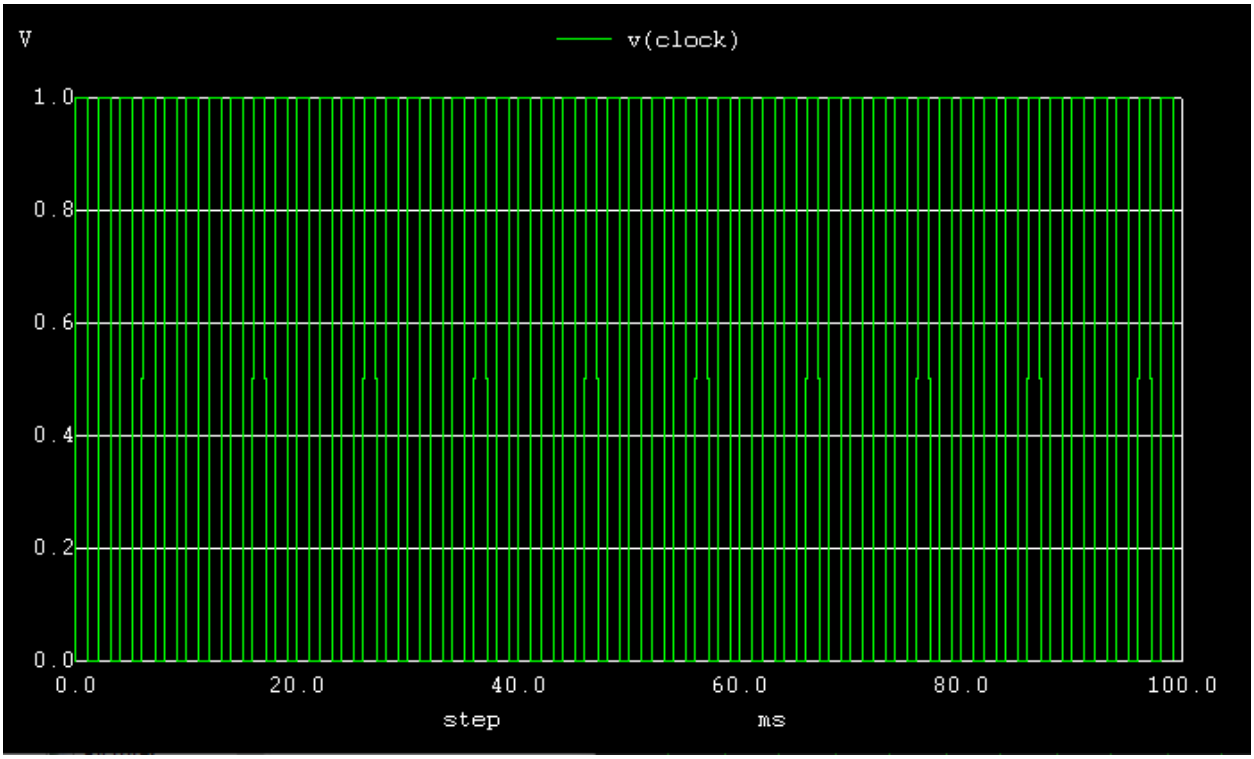
eSim Required Components :

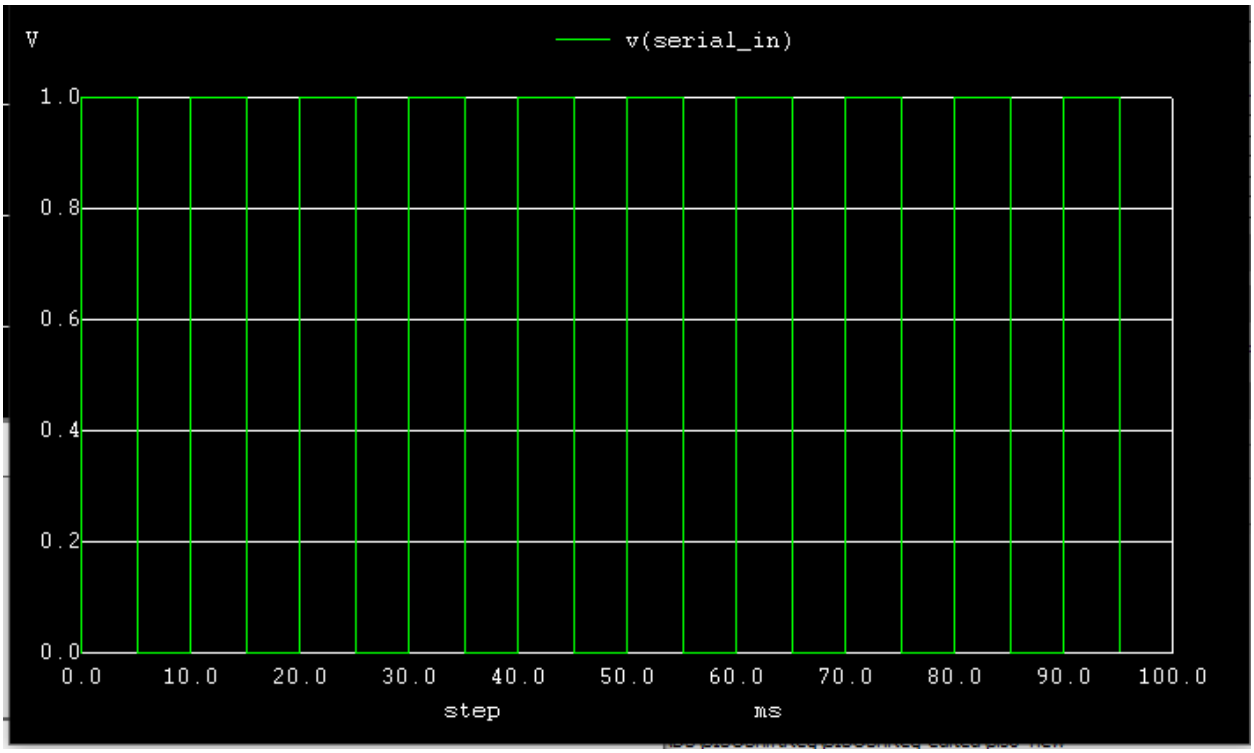
Synchronous up counter	
Component Name	**Type**
d_dff	d flip flop
clock	clock input
DC	dc voltage source for logic 1

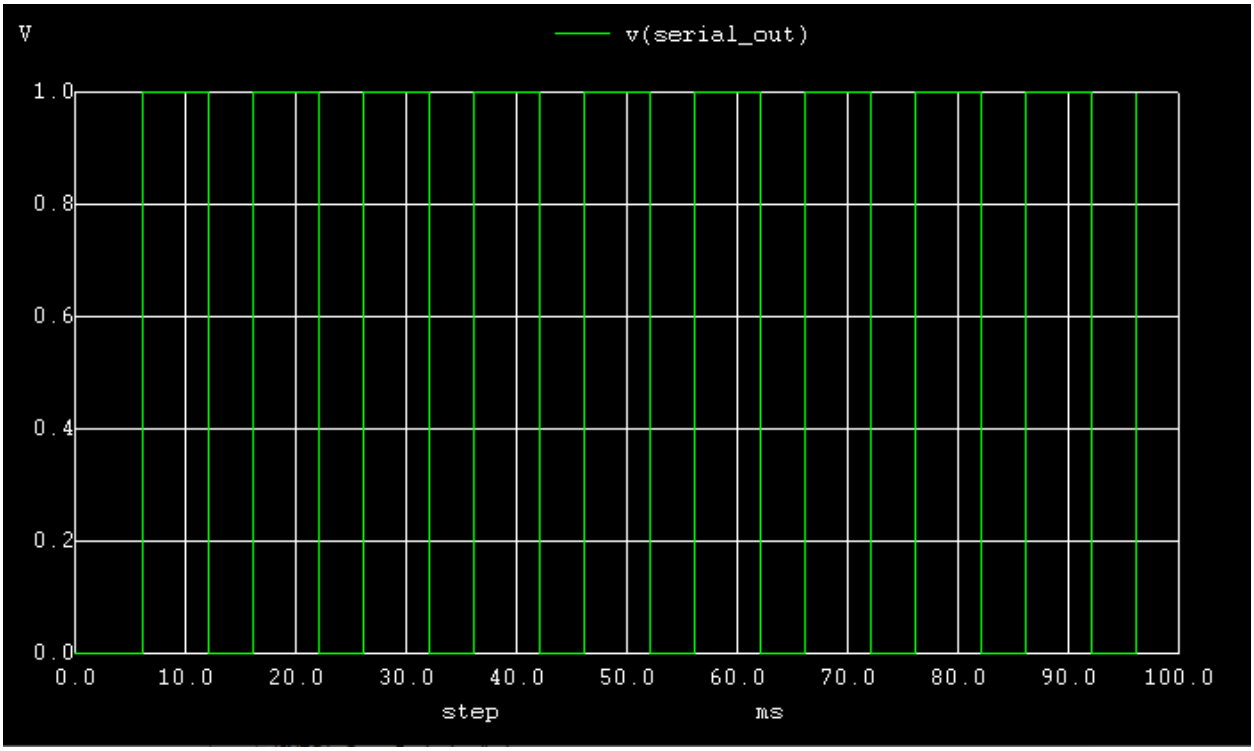
ESIM Circuit design snapshot:



OUTPUT –


V
v(clock)
1.0
0.8
0.6
0.4
0.2
0.0
0.0
20.0
40.0
60.0
80.0
100.0
step
ms


V
v(serial_in)
1.0
0.8
0.6
0.4
0.2
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
step
ms



References:

- https://www.electrical4u.com/serial-in-serial-out-siso-shift-register/
- https://www.geeksforgeeks.org/shift-registers-in-digital-logic/