Title of the experiment

CMOS NAND Gate Using 0.5um Technology

Theory:

NAND gate is one of the basic logic gates to perform the digital operation on the input signals. It is the combination of AND Gate followed by NOT gate i.e. it is the opposite operation of AND gate where the Logic NAND gate is complementary of AND gate. The logic output of NAND gate is low (FALSE) only when the inputs are high (TRUE).

CMOS NAND gate is one of the important and simple realizations. CMOS is the combination of PMOS and NMOS. The circuit shows the realization of CMOS NAND gate which consists of two PMOS and two NMOS gates. Here in this circuit when Va and Vb are high i.e. at 5V then the two PMOS will be open circuited and two NMOS will be Short circuited. The output Vout will be shorted to ground and produces zero output. If any of the input is low (0 V) corresponding PMOS will be shorted and NMOS will opened the Vout is shorted to Vdd which provides high output. The truth table shows all the possible operation of NAND gate using CMOS.

Schematic diagram:

The circuit schematic of the CMOS NAND Gate Using 0.5um in eSim is as shown below:

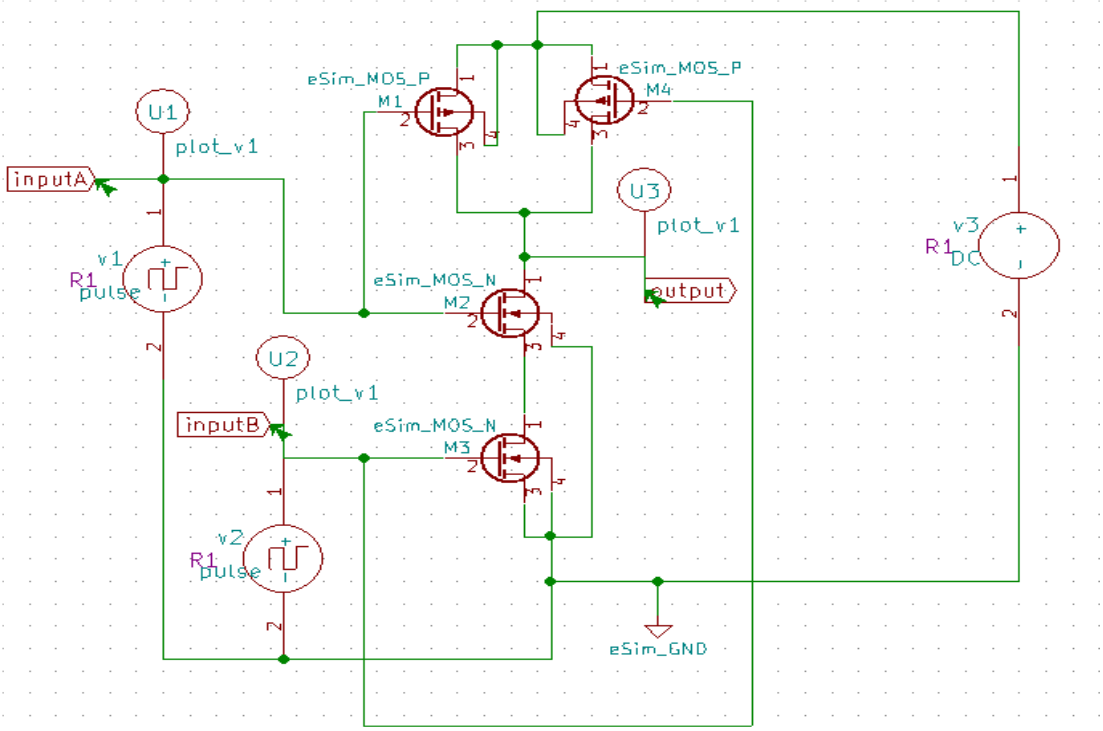

Figure 1: CMOS NAND Gate Using 0.5um Technology

Simulation Results:

1. Ngspice Plots-

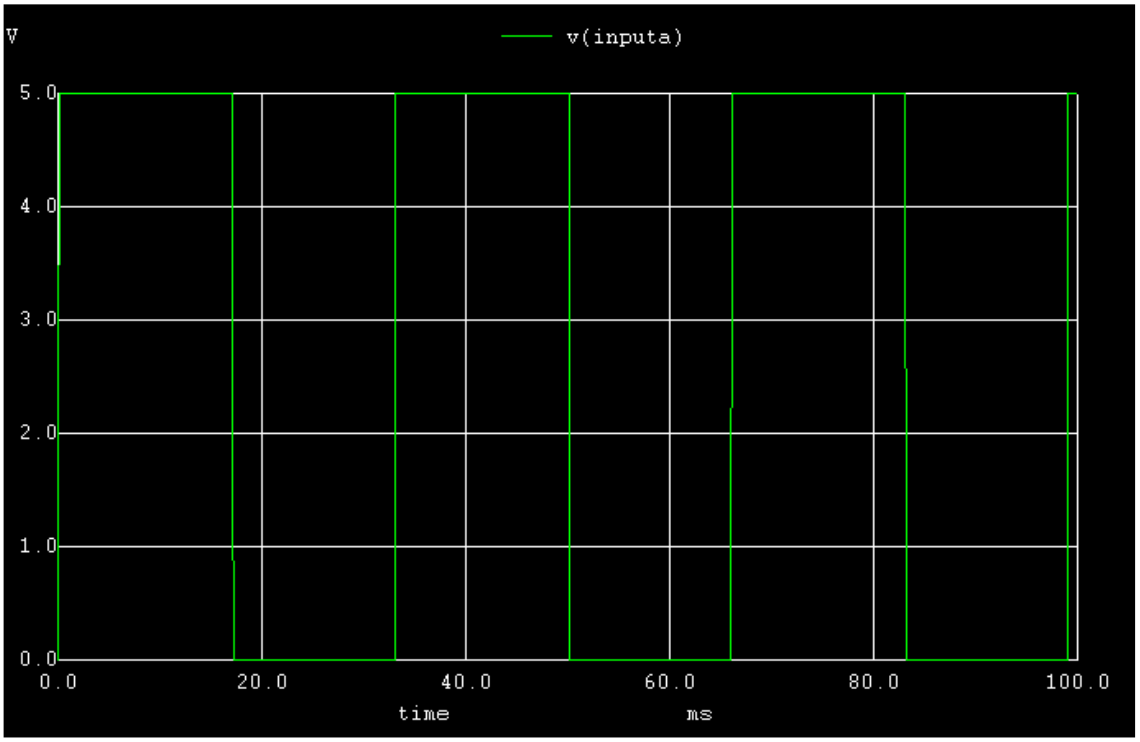

Figure 2: Ngspice Input A Plot

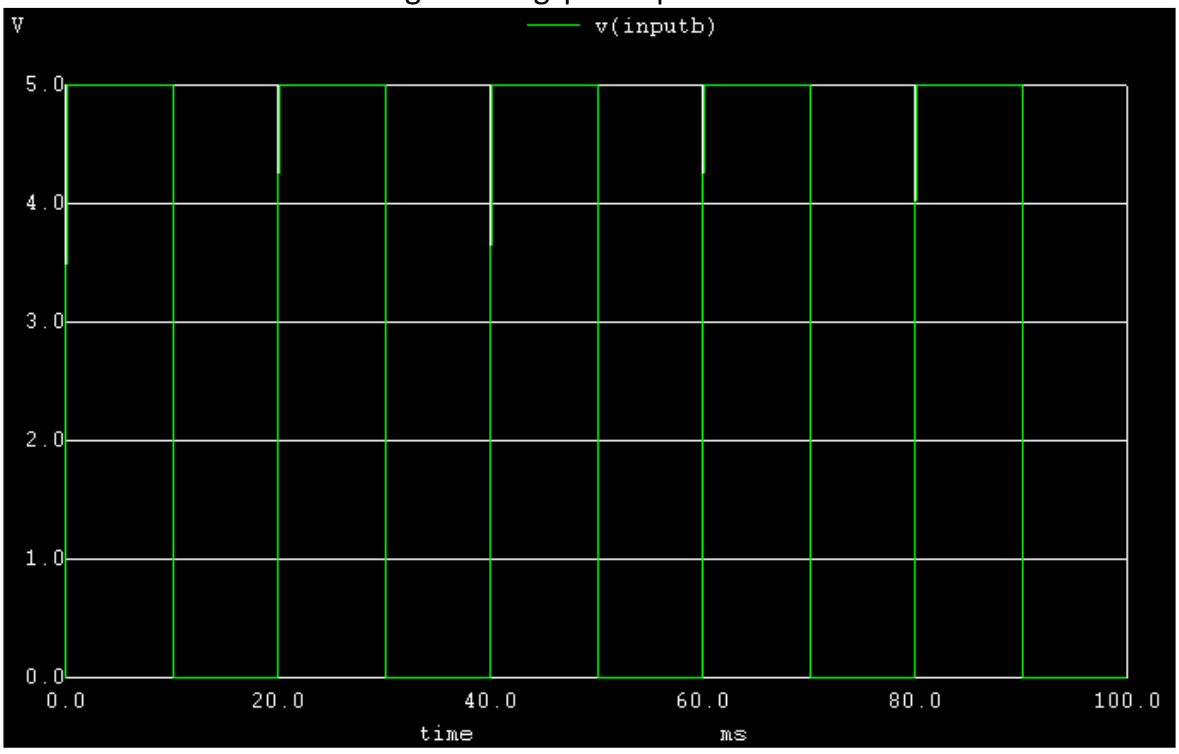

Figure 3: Ngspice Input B Plot

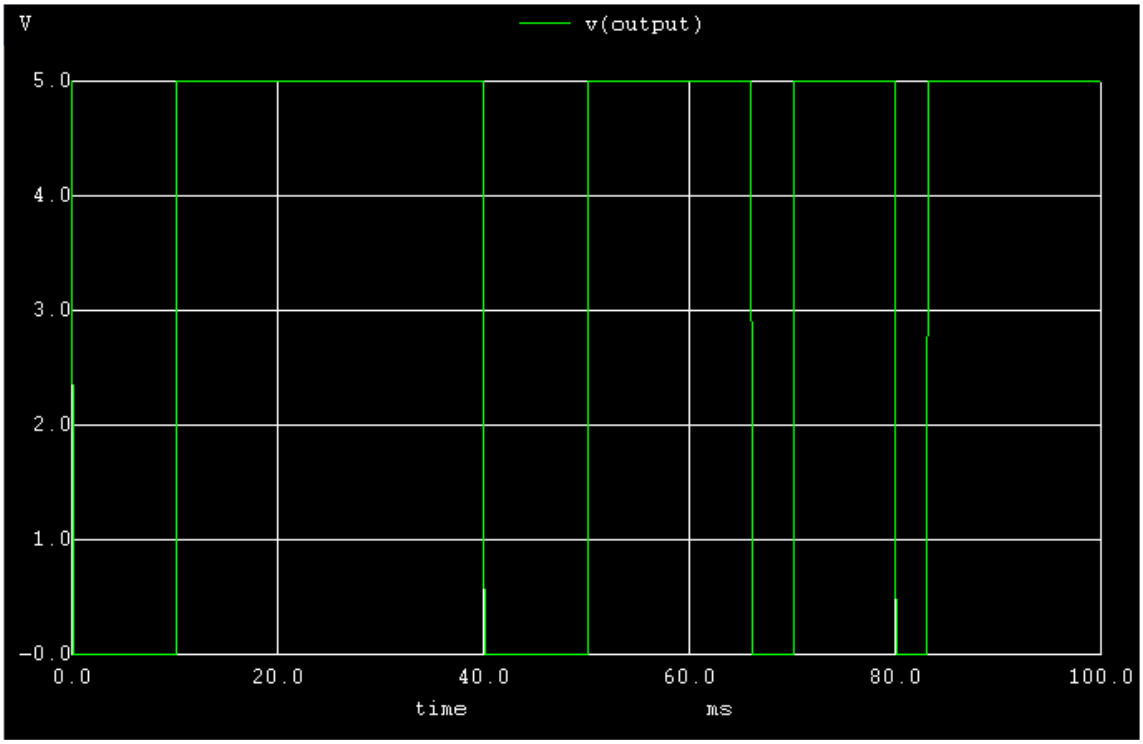

Figure 4: Ngspice Output Plot

Python Plots-

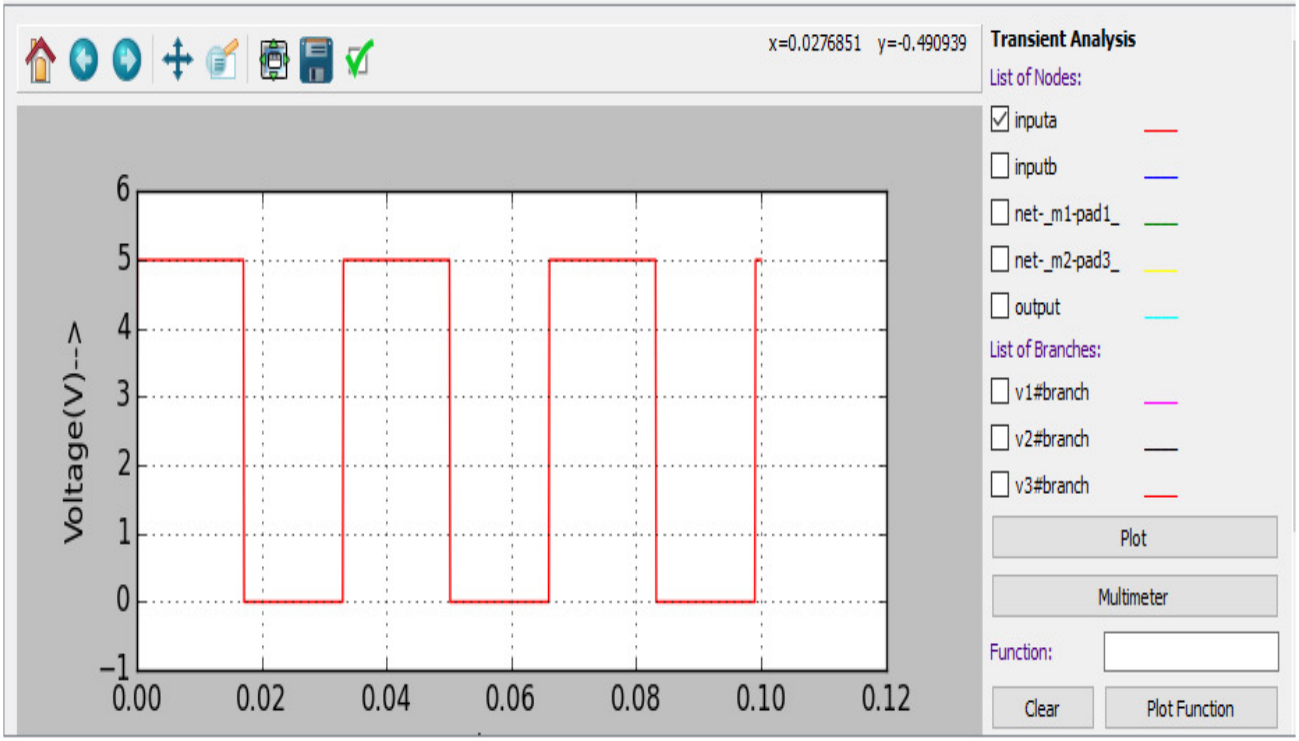

Figure 5: Python Input A Plot

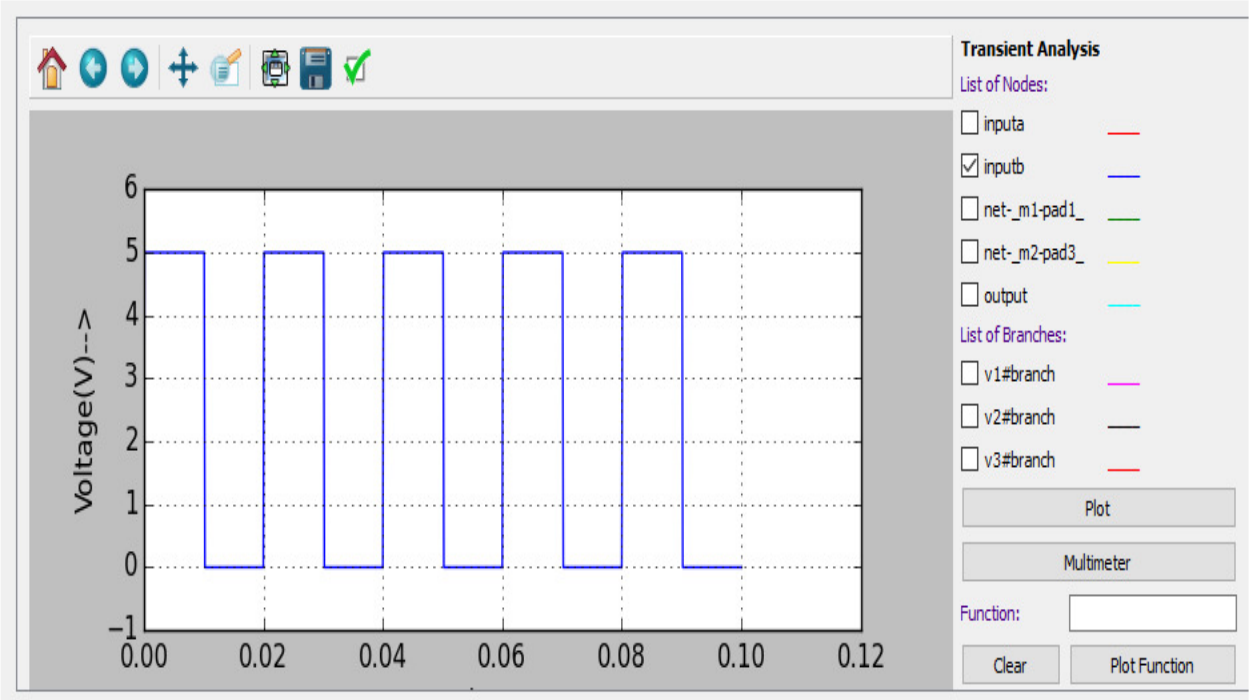

Figure 6: Python Input B Plot

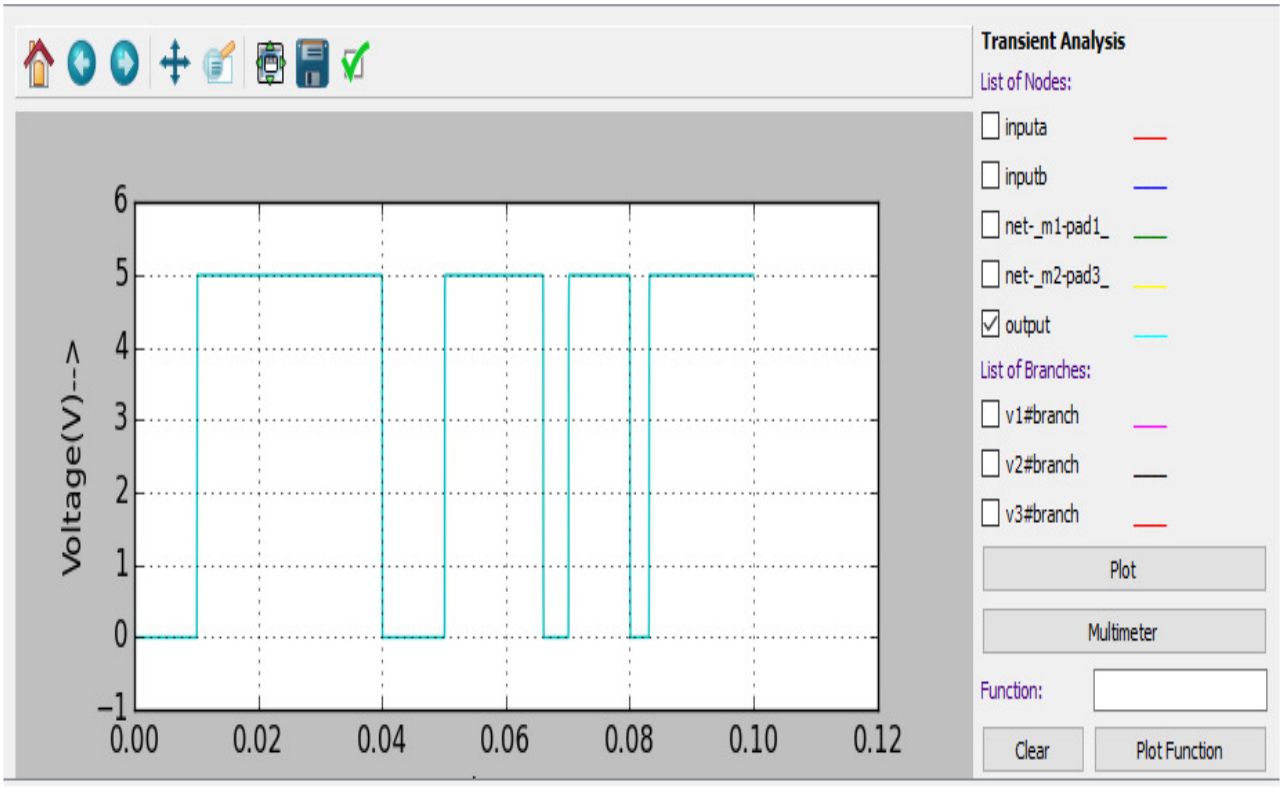

Figure 7: Python Output Plot

Conclusion:

Thus, we have studied the CMOS NAND Gate Using 0.5um Technology and the simulation plot of ngspice and python plot obtained in eSim.

References:

1) https://en.wikipedia.org/wiki/CMOS#cite_note-1
2) http://ecetutorials.com/digital-electronics/nand-gate-truth-table-relaisation-using-diode-transistor-cmos/
3) https://www.researchgate.net/figure/a-A-conventional-2-input-CMOS-NAND-gate-characterized-by-a-single-output-delay_fig14_304132213