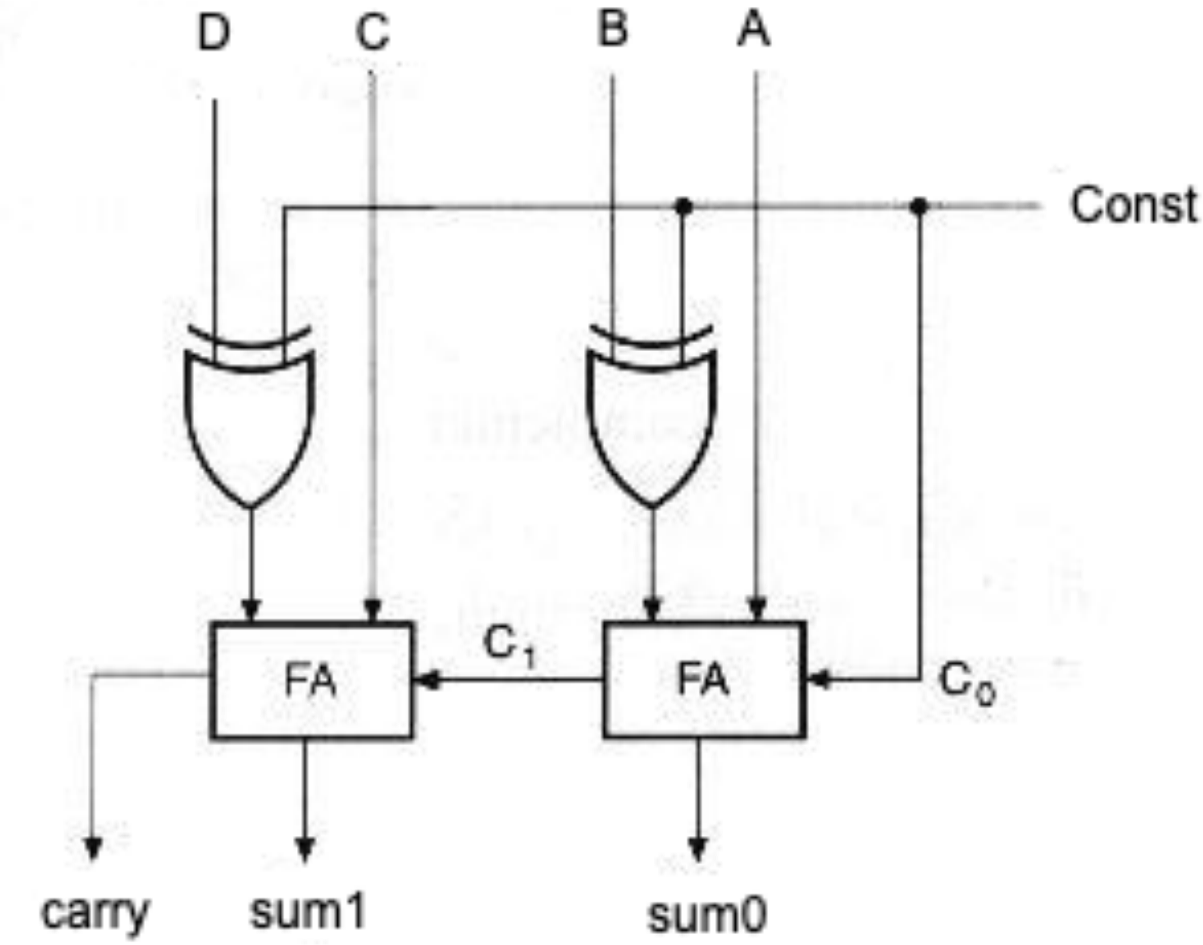
Title : A 2-Bit Binary Adder Subtractor Circuit

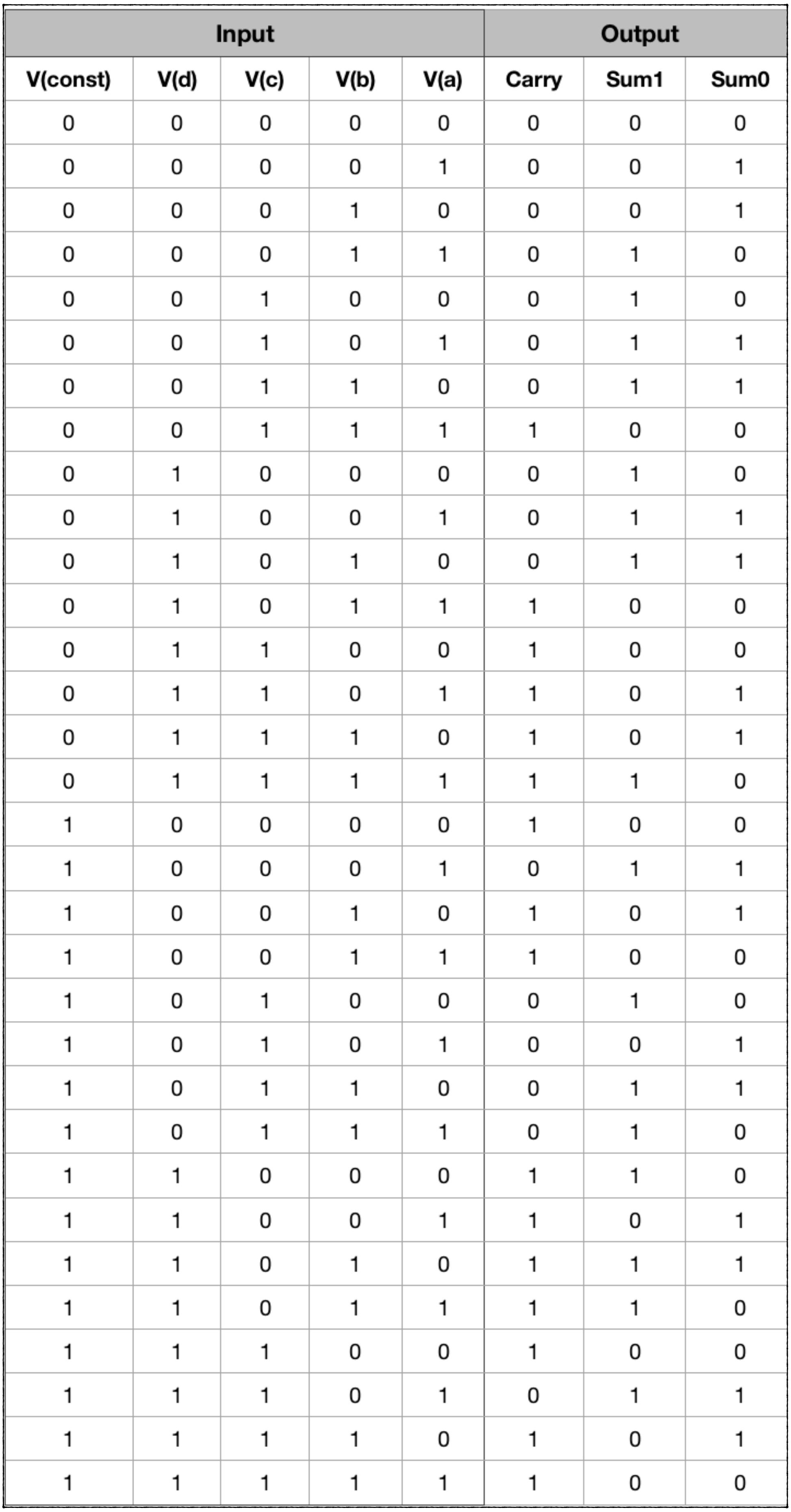
Theory

In Digital Circuits, A Binary Adder-Subtractor is one which is capable of both addition and subtraction of binary numbers in one circuit itself. The operation being performed depends upon the binary value the control signal holds. It is one of the components of the ALU (Arithmetic Logic Unit).

Circuit Diagram

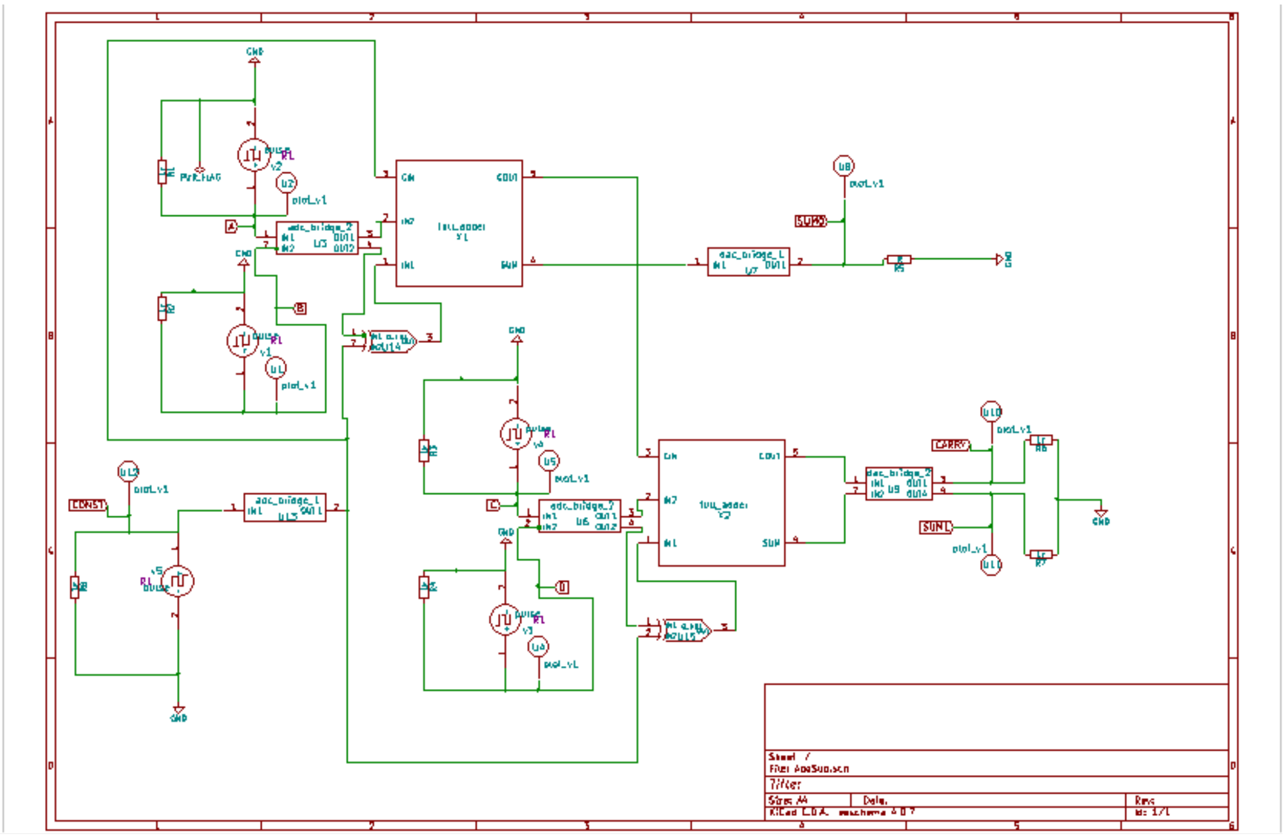


Truth Table

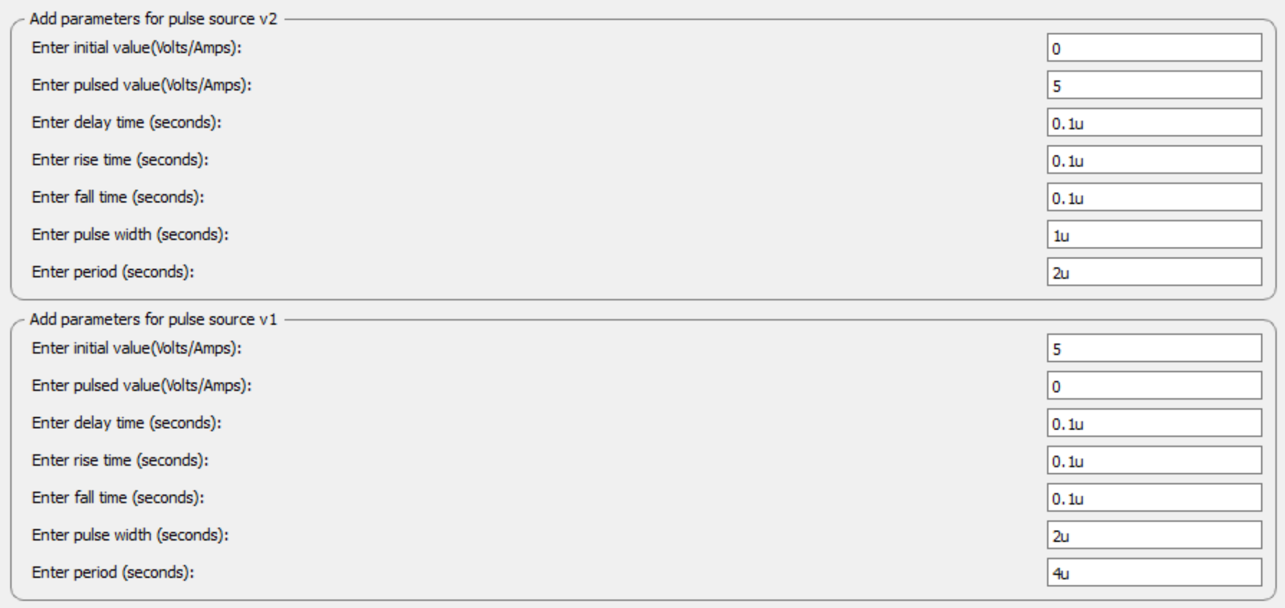


Input					Output		
V(const)	V(d)	V(c)	V(b)	V(a)	Carry	Sum1	Sum0
0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	1
0	0	0	1	0	0	0	1
0	0	0	1	1	0	1	0
0	0	1	0	0	0	1	0
0	0	1	0	1	0	1	1
0	0	1	1	0	0	1	1
0	0	1	1	1	1	0	0
0	1	0	0	0	0	1	0
0	1	0	0	1	0	1	1
0	1	0	1	0	0	1	1
0	1	0	1	1	1	0	0
0	1	1	0	0	1	0	0
0	1	1	0	1	1	0	1
0	1	1	1	0	1	0	1
0	1	1	1	1	1	1	0
1	0	0	0	0	1	0	0
1	0	0	0	1	0	1	1
1	0	0	1	0	1	0	1
1	0	0	1	1	1	0	0
1	0	1	0	0	0	1	0
1	0	1	0	1	0	0	1
1	0	1	1	0	0	1	1
1	0	1	1	1	0	1	0
1	1	0	0	0	1	1	0
1	1	0	0	1	1	0	1
1	1	0	1	0	1	1	1
1	1	0	1	1	1	1	0
1	1	1	0	0	1	0	0
1	1	1	0	1	0	1	1
1	1	1	1	0	1	0	1
1	1	1	1	1	1	0	0

Schematic Diagram



Kicad to NgSpice



Add parameters for pulse source v2

Enter initial value(Volts/Amps): 0

Enter pulsed value(Volts/Amps): 5

Enter delay time (seconds): 0.1u

Enter rise time (seconds): 0.1u

Enter fall time (seconds): 0.1u

Enter pulse width (seconds): 1u

Enter period (seconds): 2u

Add parameters for pulse source v1

Enter initial value(Volts/Amps): 5

Enter pulsed value(Volts/Amps): 0

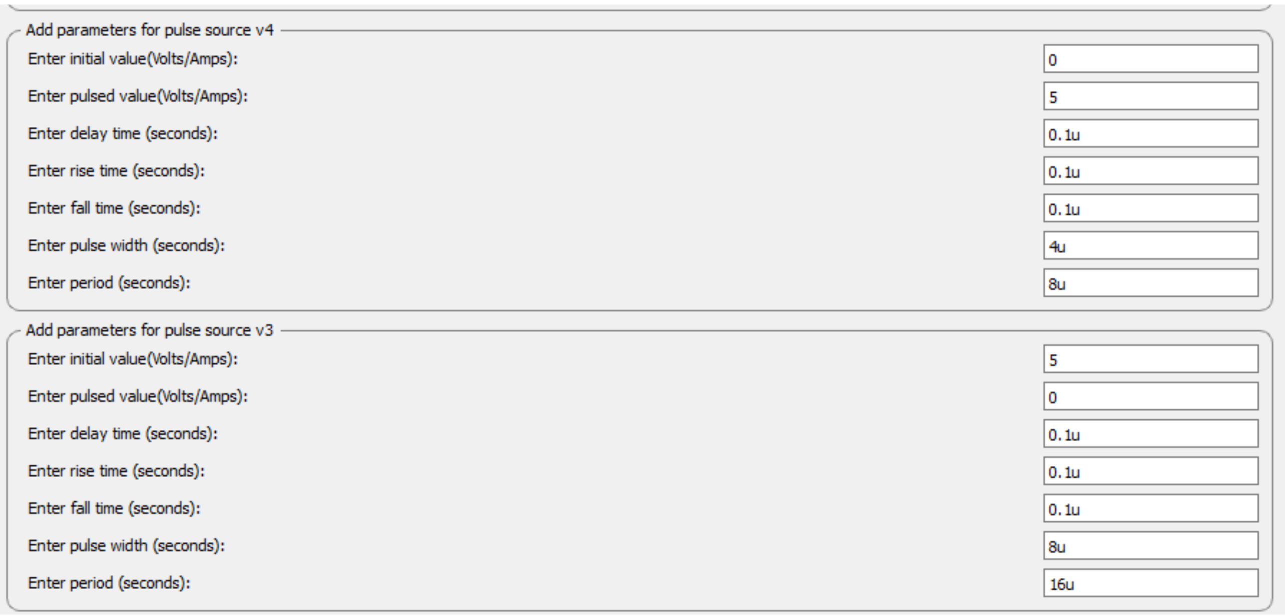
Enter delay time (seconds): 0.1u

Enter rise time (seconds): 0.1u

Enter fall time (seconds): 0.1u

Enter pulse width (seconds): 2u

Enter period (seconds): 4u



Add parameters for pulse source v4

Enter initial value(Volts/Amps): 0

Enter pulsed value(Volts/Amps): 5

Enter delay time (seconds): 0.1u

Enter rise time (seconds): 0.1u

Enter fall time (seconds): 0.1u

Enter pulse width (seconds): 4u

Enter period (seconds): 8u

Add parameters for pulse source v3

Enter initial value(Volts/Amps): 5

Enter pulsed value(Volts/Amps): 0

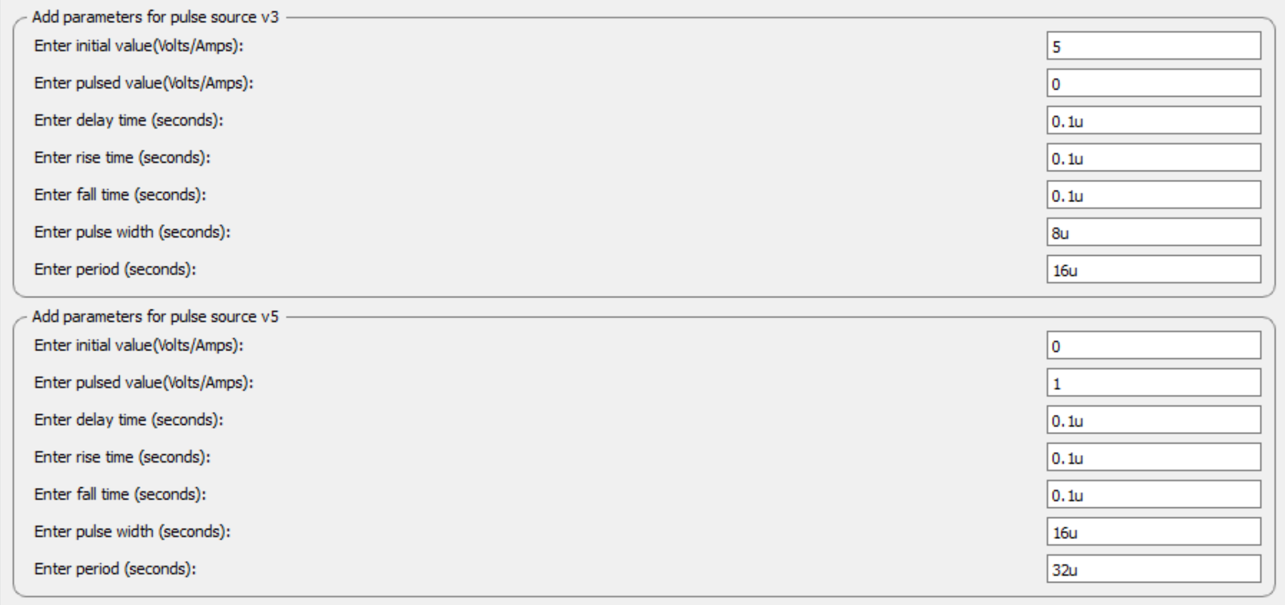
Enter delay time (seconds): 0.1u

Enter rise time (seconds): 0.1u

Enter fall time (seconds): 0.1u

Enter pulse width (seconds): 8u

Enter period (seconds): 16u



Add parameters for pulse source v3

Enter initial value(Volts/Amps): 5

Enter pulsed value(Volts/Amps): 0

Enter delay time (seconds): 0.1u

Enter rise time (seconds): 0.1u

Enter fall time (seconds): 0.1u

Enter pulse width (seconds): 8u

Enter period (seconds): 16u

Add parameters for pulse source v5

Enter initial value(Volts/Amps): 0

Enter pulsed value(Volts/Amps): 1

Enter delay time (seconds): 0.1u

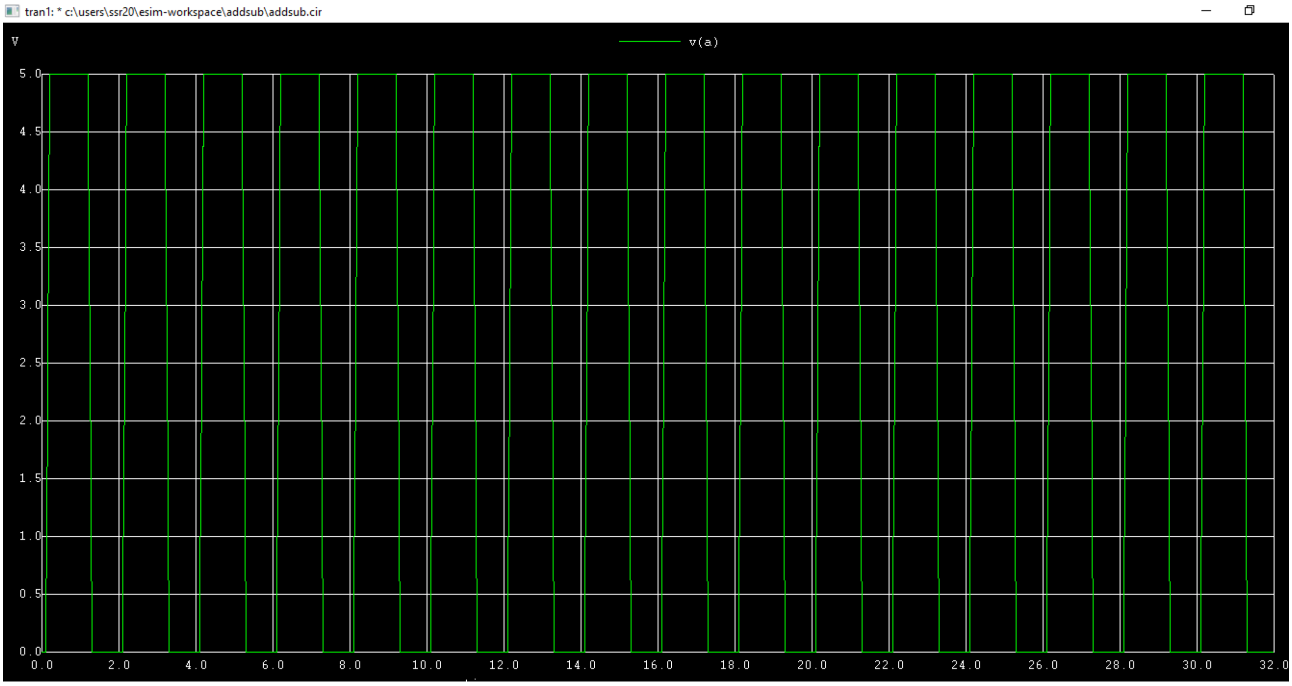
Enter rise time (seconds): 0.1u

Enter fall time (seconds): 0.1u

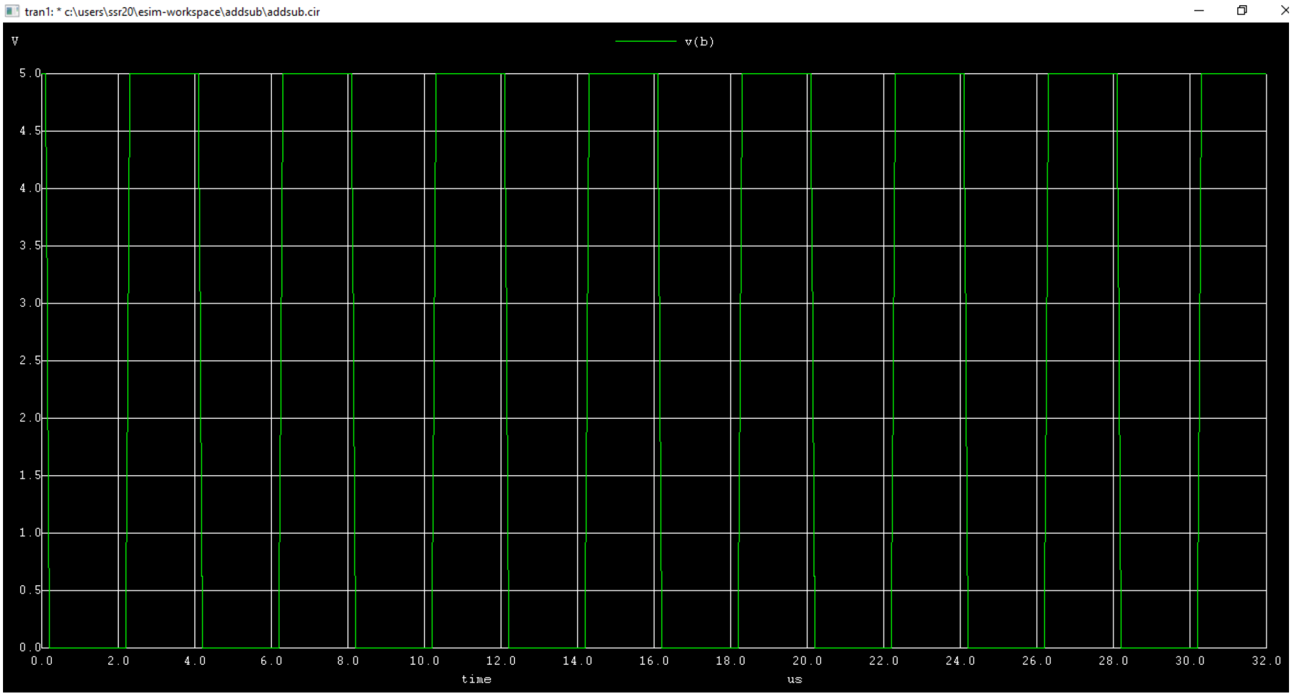
Enter pulse width (seconds): 16u

Enter period (seconds): 32u

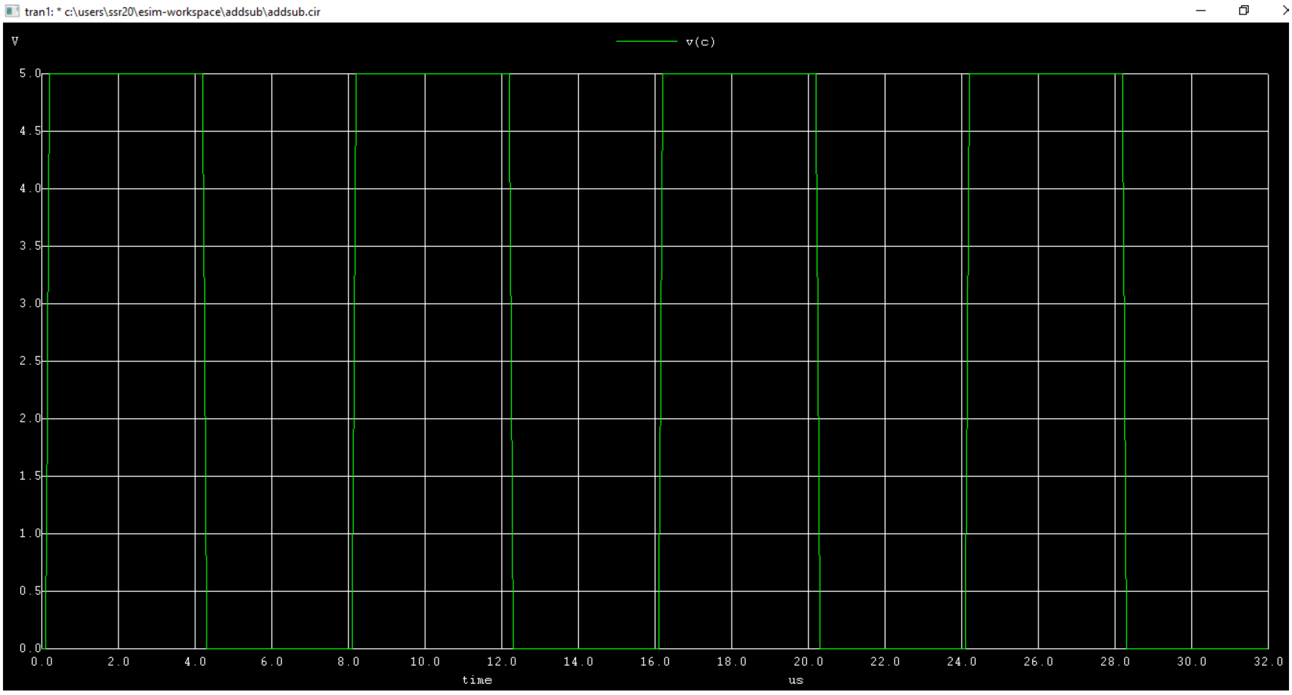
Input


tran1: * c:\users\ssr20\esim-workspace\addsub\addsub.cir
V
v(a)
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0.0
2.0
4.0
6.0
8.0
10.0
12.0
14.0
16.0
18.0
20.0
22.0
24.0
26.0
28.0
30.0
32.0

V(A)

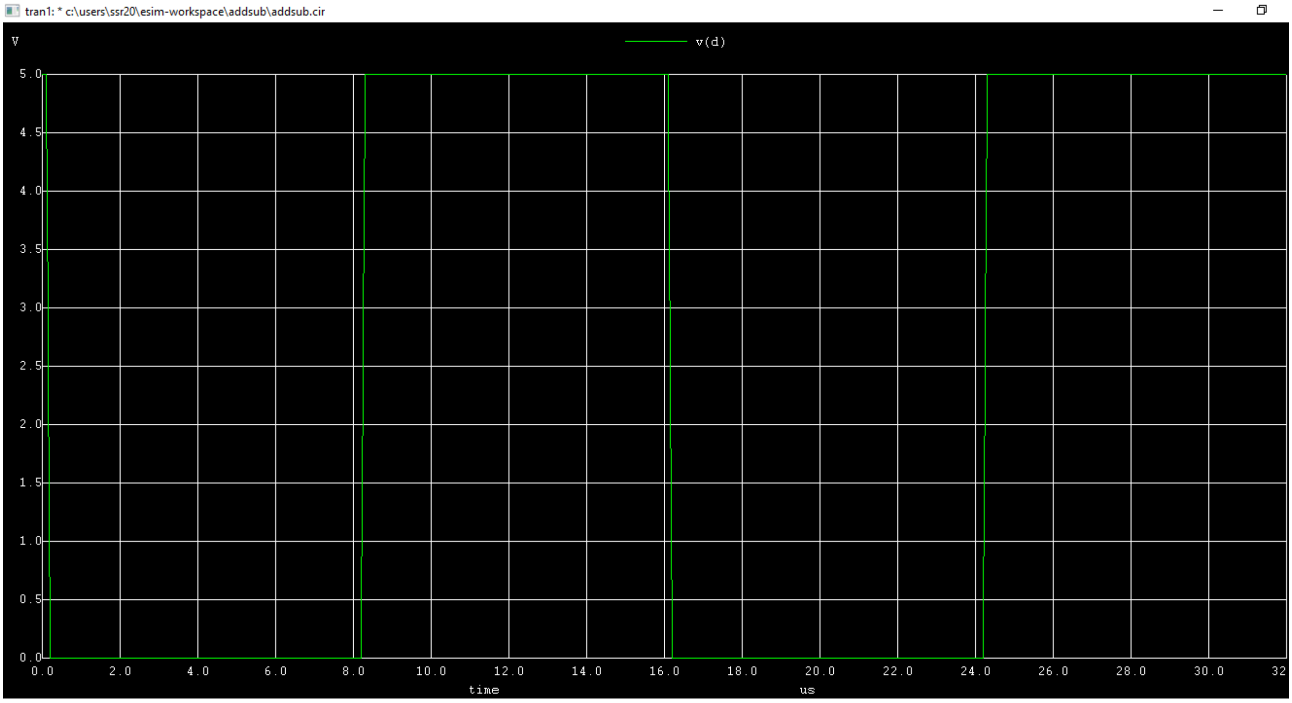

tran1: * c:\users\ssr20\esim-workspace\addsub\addsub.cir
V
v(b)
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0.0
2.0
4.0
6.0
8.0
10.0
12.0
14.0
16.0
18.0
20.0
22.0
24.0
26.0
28.0
30.0
32.0
time
us

V(B)



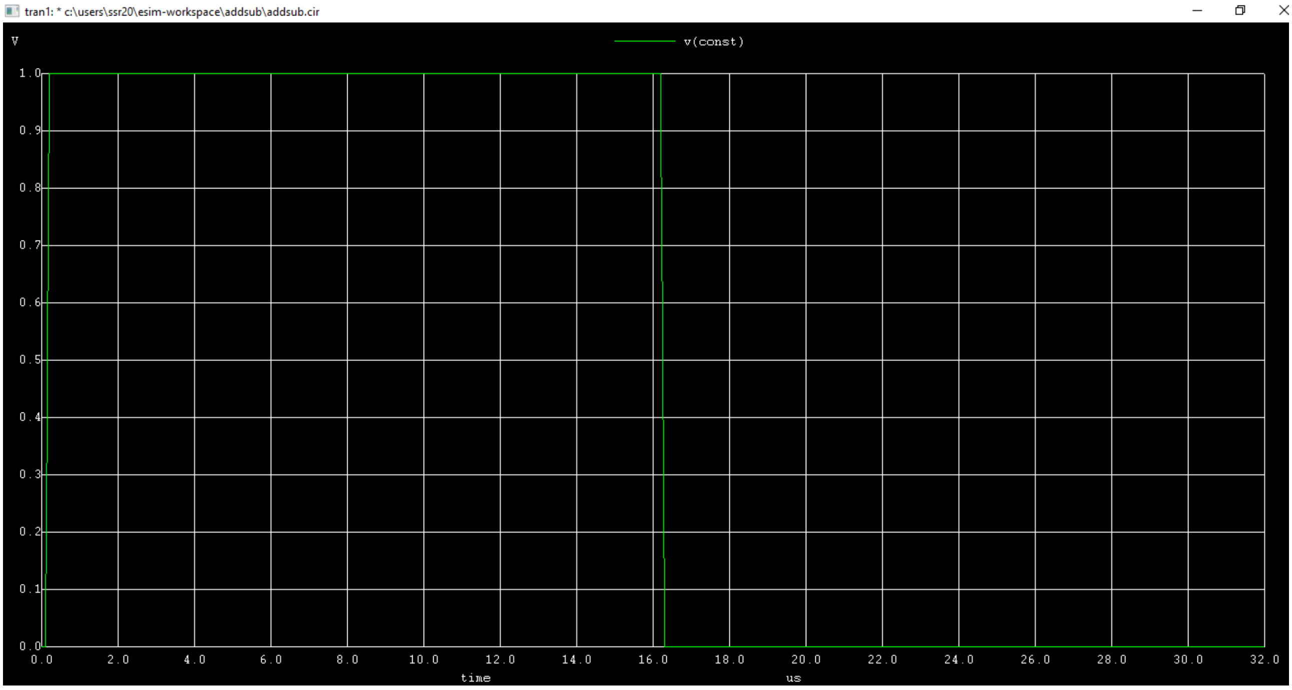
tran1: * c:\users\ssr20\esim-workspace\addsub\addsub.cir

V(C)



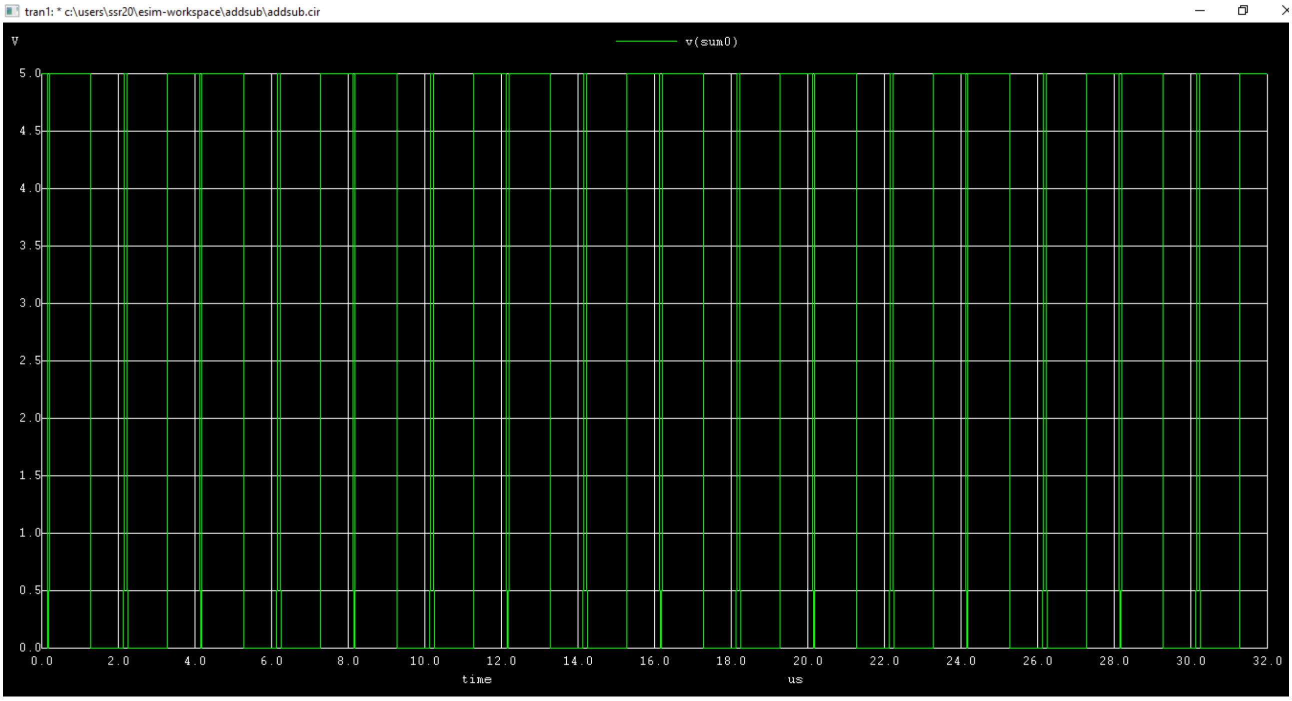
tran1: * c:\users\ssr20\esim-workspace\addsub\addsub.cir

V(D)

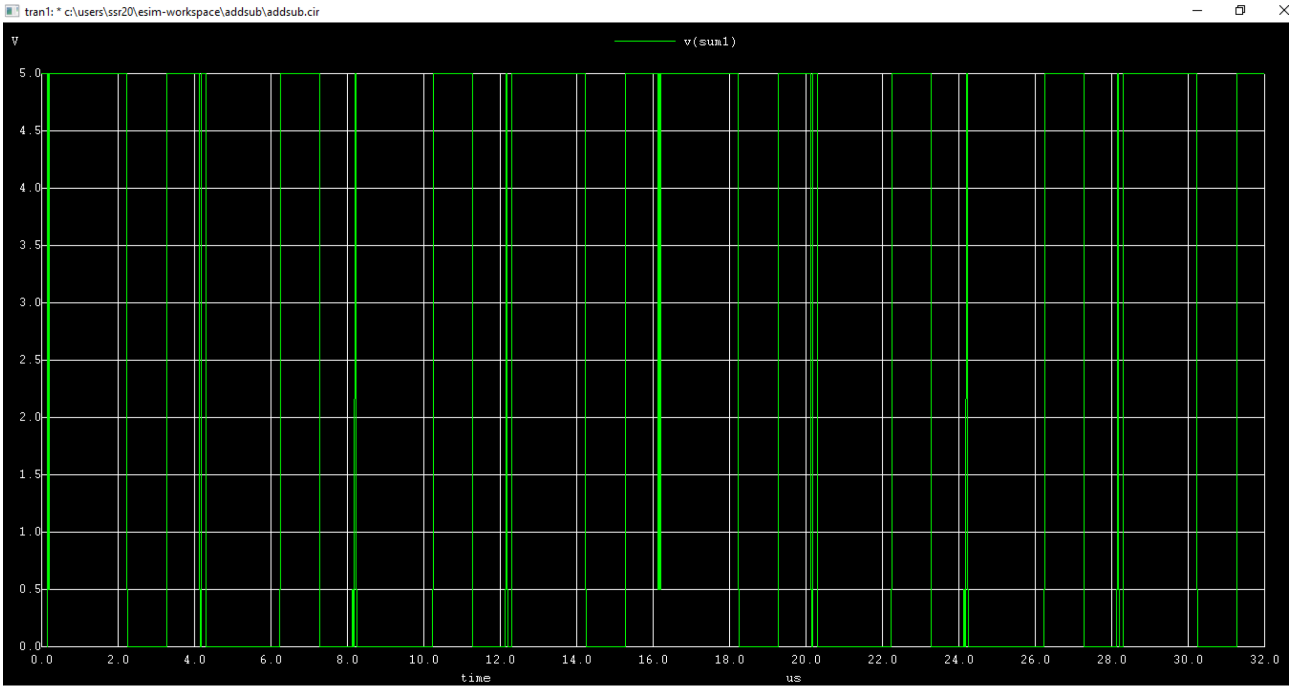


V(const)

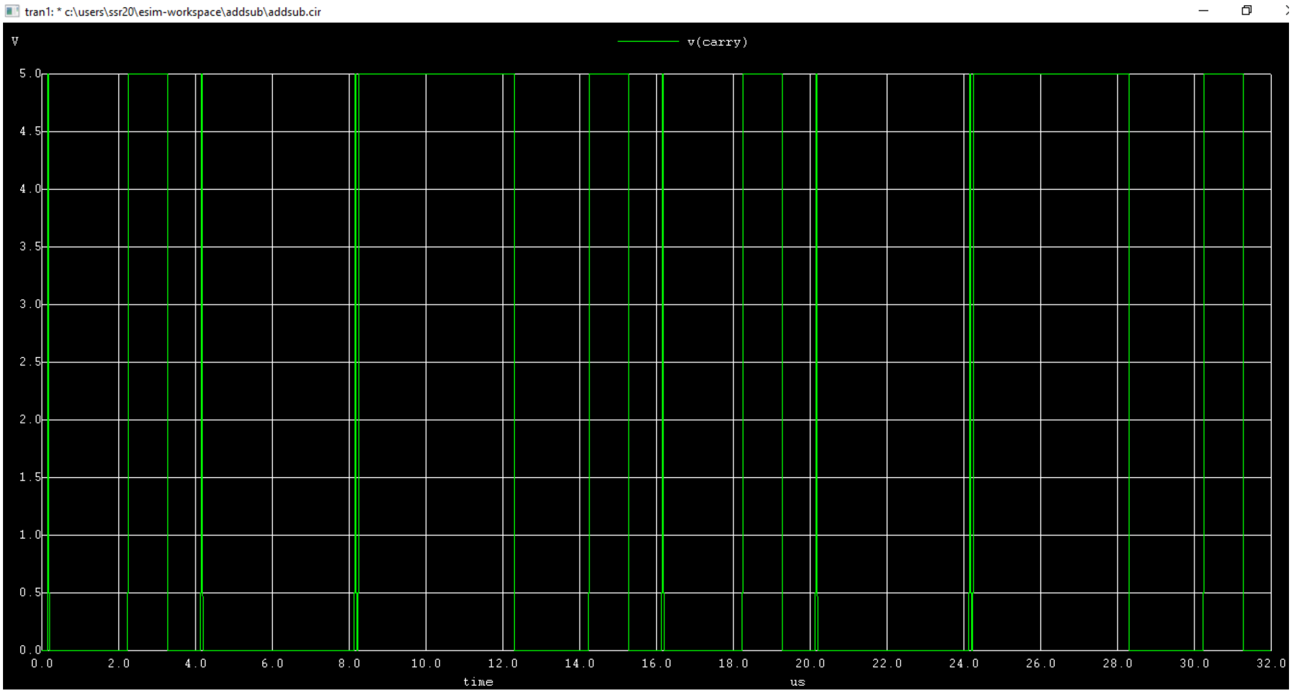
Output



V(Sum0)



V(Sum1)



V(carry)

Conclusion

Thus we have studied how an adder subtractor circuit works and implemented a 2-bit binary adder subtractor circuit using eSim.

References

https://www.geeksforgeeks.org/4-bit-binary-adder-subtractor/