Title of the experiment:

Implementation of Odd Stage Ring Oscillator Using 0.5um CMOS Process

Theory:

The **ring oscillator** is composed of connecting a series of inverters, or logical NOT gates, in a back-to-back fashion. Each of the inverter receives its input from the output of the previous inverter and the output of the last inverter is fed back as input to the first stage, thus giving the name, ring oscillator.

The output of such an arrangement oscillates between two voltage levels, hence this belongs to family of astable circuits. In order to understand the operation of ring oscillator, we must have knowledge on Gate delay. Gate delay, also known as propagation delay, is the time difference of change of output when a change in input was observed. Thus, in our context, this delay is caused by the charging and discharging of the gate capacitance that must be charged before current can flow between the source and the drain. Thus, the frequency of oscillation can be controlled by the increasing or decreasing this gate delay.

Consider each of the stage (inverter) to have a negative gain slightly greater than 1. Initially, let's assume there is no input at the first stage. Due to its inverting properties, the output of the first stage is changed in reverse direction by amount greater than the input voltage, for a gain greater than 1. This happens in each of the subsequent stages. This amplified and reversed signal propagates from the output through the time-delay and back to the input where it is amplified and inverted again. This results in generation of a sine wave, whose time period is equal to the total delay of each stage.

If *t* is the propagation delay of each stage, *n* represents the number of inverters in the oscillator chain, the frequency of oscillation is given by:

$$f = \frac{1}{2tn}$$

Ring oscillators find applications in Voltage controlled oscillators, where the conventional inverter is replaced by a current-starved inverter, also in random number generators. The inverter feedback can be used as a storage element and it is the basic building block of static random access memory or SRAM.

Schematic Diagram:

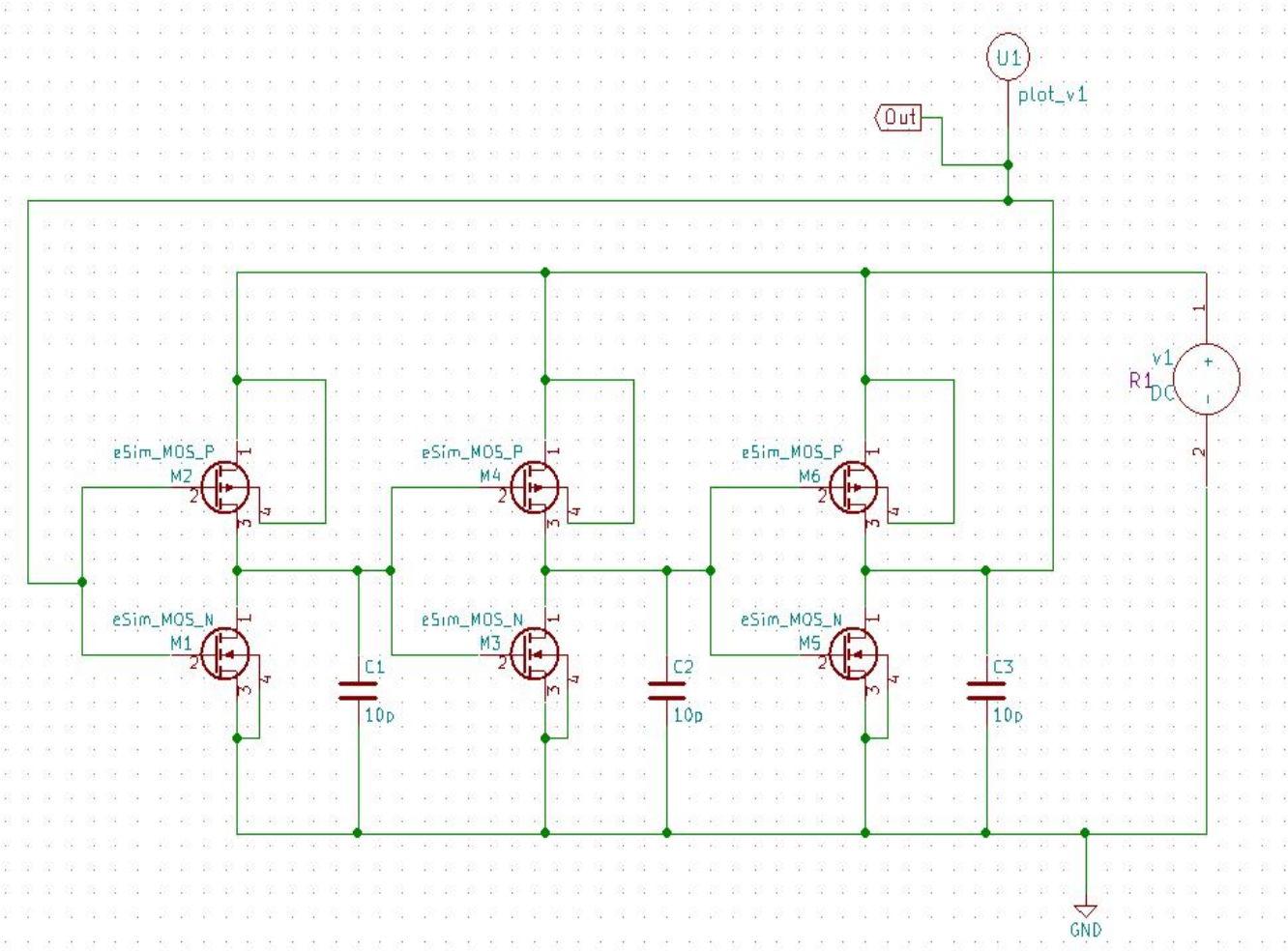

Fig.1 Ring Oscillator

Simulation Results:

1. Ngspice Plot:

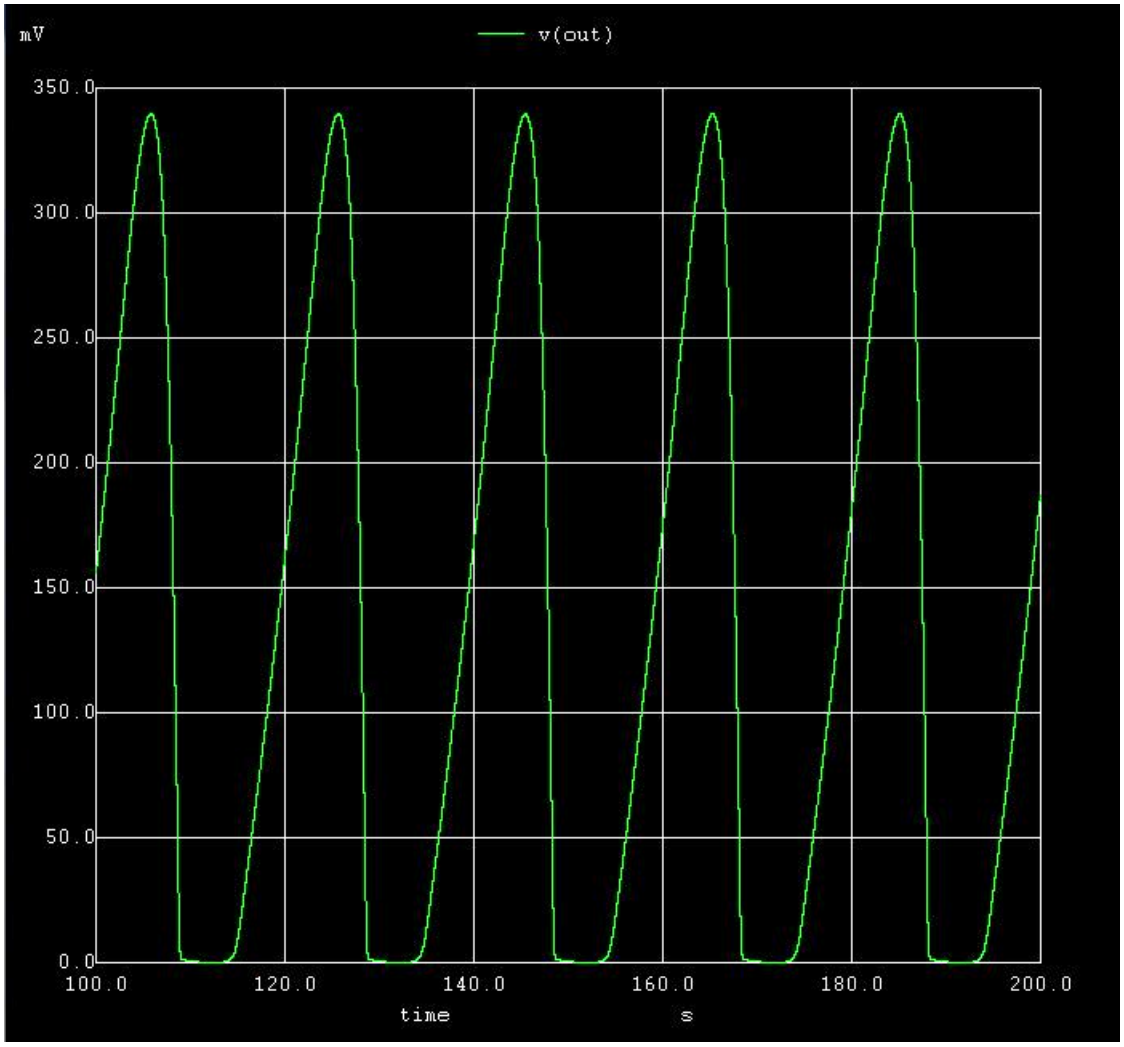

Fig 2. Output Waveform

2. Python Plot:

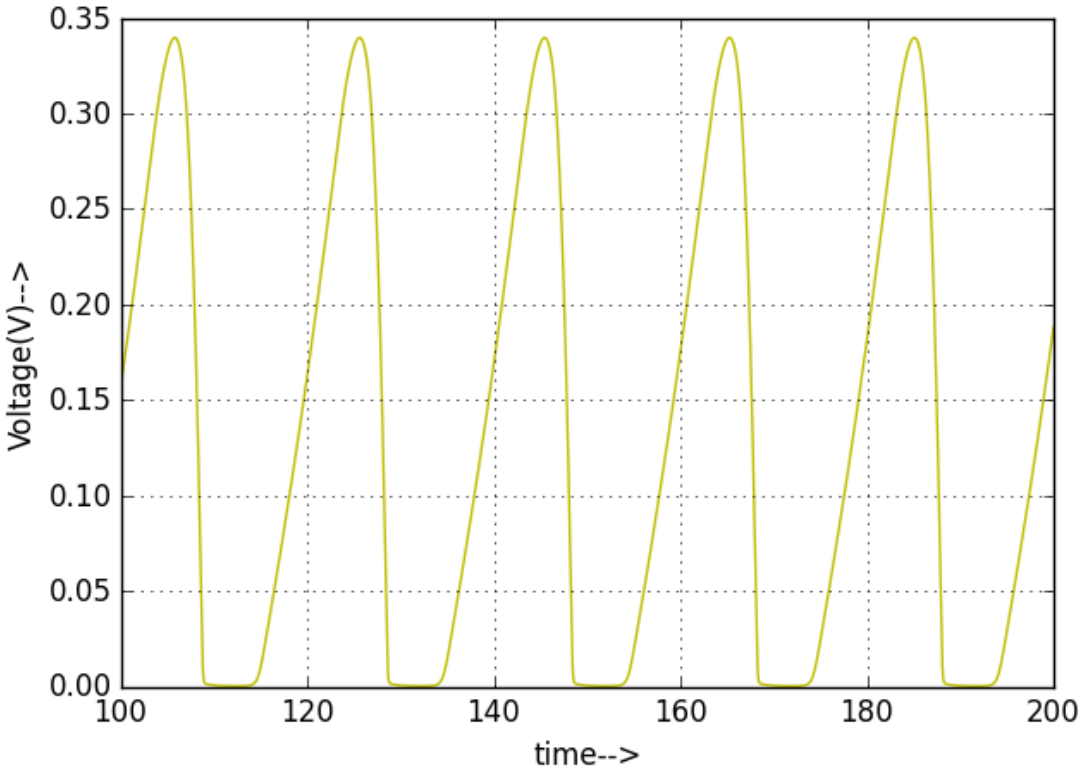

Fig 3. Output Waveform

Conclusion:

Thus we have studied the operation of Ring Oscillator implemented using odd stage of CMOS inverters.

References:

1. Jan M. Rabaey ,Anantha Chandrakasan, Borivoje Nikolic,

Digital Integrated Circuits: A Design perspective, Second Edition , Pearson , 2016.

2. https://en.wikipedia.org/wiki/Ring_oscillator