TITLE OF THE EXPERIMENT

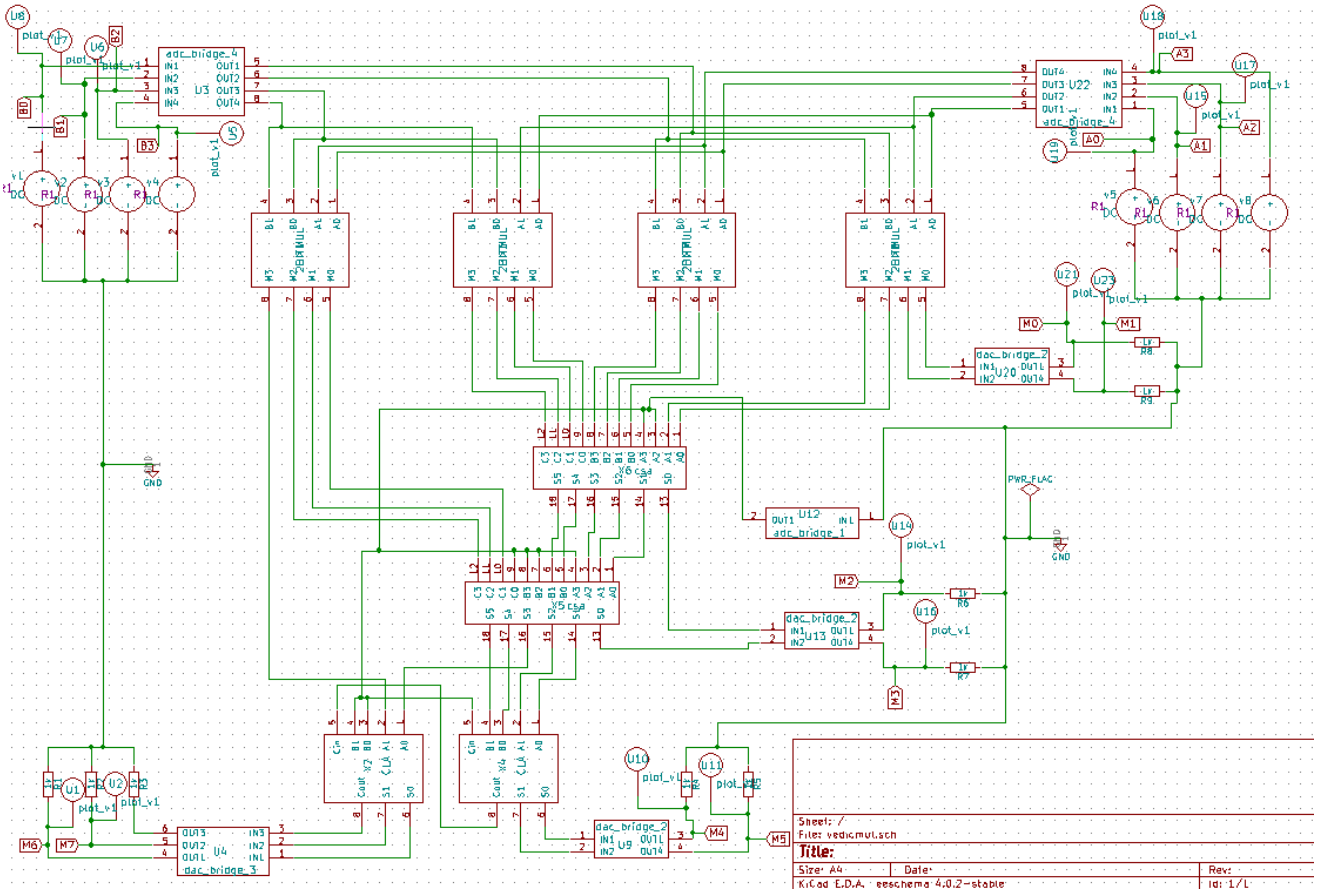
DESIGN OF FOUR BIT VEDIC MULTIPLIER USING ESIM

THEORY

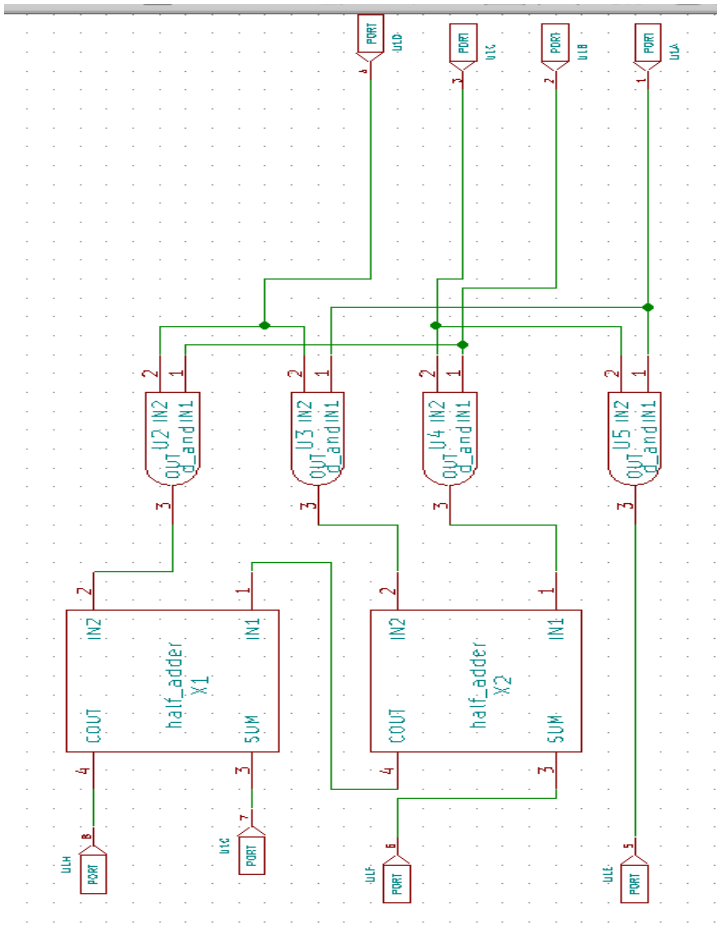
The performance of the multiplier determines the system performance, because the multiplier is slowest element in the system. Multiplication is one of the major operation in arithmetic and logical operations and multiplier is used in many applications like FFT, DFT, Image enhancement, DWT etc,. The multiplication speed influences the processor speed, so the speed of the multiplication should be high. There is one such promising solution i.e., Vedic multiplier. Vedic multiplier is designed using Vedic mathematics. Vedic mathematics is an ancient system of mathematics, which is formulated by Sri Jagadguru Bharathi Krishna Tirthaji (1884-1960). The word Vedic is obtained from the word —Veda‖ which gives the meaning of power house of knowledge and devine.

Schematic Diagram

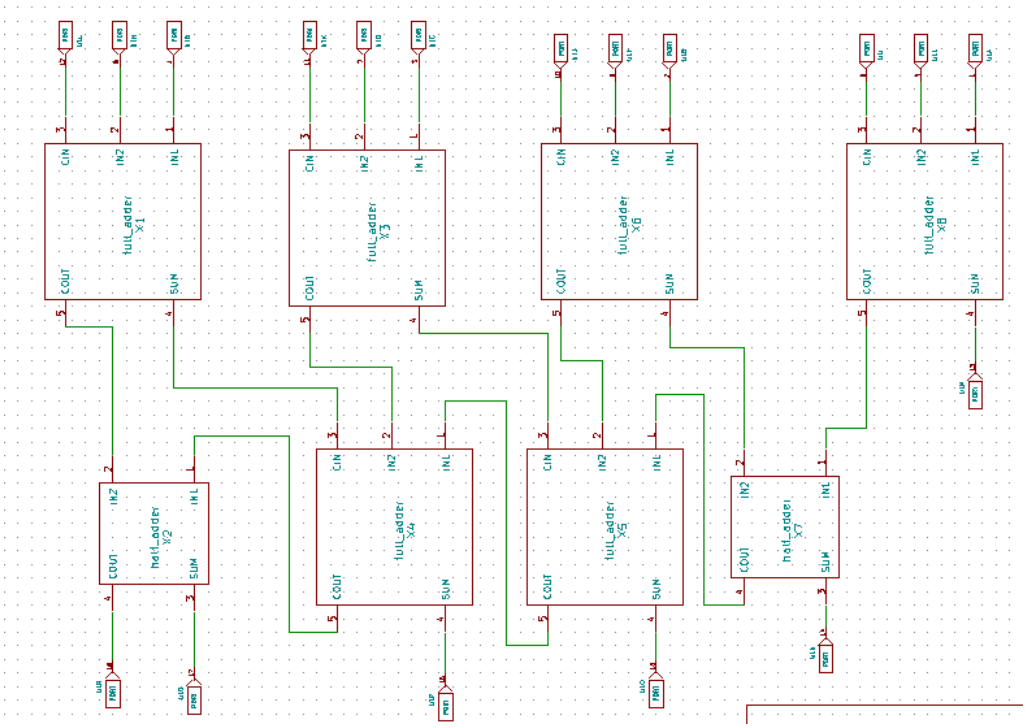
The schematic diagram of four bit vedic multiplier is shown below.It is done using subcircuits of 2X2 Multipliers,Carry save adder,Ripple carry adder.



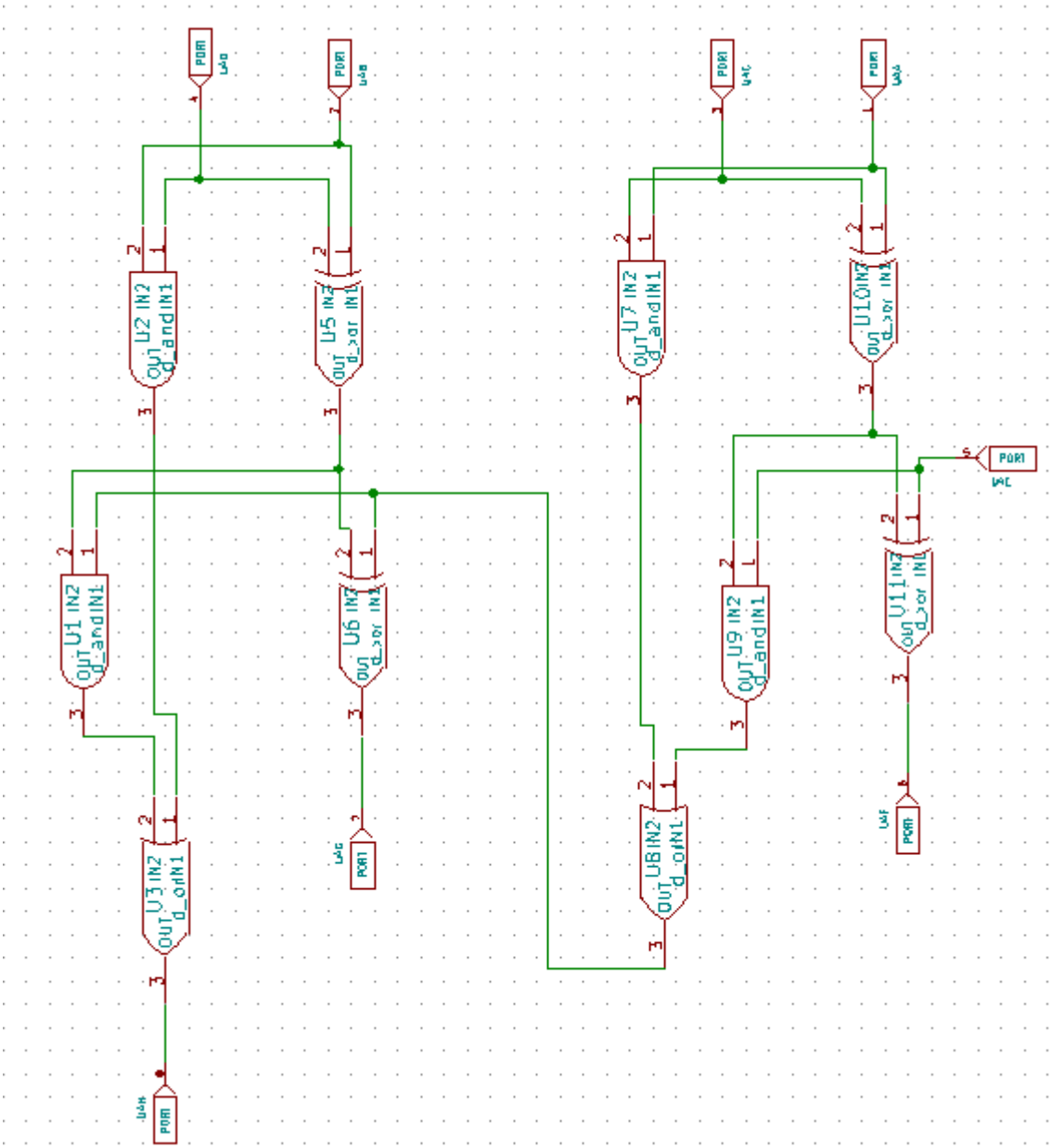
Subcircuit of 2X2 Multiplier



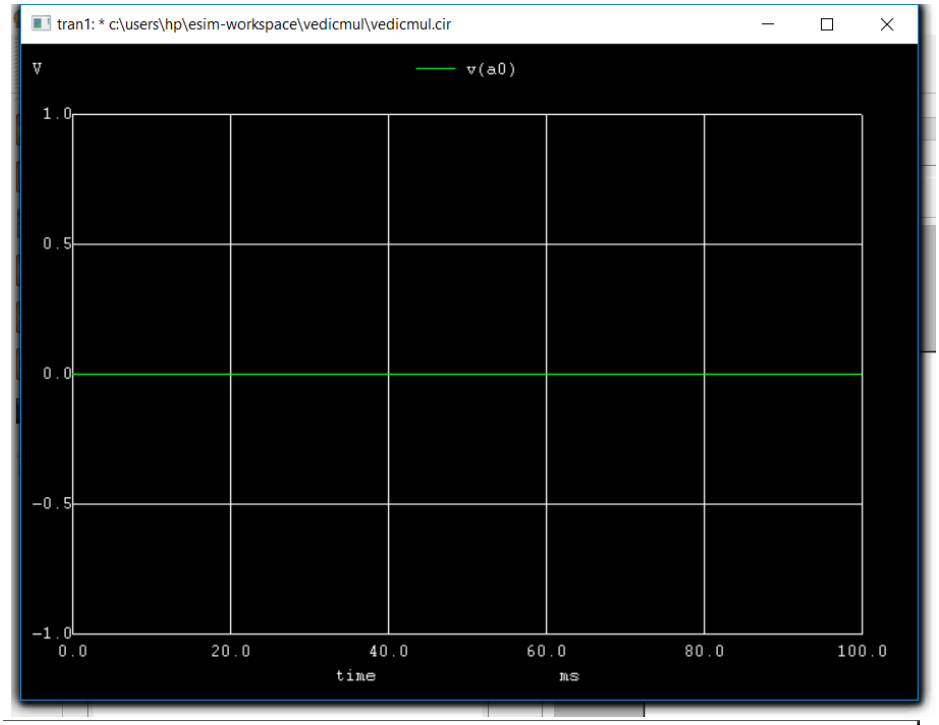
Subcircuit of Carry Save Adder

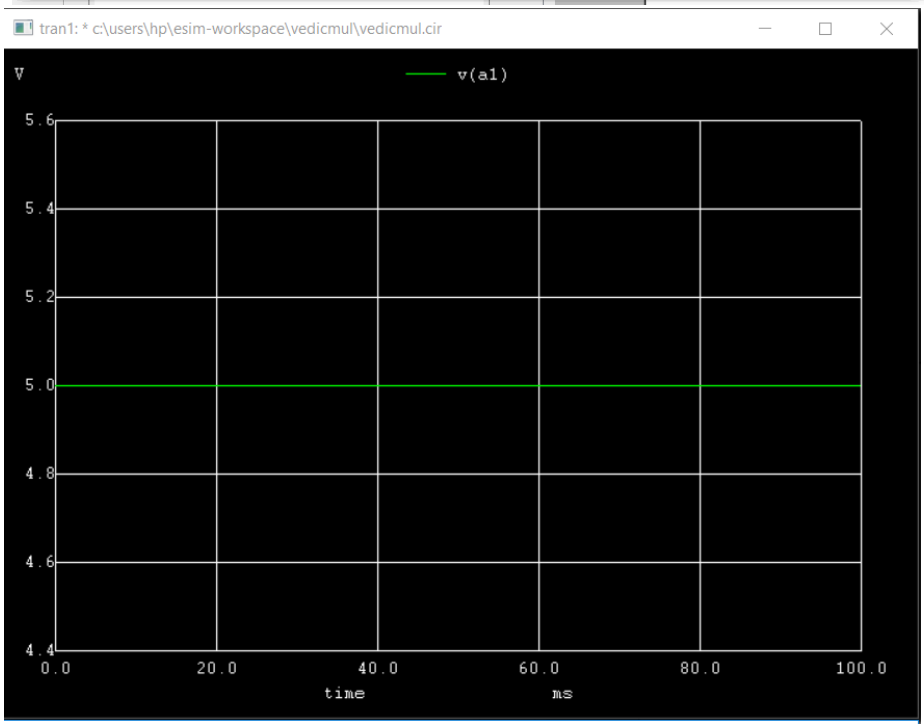


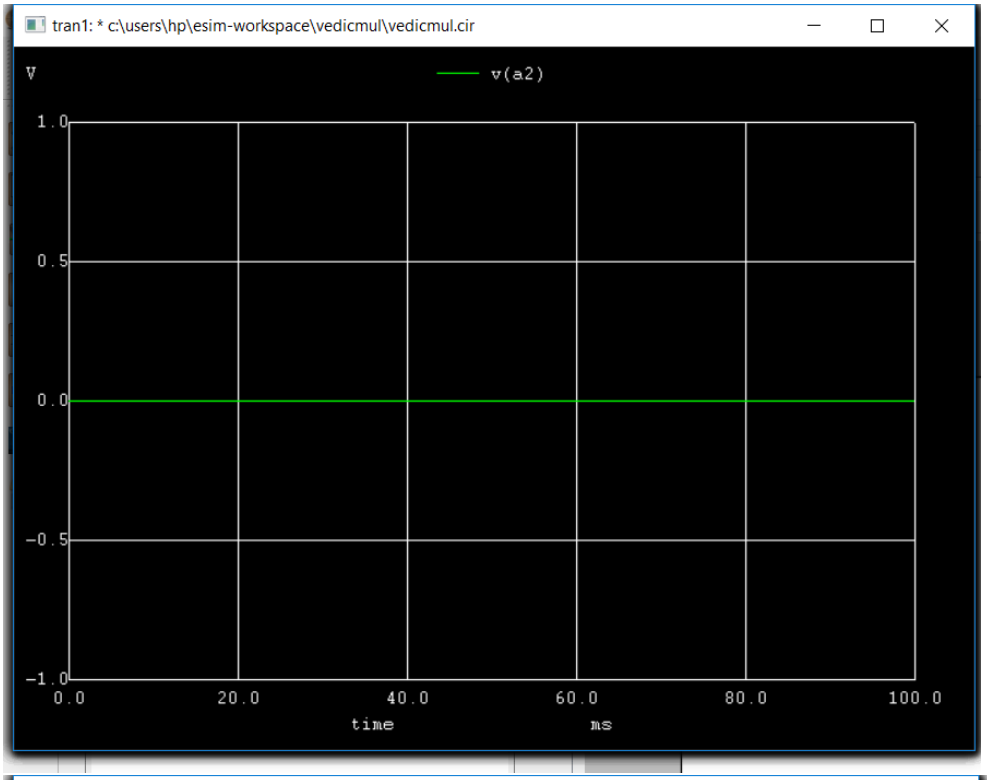
Subcircuit of Carry Look Ahead Adder

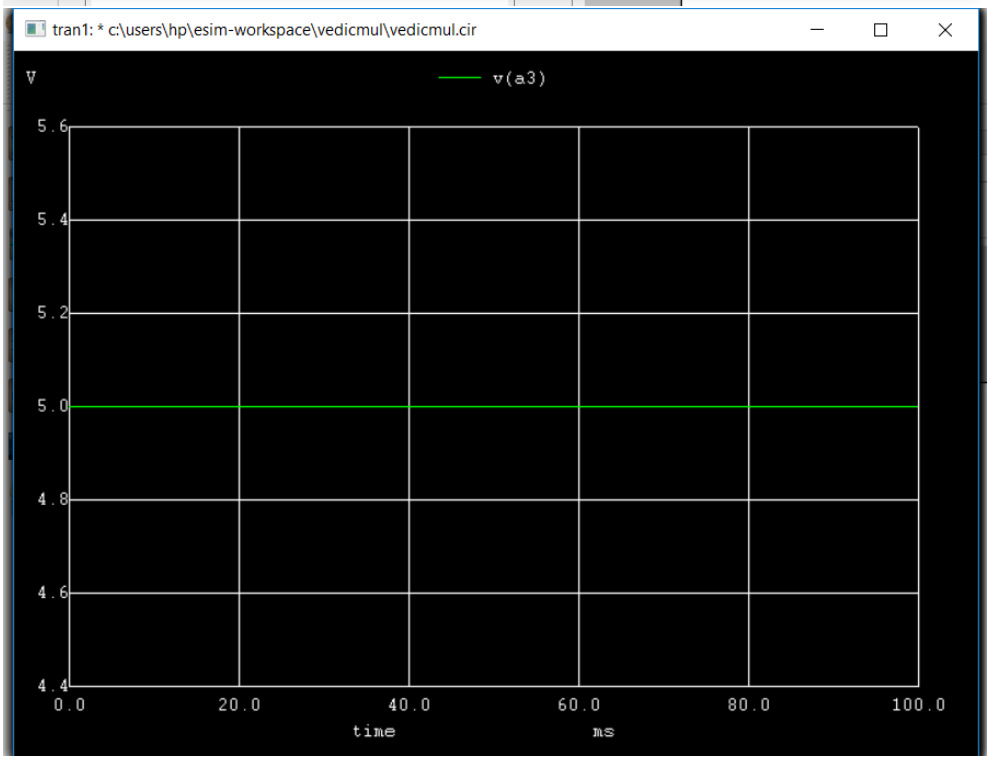


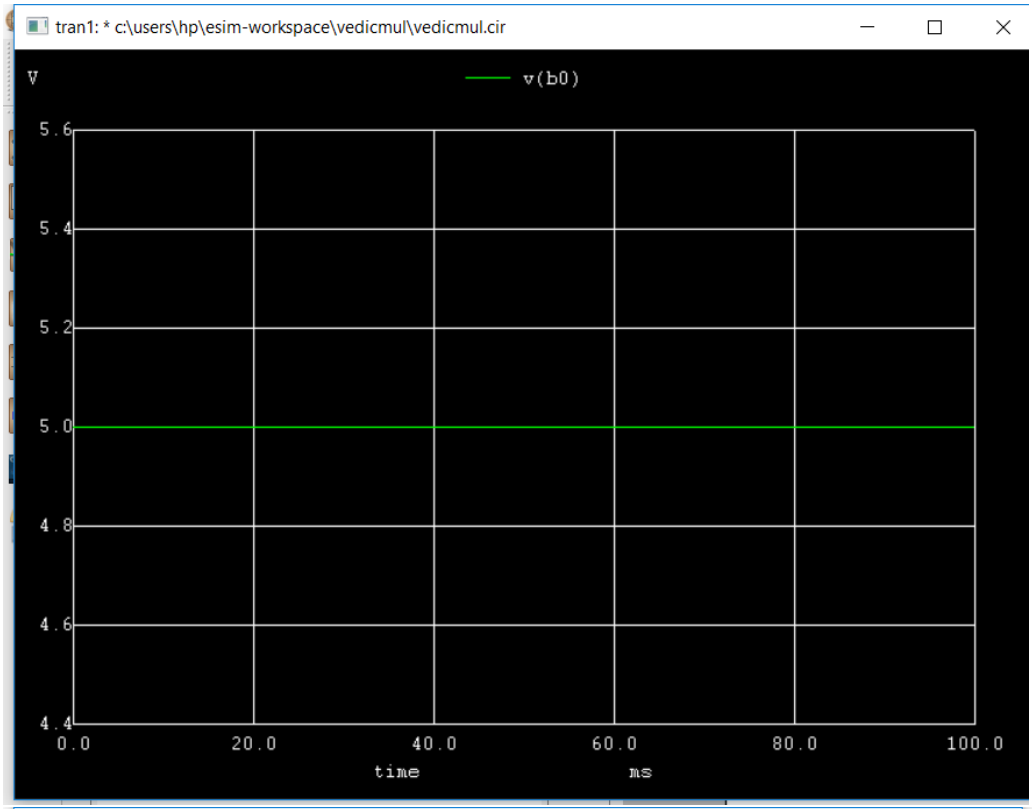
Input Ngspice Plots:

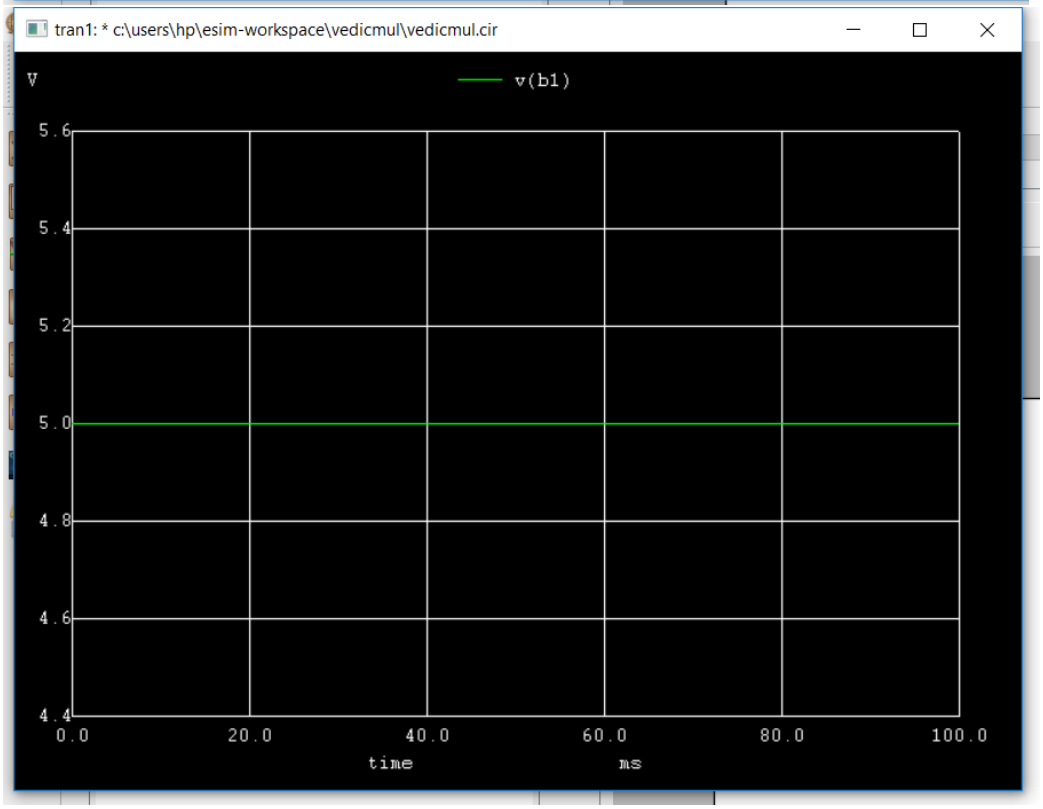


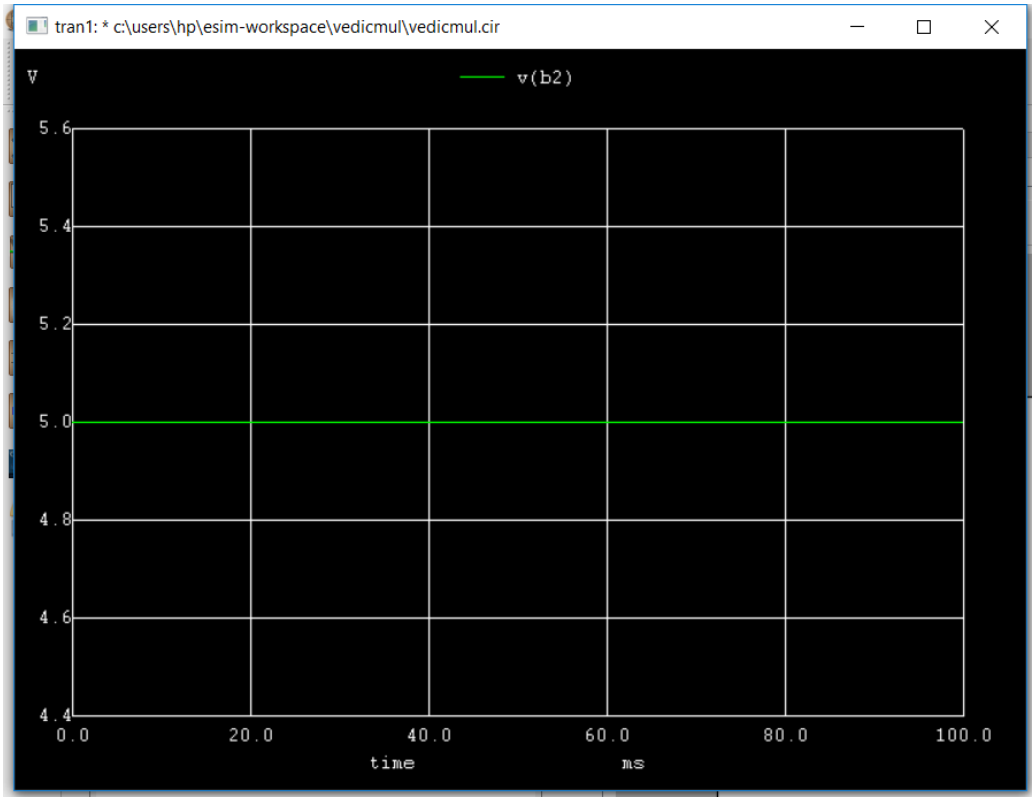


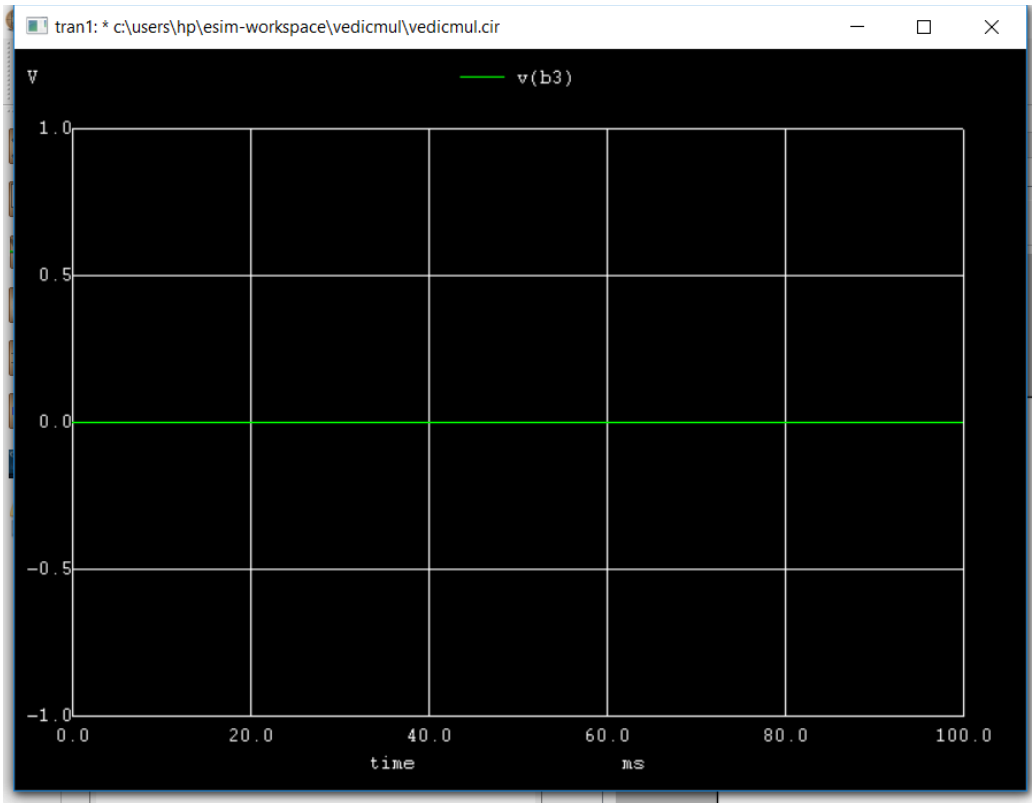

tran1: * c:\users\hp\esim-workspace\vedicmul\vedicmul.cir
V
v(a2)
1.0
0.5
0.0
-0.5
-1.0
0.0
20.0
40.0
60.0
80.0
100.0
time
ms


tran1: * c:\users\hp\esim-workspace\vedicmul\vedicmul.cir
V
v(a3)
5.6
5.4
5.2
5.0
4.8
4.6
4.4
0.0
20.0
40.0
60.0
80.0
100.0
time
ms

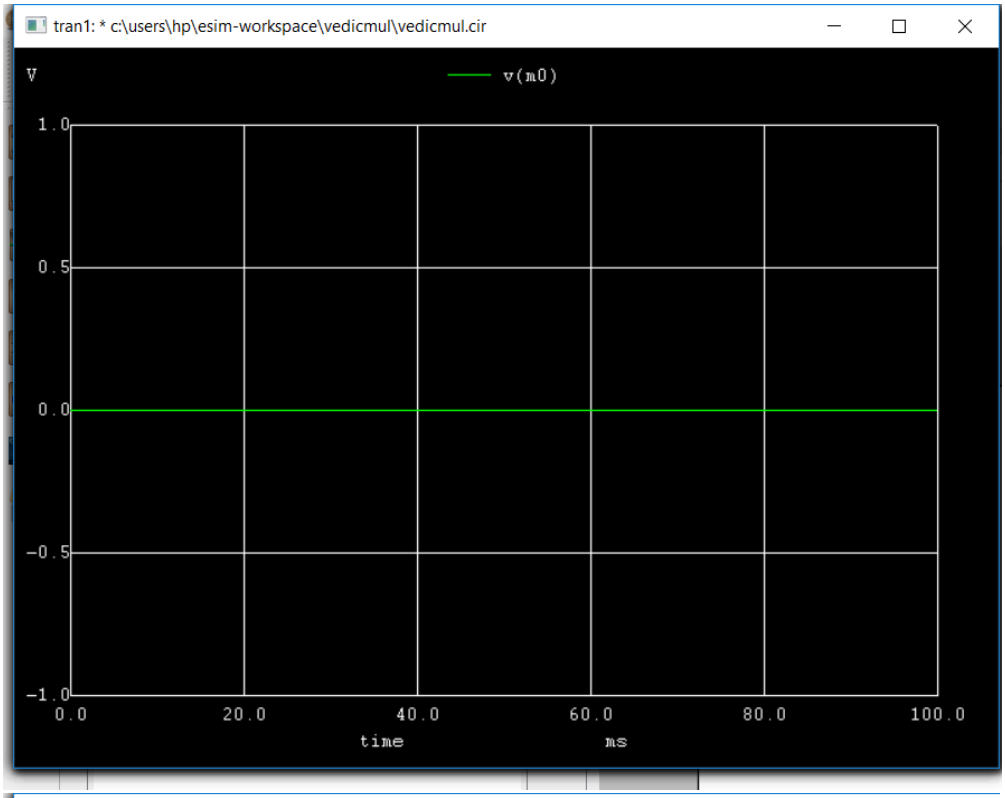

tran1: * c:\users\hp\esim-workspace\vedicmul\vedicmul.cir
V
v(b0)
5.6
5.4
5.2
5.0
4.8
4.6
4.4
0.0
20.0
40.0
60.0
80.0
100.0
time
ms

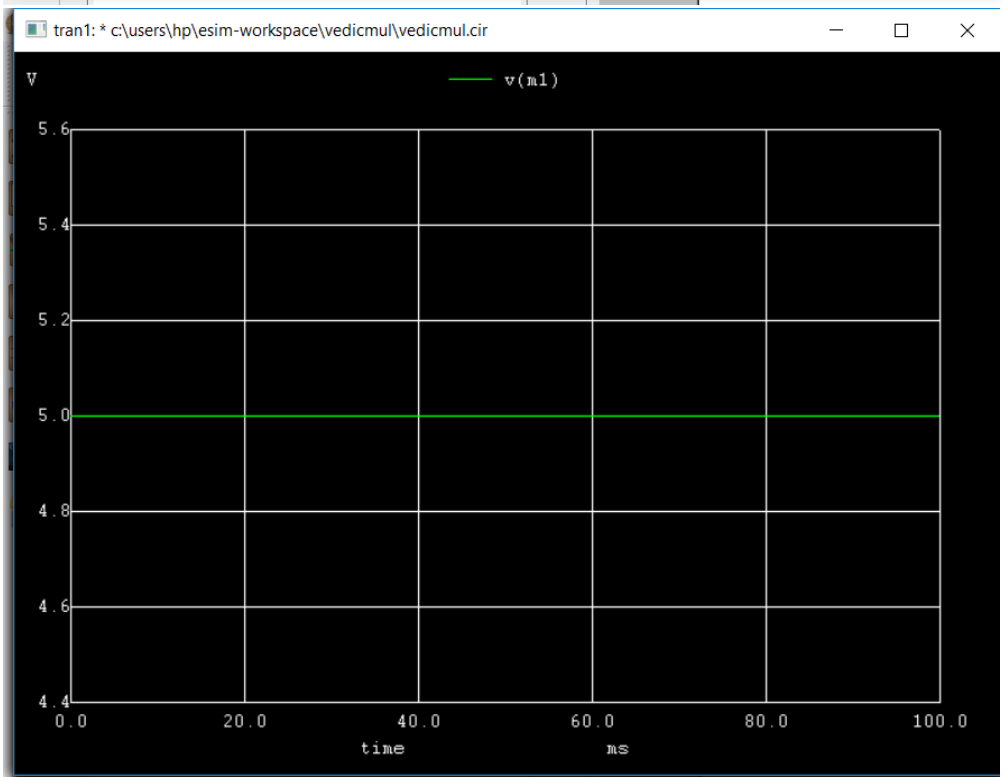

tran1: * c:\users\hp\esim-workspace\vedicmul\vedicmul.cir
V
v(b1)
5.6
5.4
5.2
5.0
4.8
4.6
4.4
0.0
20.0
40.0
60.0
80.0
100.0
time
ms

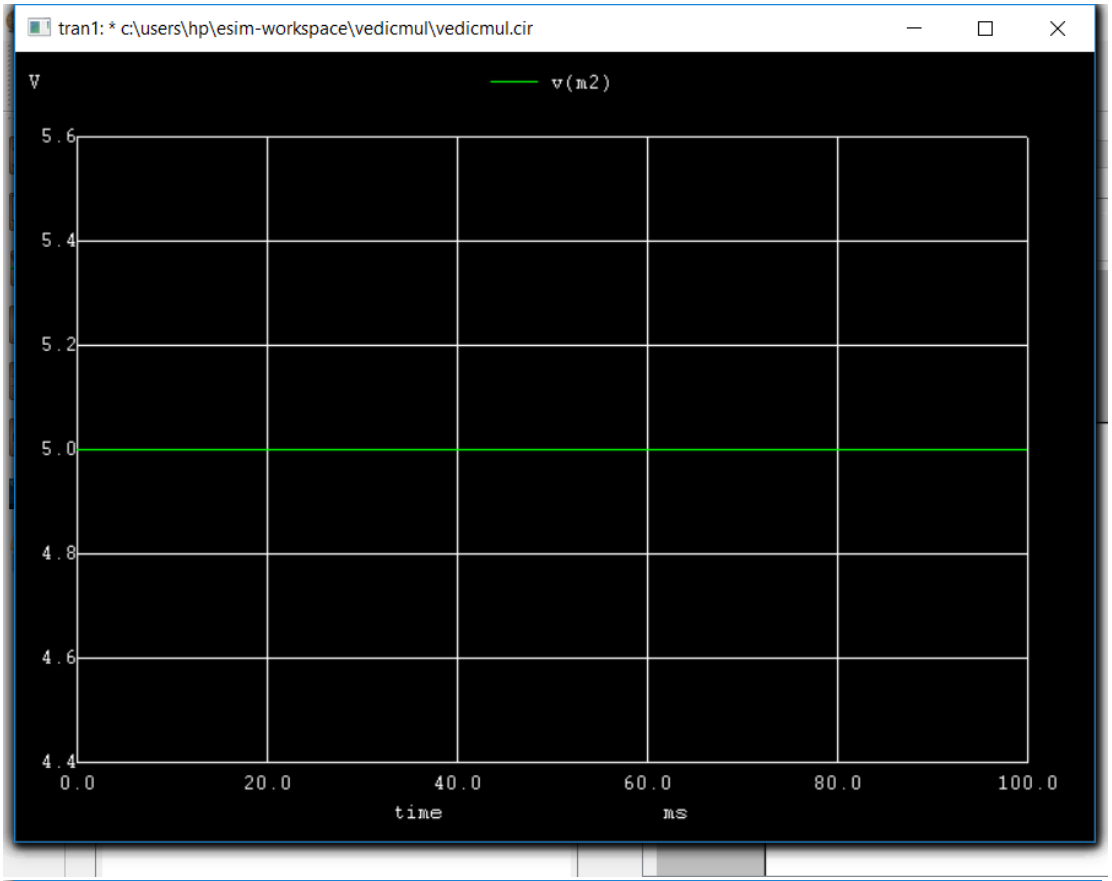

tran1: * c:\users\hp\esim-workspace\vedicmul\vedicmul.cir
V
v(b2)
5.6
5.4
5.2
5.0
4.8
4.6
4.4
0.0
20.0
40.0
60.0
80.0
100.0
time
ms

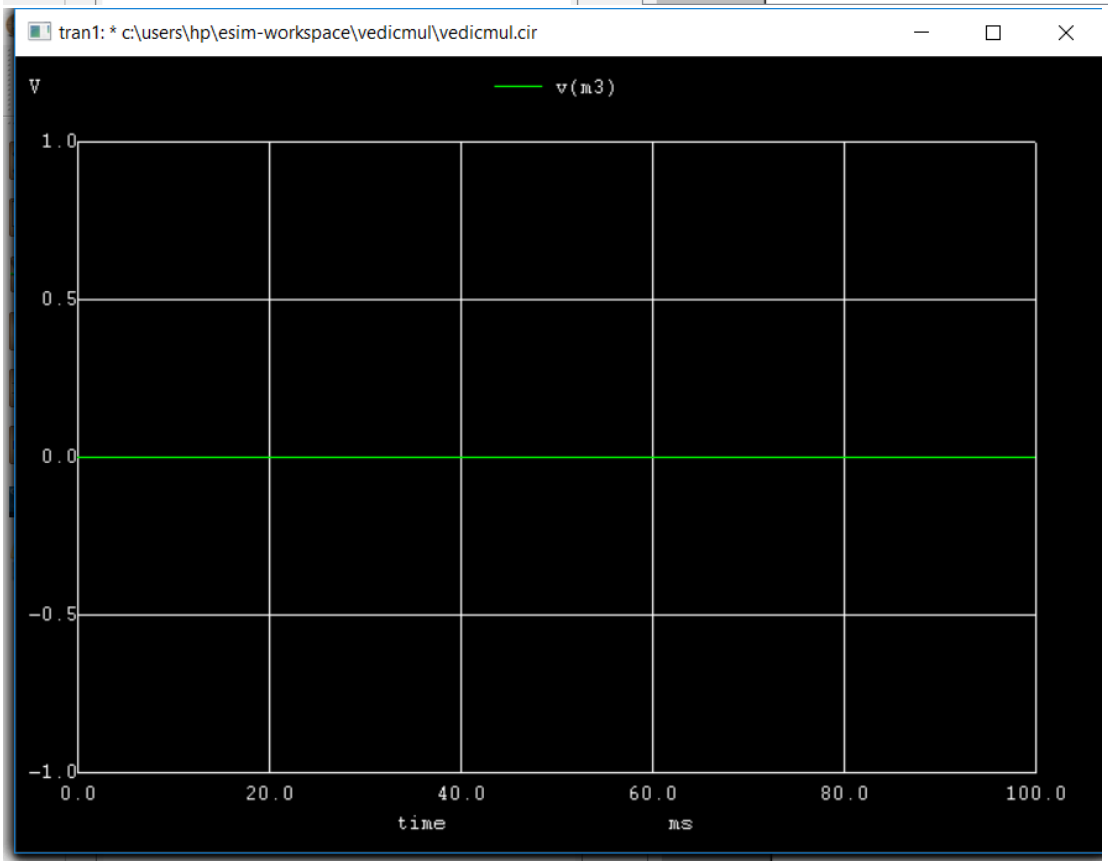

tran1: * c:\users\hp\esim-workspace\vedicmul\vedicmul.cir
V
v(b3)
1.0
0.5
0.0
-0.5
-1.0
0.0
20.0
40.0
60.0
80.0
100.0
time
ms

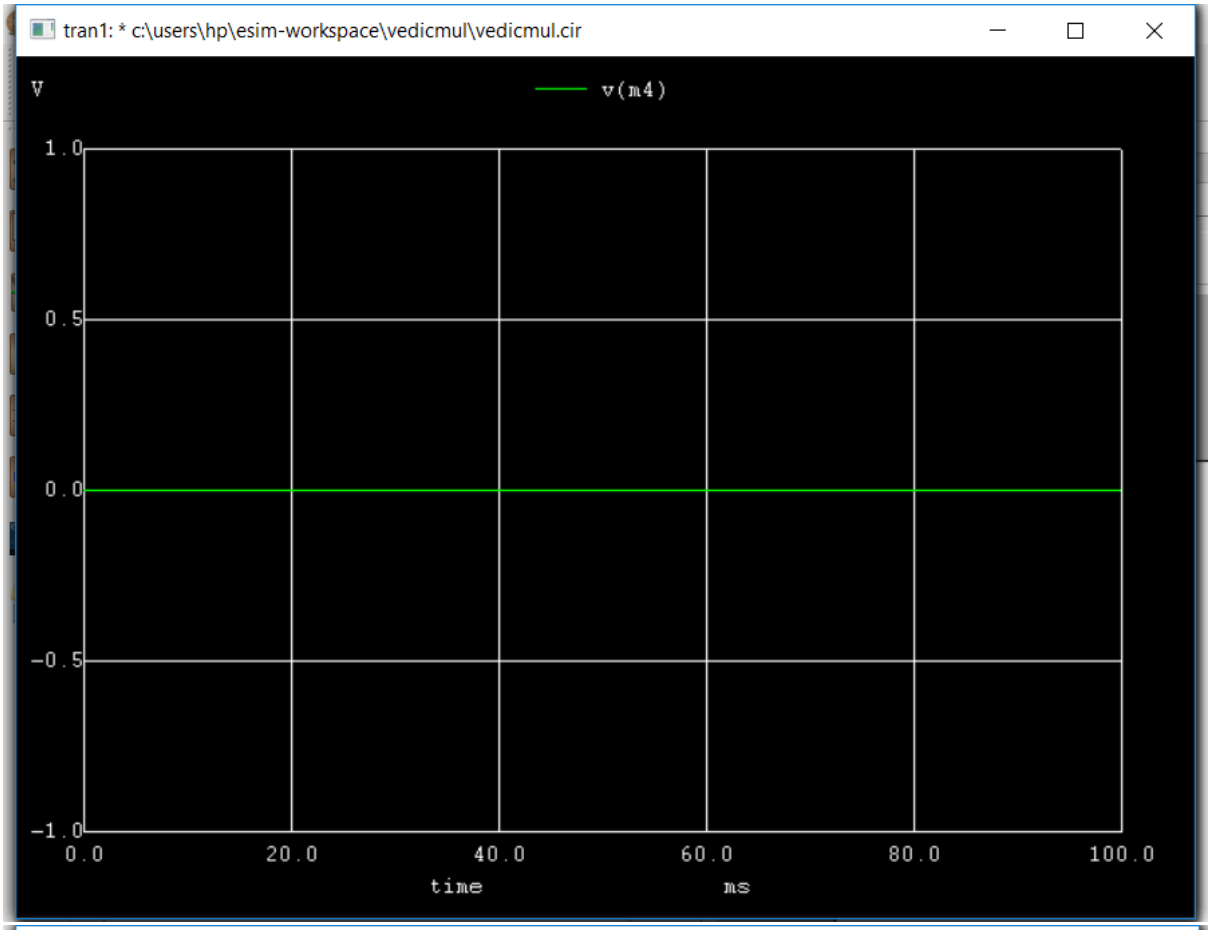
Output Ngspice Plots:

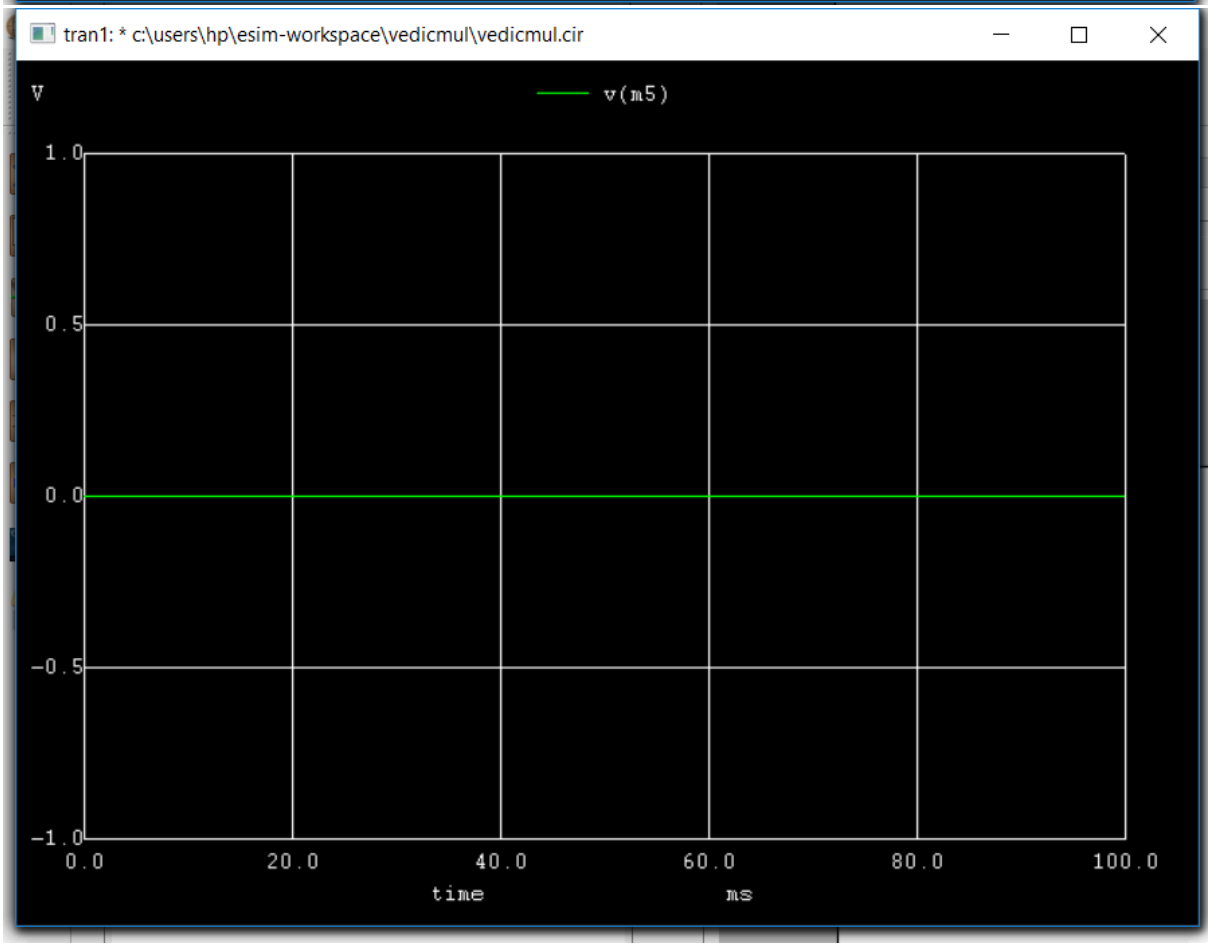


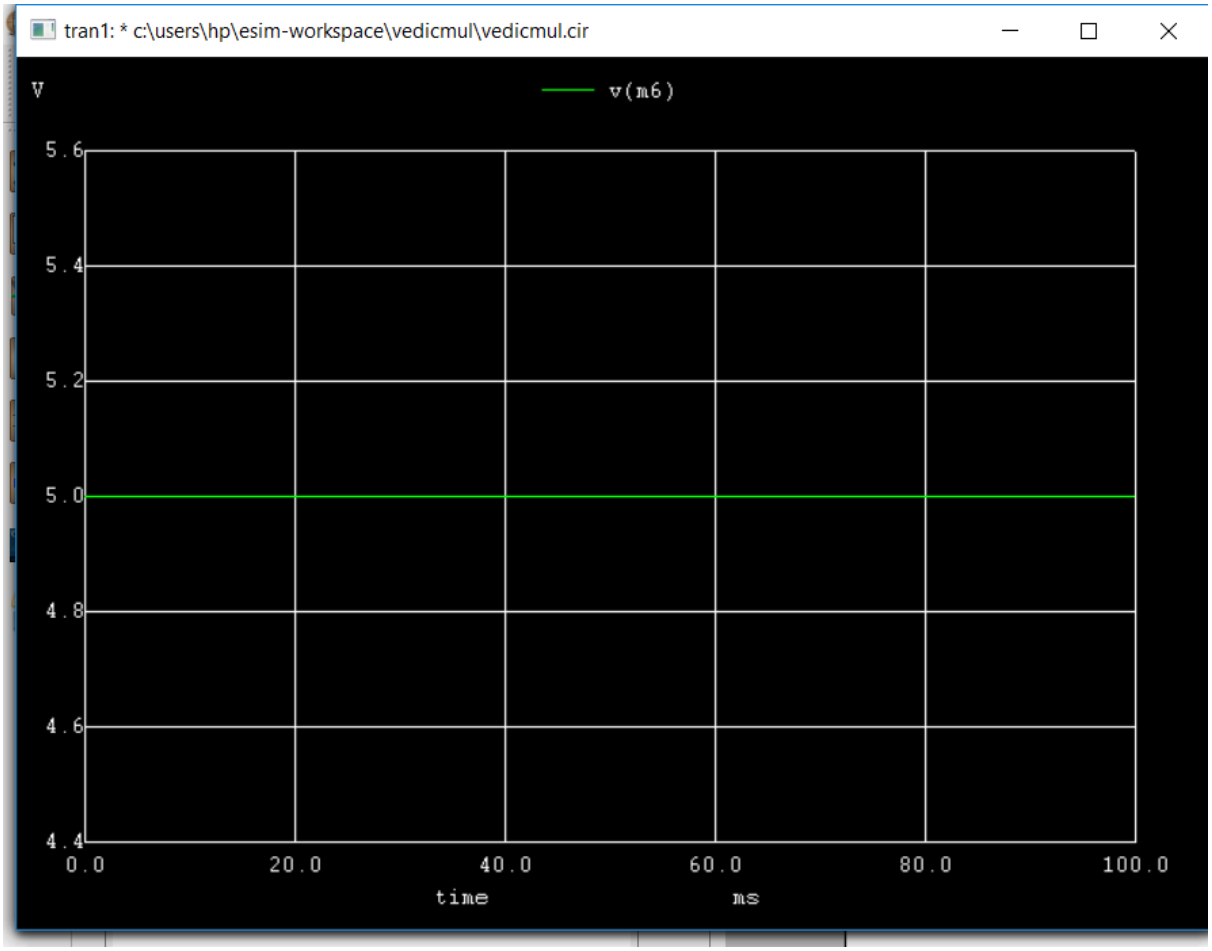


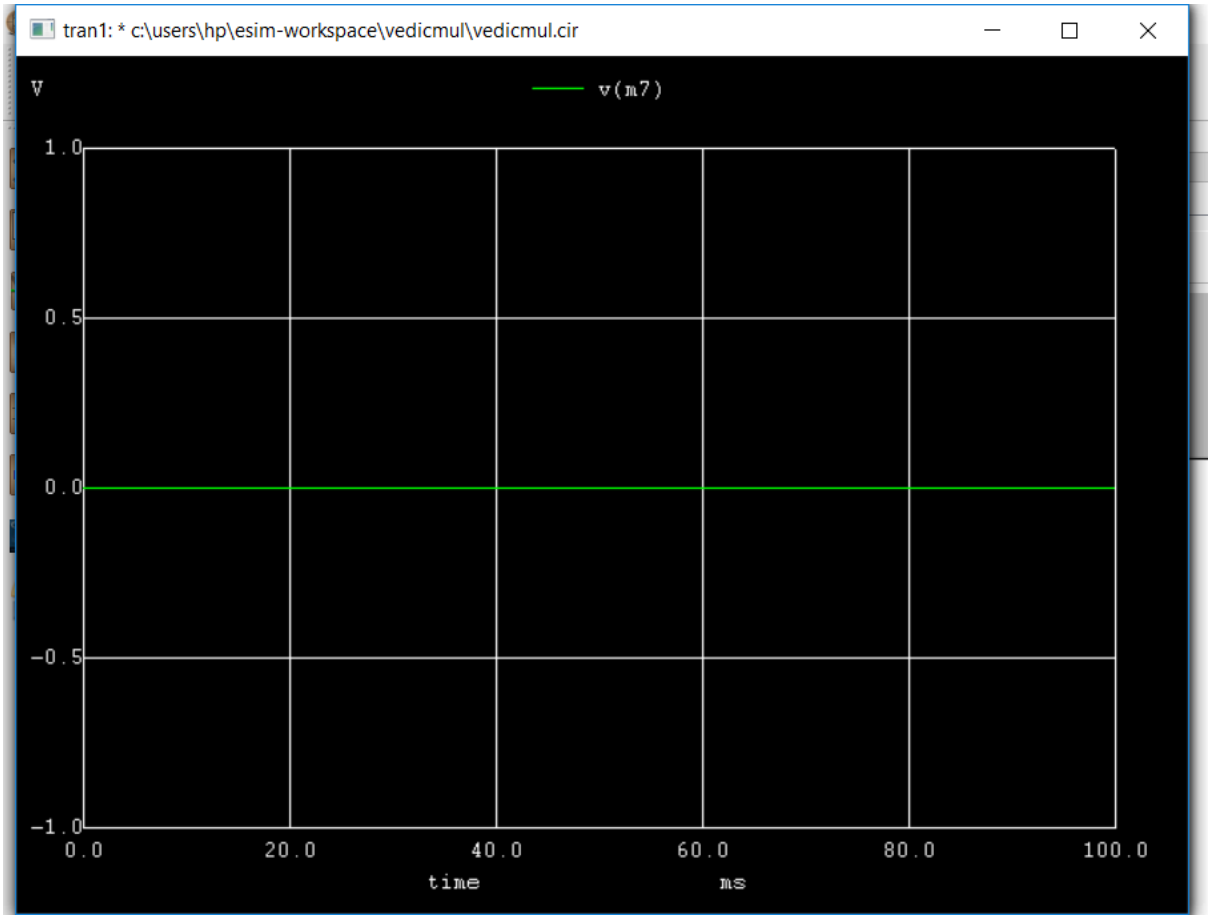

tran1: * c:\users\hp\esim-workspace\vedicmul\vedicmul.cir
V
v(m2)
5.6
5.4
5.2
5.0
4.8
4.6
4.4
0.0
20.0
40.0
60.0
80.0
100.0
time
ms


tran1: * c:\users\hp\esim-workspace\vedicmul\vedicmul.cir
V
v(m3)
1.0
0.5
0.0
-0.5
-1.0
0.0
20.0
40.0
60.0
80.0
100.0
time
ms

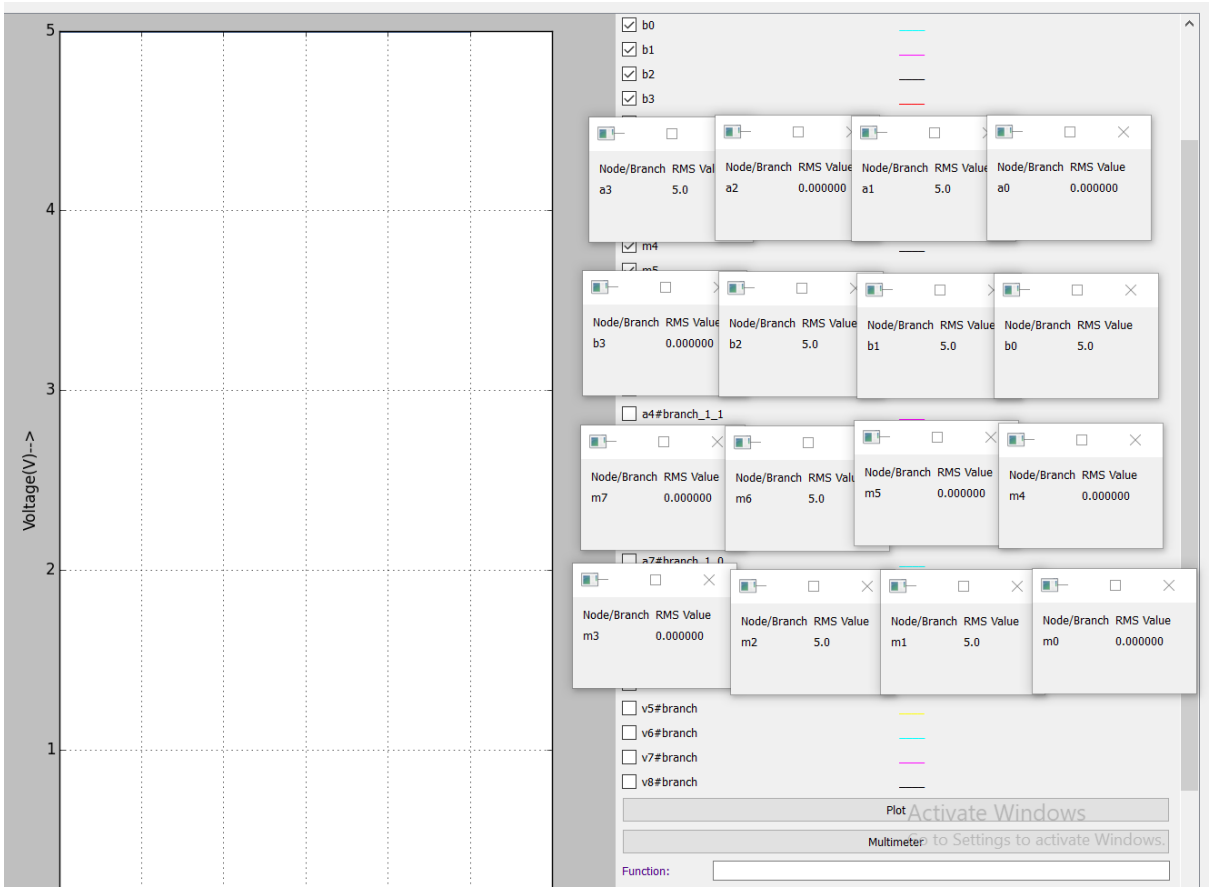

tran1: * c:\users\hp\esim-workspace\vedicmul\vedicmul.cir
V
v(m4)
1.0
0.5
0.0
-0.5
-1.0
0.0
20.0
40.0
60.0
80.0
100.0
time
ms


tran1: * c:\users\hp\esim-workspace\vedicmul\vedicmul.cir
V
v(m5)
1.0
0.5
0.0
-0.5
-1.0
0.0
20.0
40.0
60.0
80.0
100.0
time
ms


tran1: * c:\users\hp\esim-workspace\vedicmul\vedicmul.cir
V
v(m6)
5.6
5.4
5.2
5.0
4.8
4.6
4.4
0.0
20.0
40.0
60.0
80.0
100.0
time
ms


tran1: * c:\users\hp\esim-workspace\vedicmul\vedicmul.cir
V
v(m7)
1.0
0.5
0.0
-0.5
-1.0
0.0
20.0
40.0
60.0
80.0
100.0
time
ms

Python Plot:



References:

https://www.researchgate.net/figure/bit-multiplier-design1_fig7_273137511