

## Title :- 8 BIT BINARY MAGNITUDE COMPARATOR

### Theory :-

8bit comparator is implemented using two 4 bit comparators in cascaded mode.

A 4-Bit Magnitude Comparator which compares two 4-bit words (A, B), each word having four Parallel Inputs ( $A_0 - A_3$ ,  $B_0 - B_3$ );  $A_3$ ,  $B_3$  being the most significant inputs.

Here the subcircuit named 7485 is a 4 bit comparator.

Three Outputs are provided: "A greater than B" ( $A > B$ (out)),  
 "A equal to B" ( $A = B$ (out)),  
 "A less than B" ( $A < B$ (out)),

Three Expander Inputs,  $A > B$ (in),  $A = B$ (in),  $A < B$ (in), allow cascading without external gates.

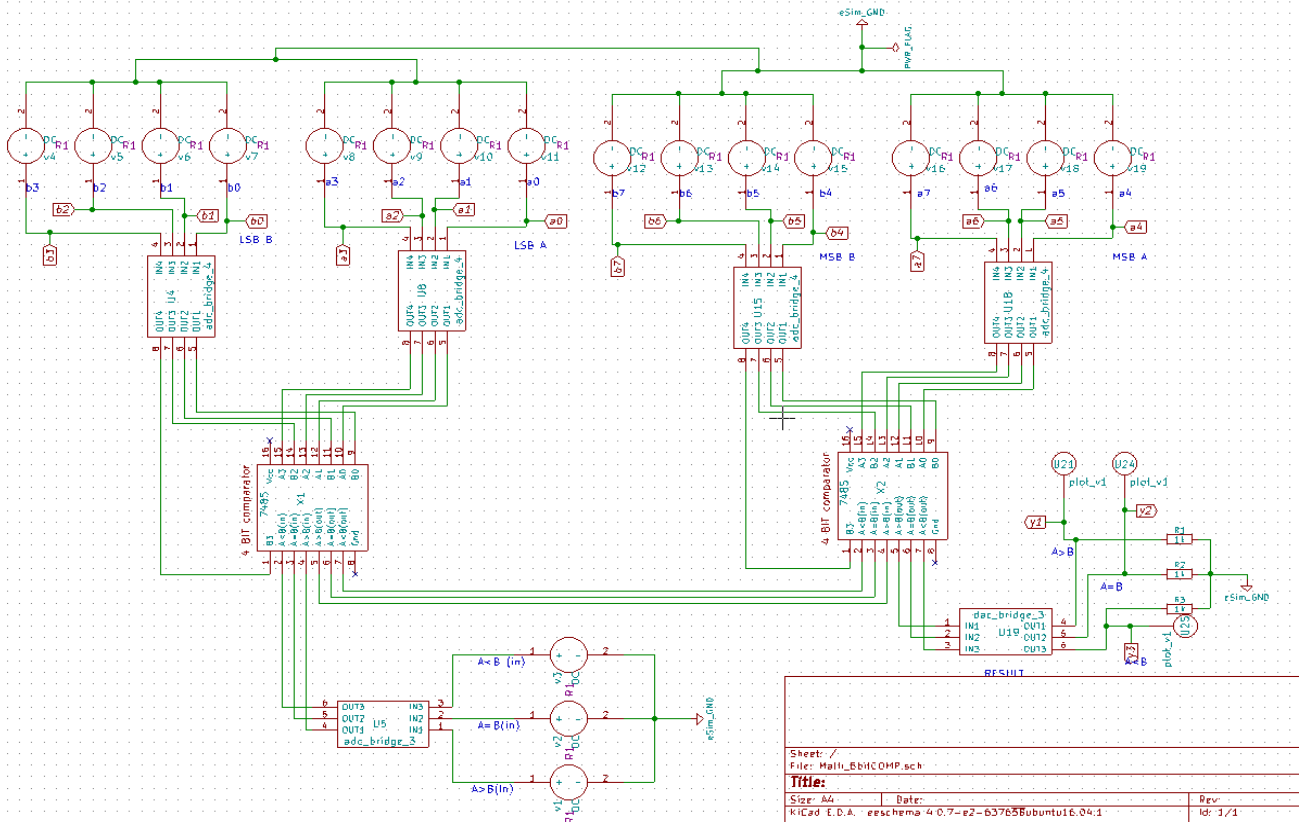
For proper compare operation, the Expander Inputs to the least significant position must be connected as follows:  $A > B$ (in)='low',  $A = B$ (in)='high',  $A < B$ (in)='low'.

For serial (ripple) expansion, the  $A > B$ (out),  $A = B$ (out),  $A < B$ (out), Outputs are connected respectively to the  $A > B$ (in),  $A = B$ (in),  $A < B$ (in) Inputs of the next most significant comparator

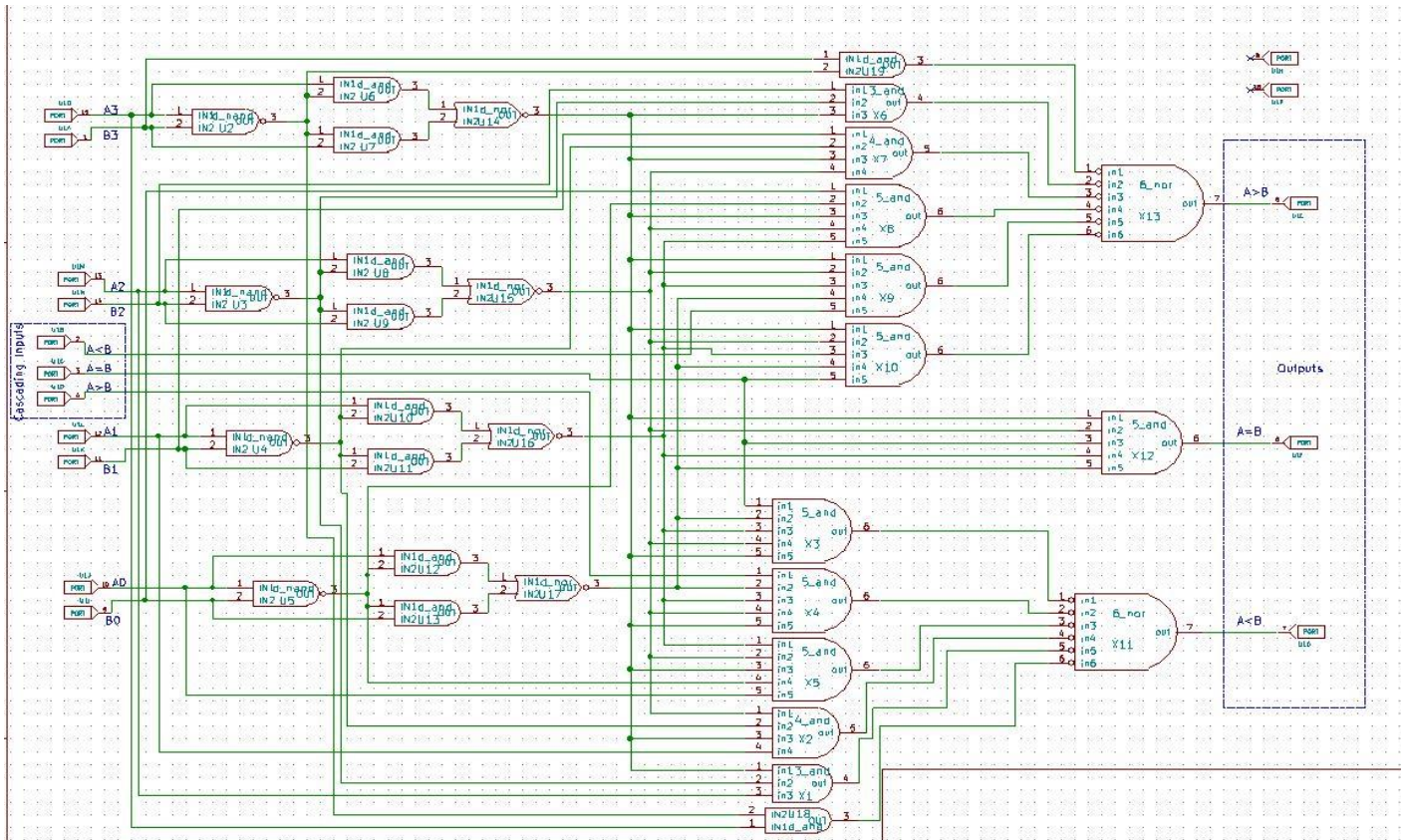
**Table 10.1 Truth table of 7485**

Comparing inputs						Cascading inputs			Outputs				
$A_3$	$B_3$	$A_2$	$B_2$	$A_1$	$B_1$	$A_0$	$B_0$	$A > B$	$A < B$	$A = B$	$A > B$	$A < B$	$A = B$
$A_3 > B_3$		x		x		x		x	x	x	1	0	0
$A_3 < B_3$		x		x		x		x	x	x	0	1	0
$A_3 = B_3$	$A_2 > B_2$			x		x		x	x	x	1	0	0
$A_3 = B_3$	$A_2 < B_2$			x		x		x	x	x	0	1	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 > B_1$				x		x	x	x	1	0	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 < B_1$				x		x	x	x	0	1	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 > B_0$					x	x	x	1	0	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 < B_0$					x	x	x	0	1	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$					1	0	0	1	0	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$					0	1	0	0	1	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$					0	0	1	0	0	1
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$					x	x	1	0	0	1
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$					1	1	0	0	0	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$					0	0	0	1	1	0

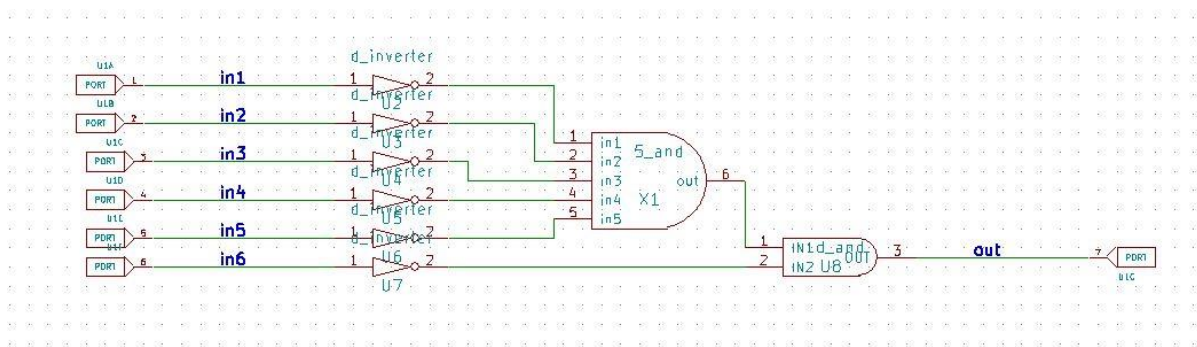
# Schematic Diagram :-



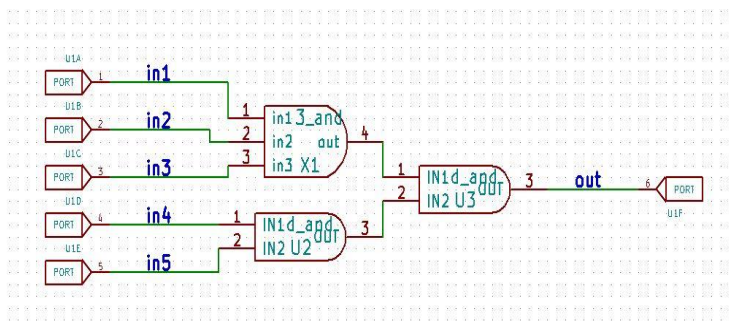
# Subcircuit schematic for 7485 block :-



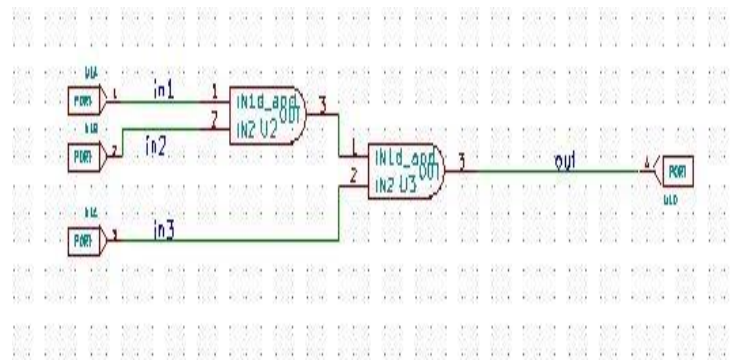
### Subcircuit Schematic for “6\_nor” used in 7485 :-



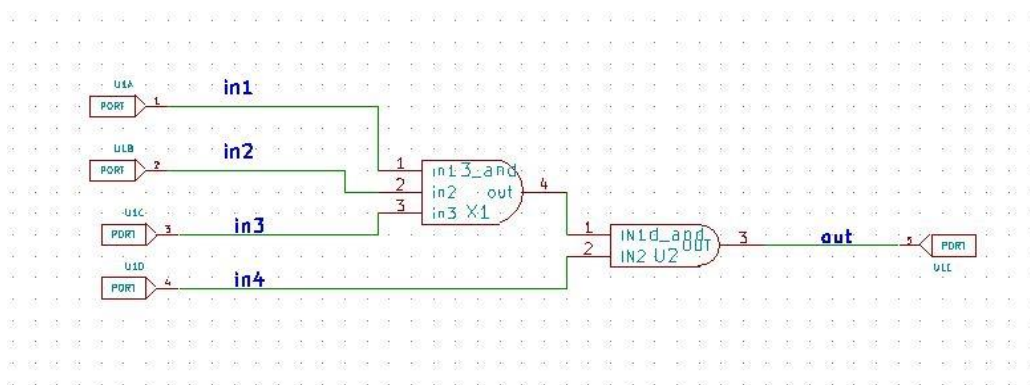
### Subcircuit Schematic for “5\_and” used :-



### Subcircuit for “3\_and”:-



### Subcircuit Schematic for “4\_and” used:-



NOTE :- Here in E-SIM software, no need to connect Vcc( pin 16 ) and GND ( pin 8 ) pins to Dc source and gnd respectively , you can leave them unconnected using NO CONNECT symbol . This is because in circuit simulation softwares , we use BASIC GATES (AND, NAND etc.) they don't need Vcc and GND. As in manufacturing an IC , they use MOSFETs to implement those GATES ,there MOSFETs require Vcc and Gnd

## Simulation Results :-

Input:-

A[7 : 0] - 0 1 1 0 1 0 0 0

B[7 : 0] - 1 0 0 1 0 0 0 0

A	Bit	Voltage source	Value (v)
7	0	V16	0
6	1	V 17	5
5	1	V18	5
4	0	V19	0
3	1	V8	5
2	0	V9	0
1	0	V10	0
0	0	V11	0

B	Bit	Voltage source	Value (v)
7	1	V12	5
6	0	V 13	0
5	0	V14	0
4	1	V15	5
3	0	V4	0
2	0	V5	0
1	0	V6	0
0	0	V7	0

Output :-

Plot y1 corresponds to  $A > B$

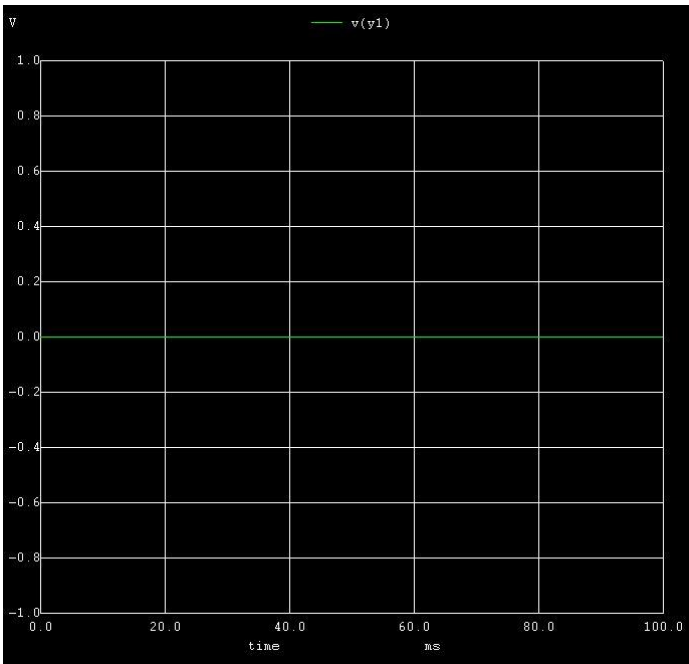
Plot y2 corresponds to  $A = B$

Plot y3 corresponds to  $A < B$

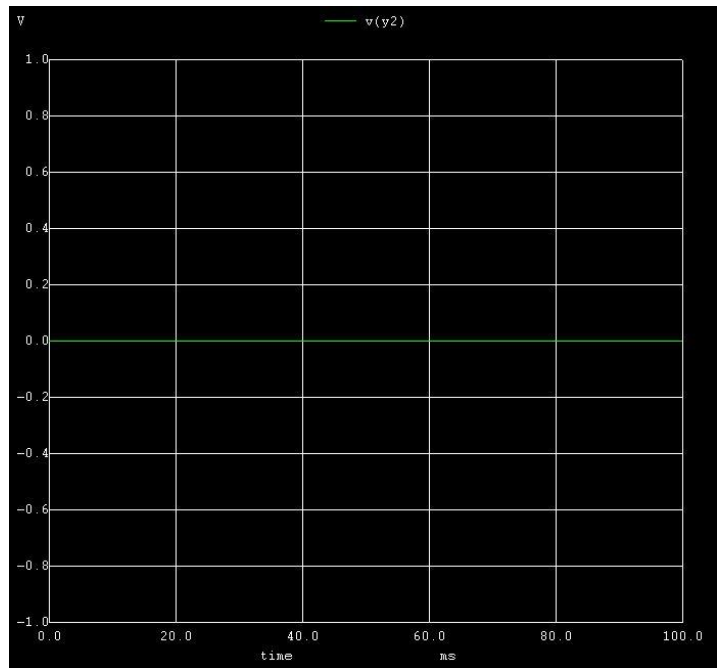
RESULT:-  $A < B$  i.e.  $y_3 = 5v$

# Ngspice Plots

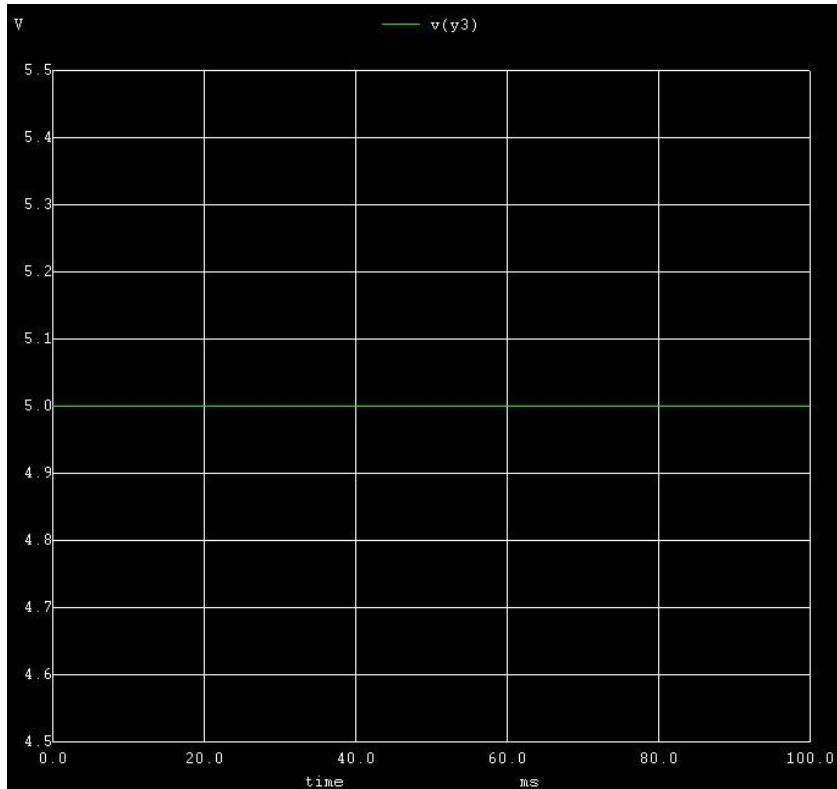
Y1 (A>B)



y2 (A=B)

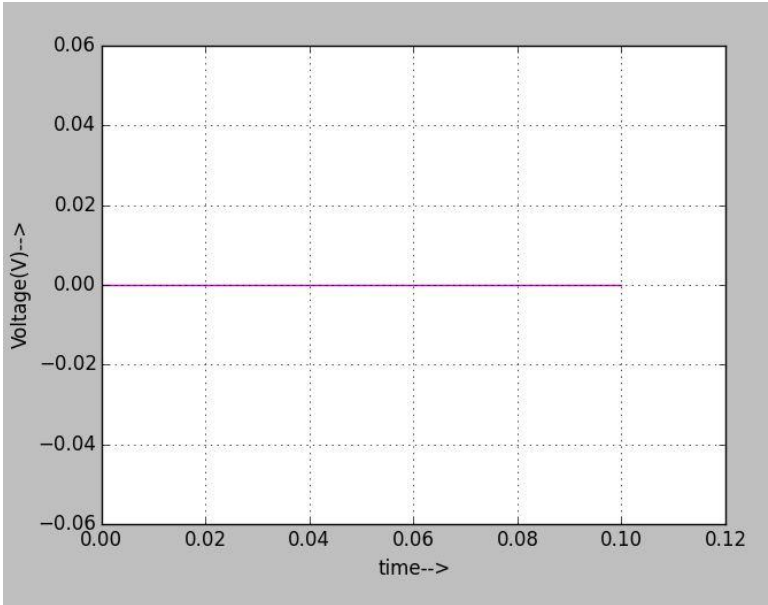


Y3 (A<B)

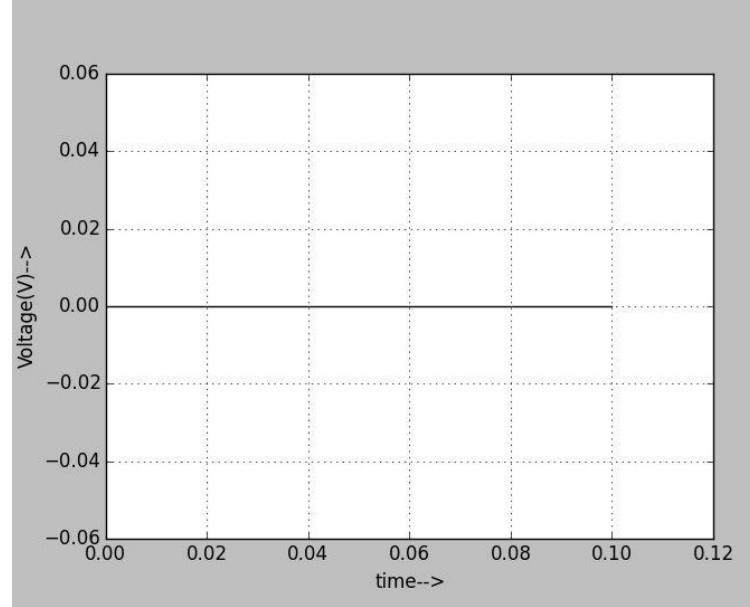


# Python Plots

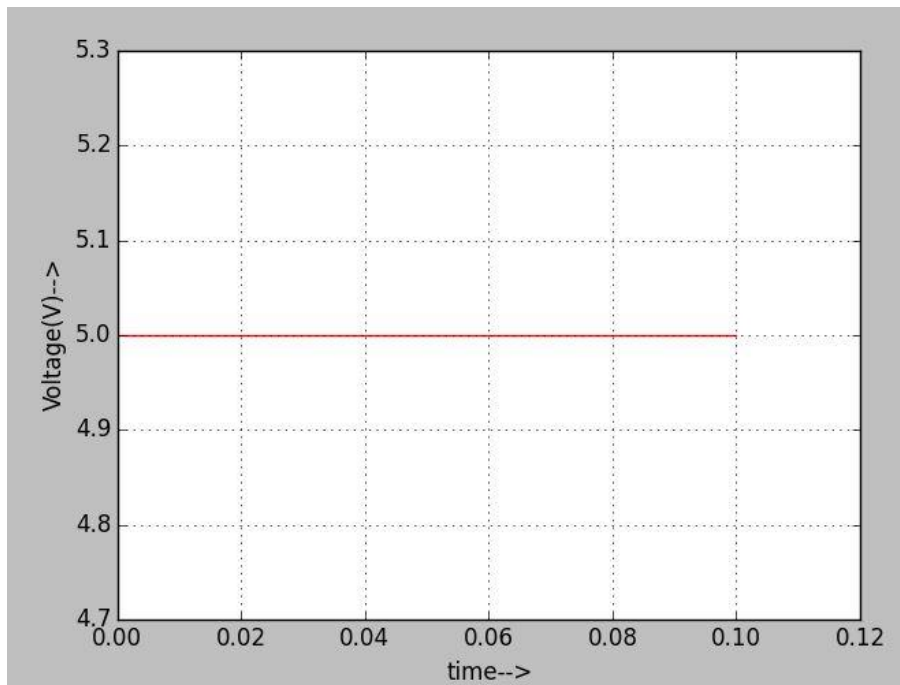
Y1 (A>B)



y2 (A=B)



Y3 (A<B)



fwef

Input:-

A[7:0] - 1 0 0 0 1 1 0 1

A	Bit	Voltage source	Value (v)
7	1	V16	5
6	0	V 17	0
5	0	V18	0
4	0	V19	0
3	1	V8	5
2	1	V9	5
1	0	V10	0
0	1	V11	5

B[7:0] - 1 0 0 0 1 1 0 0

B	Bit	Voltage source	Value (v)
7	1	V12	5
6	0	V 13	0
5	0	V14	0
4	0	V15	0
3	1	V4	5
2	1	V5	5
1	0	V6	0
0	0	V7	0

Output :-

Plot y1 corresponds to A>B

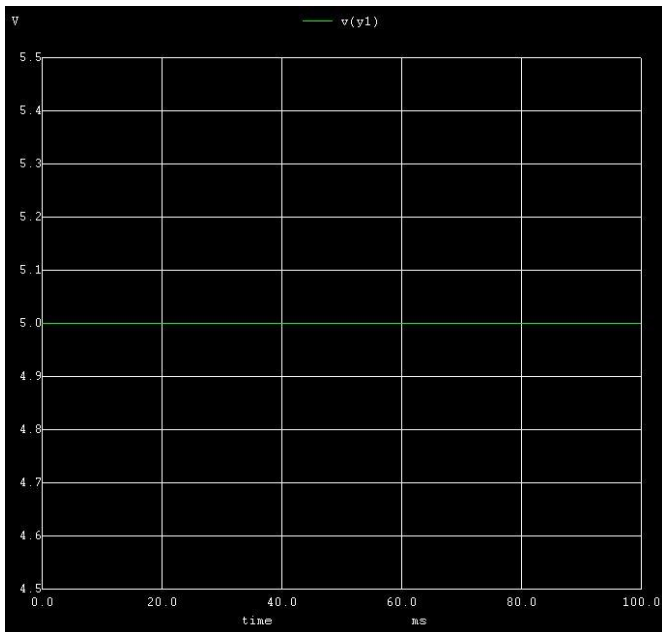
Plot y2 corresponds to A=B

Plot y3 corresponds to A<B

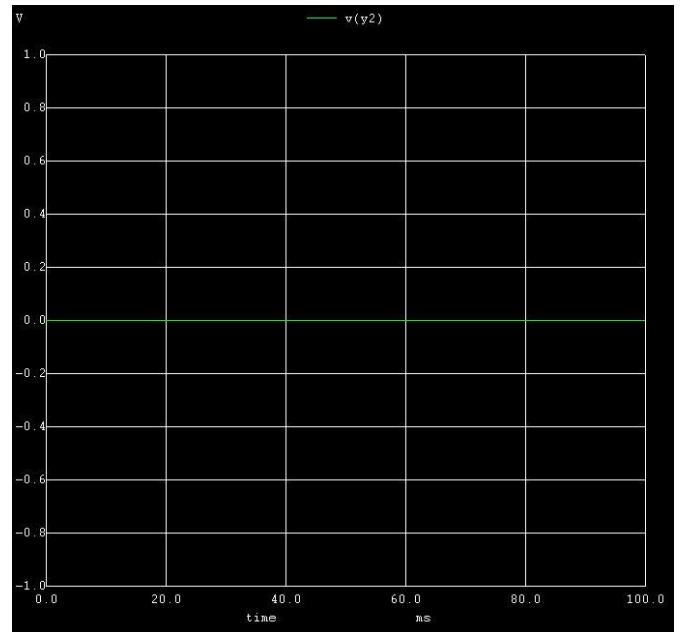
RESULT:- A>B i.e. y1 = 5v

# Ngspice Plots

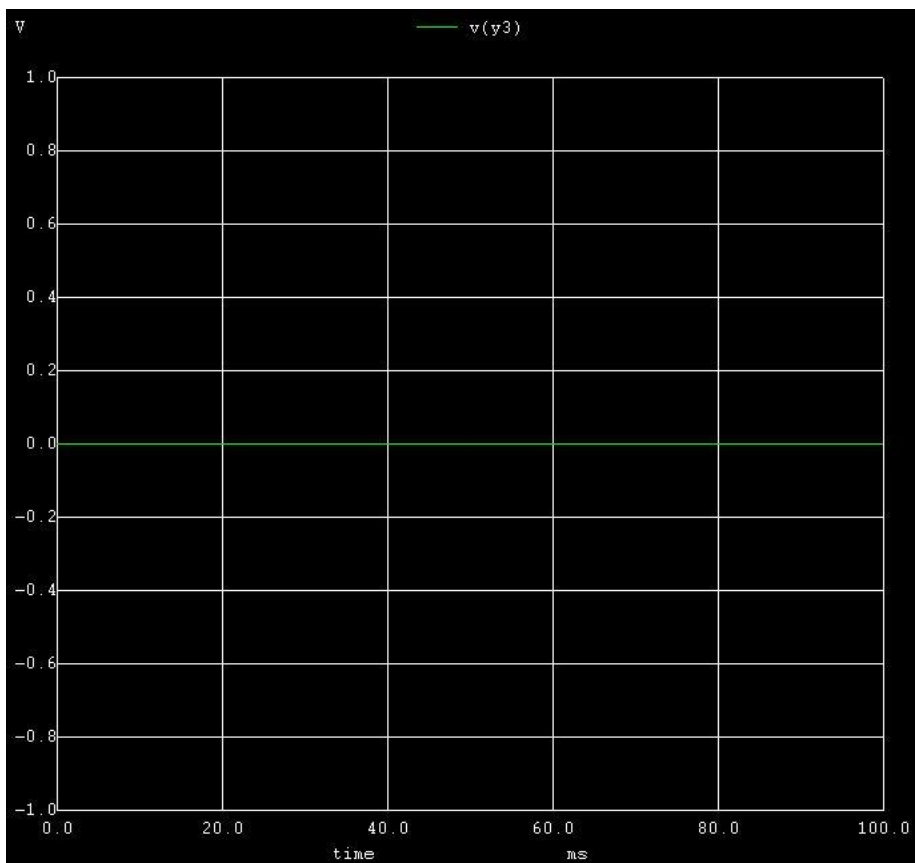
Y1 (A>B)



y2 (A=B)



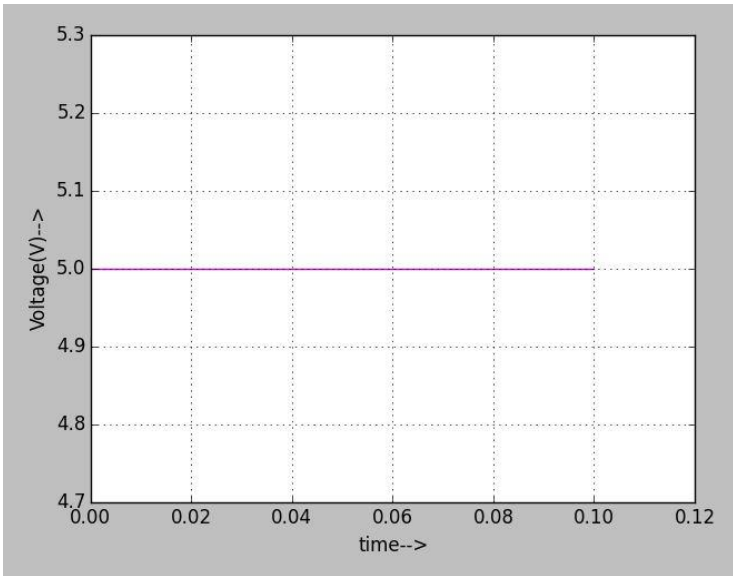
Y3 (A<B)



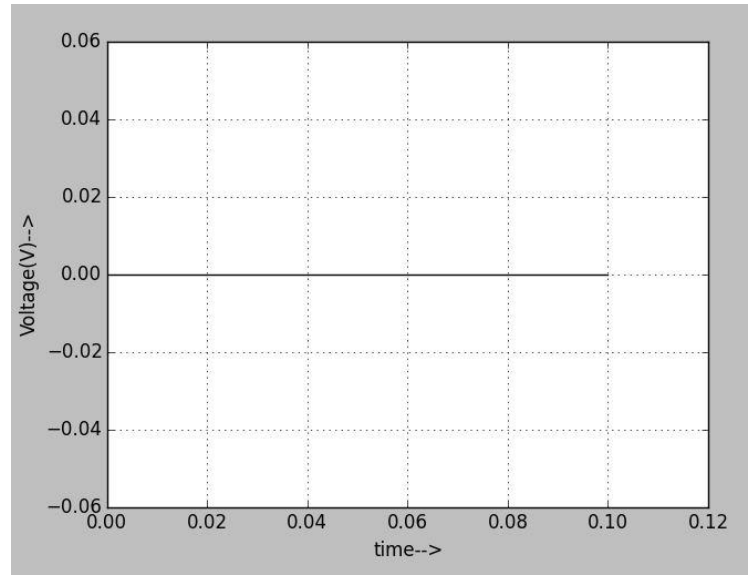


# Python Plots

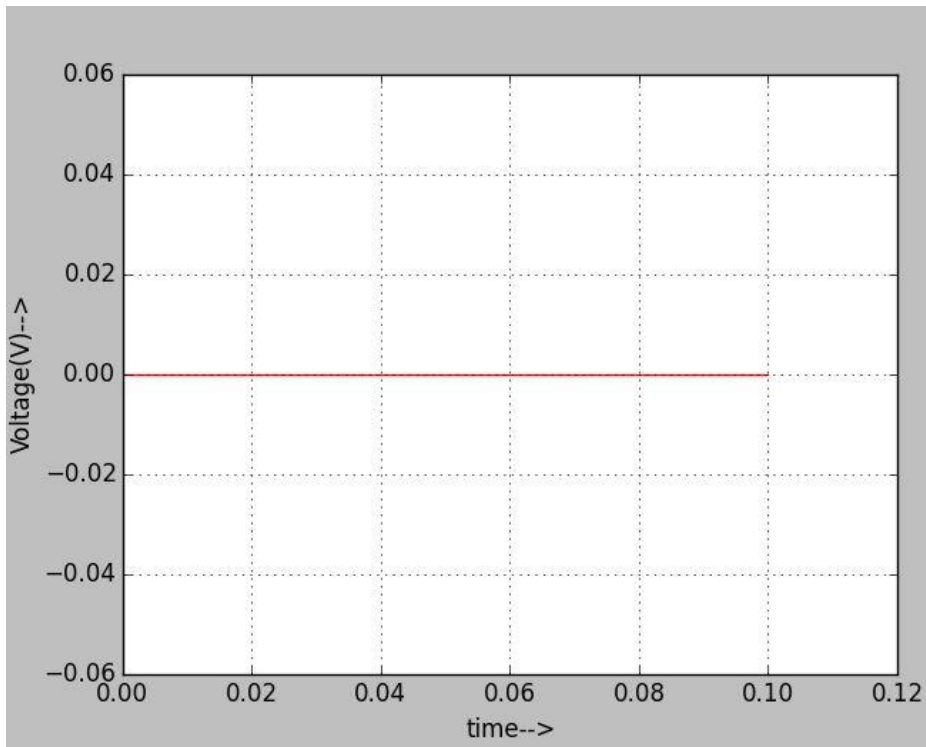
Y1 (A>B)



y2 (A=B)



Y3 (A<B)



Input:-

A[7:0] - 00001000

A	Bit	Voltage source	Value (v)
7	0	V16	0
6	0	V17	0
5	0	V18	0
4	0	V19	0
3	1	V8	5
2	0	V9	0
1	0	V10	0
0	0	V11	0

B[7:0] - 00001000

B	Bit	Voltage source	Value (v)
7	0	V12	0
6	0	V13	0
5	0	V14	0
4	0	V15	0
3	1	V4	5
2	0	V5	0
1	0	V6	0
0	0	V7	0

Output :-

Plot y1 corresponds to A>B

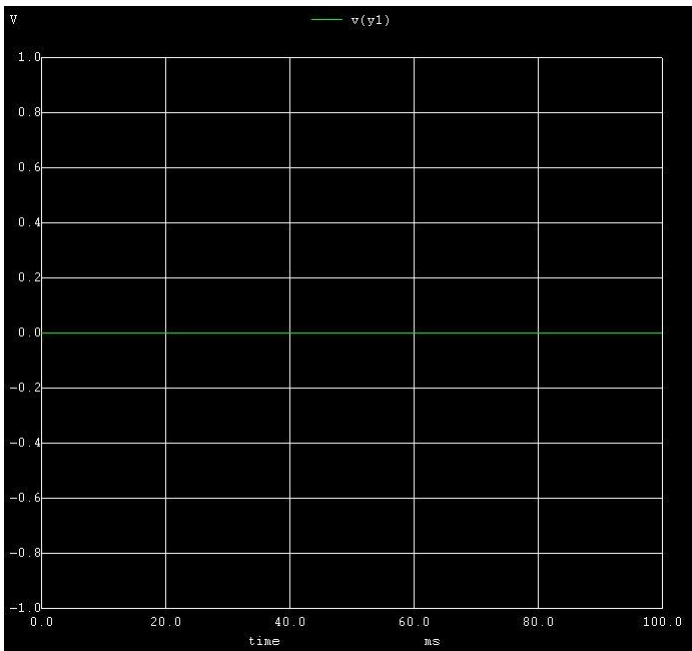
Plot y2 corresponds to A=B

Plot y3 corresponds to A<B

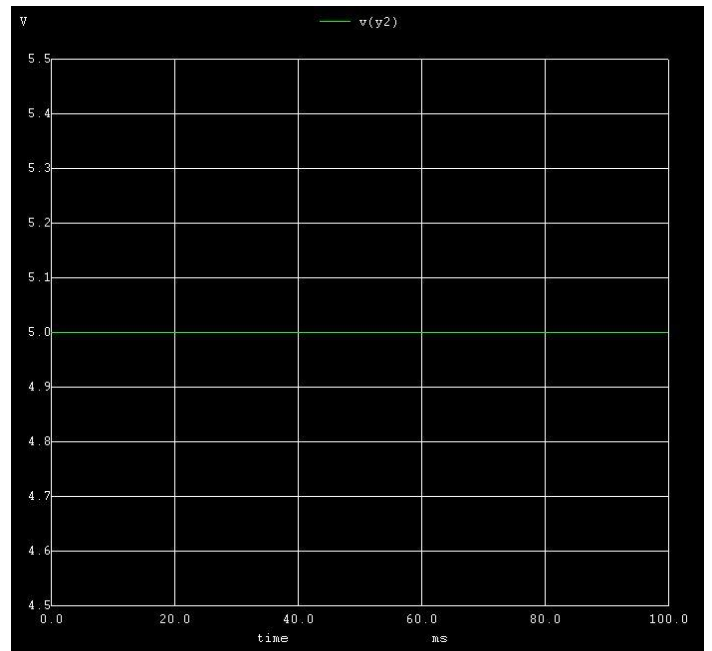
RESULT:- A=B i.e. y2 = 5v

# Ngspice Plots

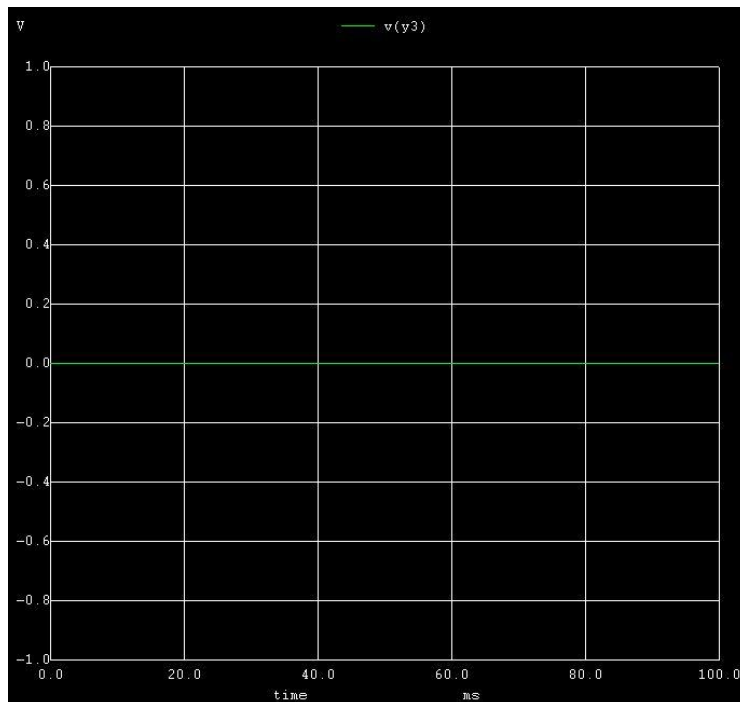
y1 (A>B)



y2 (A=B)

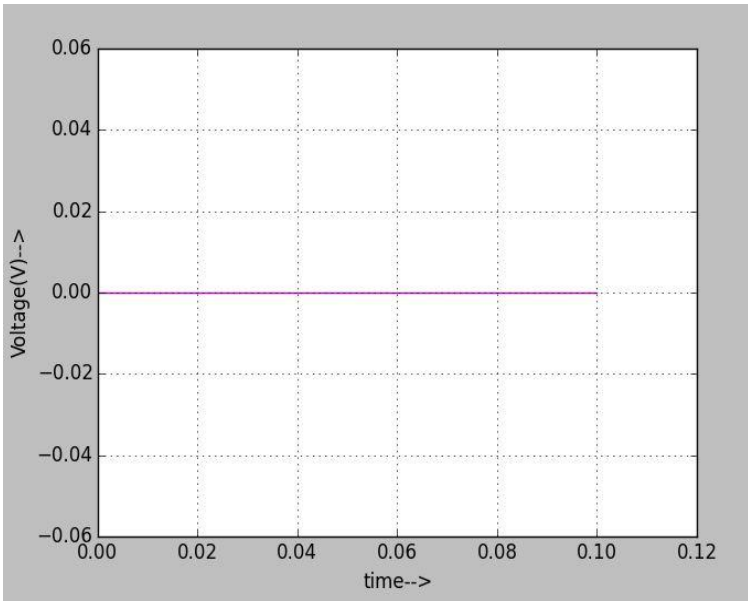


Y3 (A<B)

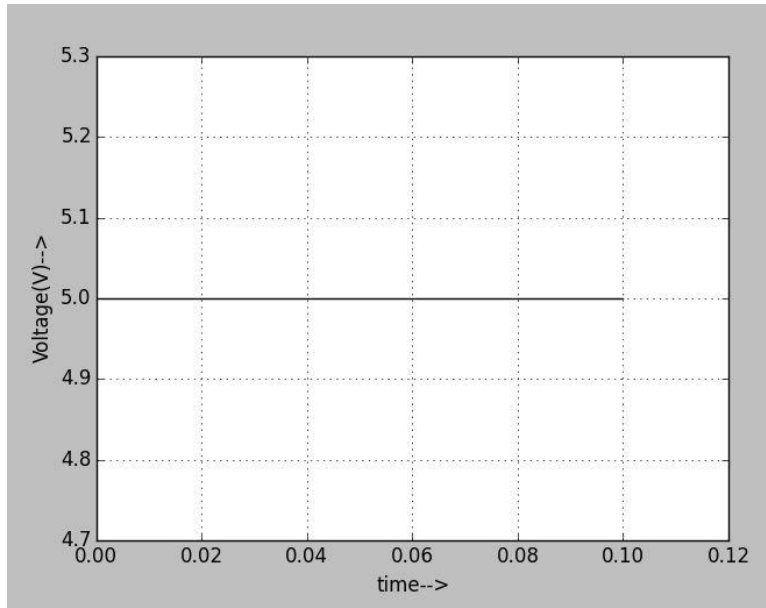


# Python Plots

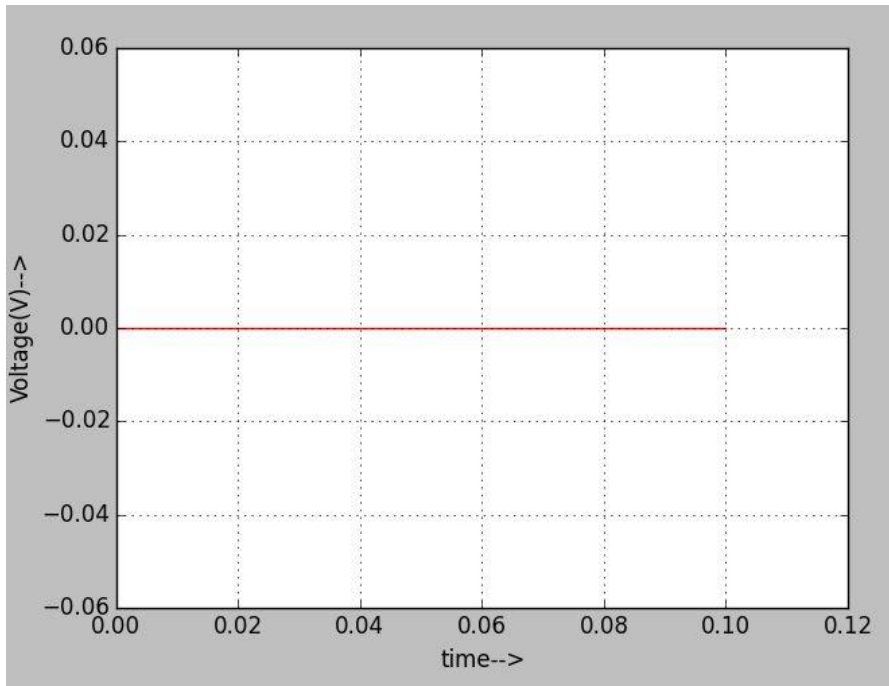
y1 (A>B)



y2 (A=B)



Y3 (A<B)



## References:-

- 1) <http://www.sycelectronica.com.ar/semiconductores/74LS85.pdf>
- 2) <https://www.youspice.com/spiceprojects/spice-simulation-projects/general-electronics-spice-simulation-projects/digital-basic-components-spice-simulation-projects/8-bit-comparator-with-two-4-bit-comparator-in-cascade/>