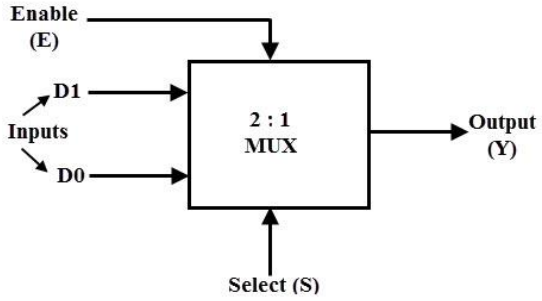
Title:- 74157 A Quad 2 line to 1 line Multiplexer

Theory :-

The multiplexer, shortened to “MUX” or “MPX”, is a combinational logic circuit designed to switch one of several input lines through to a single common output line by the application of a control signal.

A 2-to-1 multiplexer consists of two inputs D0 and D1, one select input S and one output Y. Depends on the select signal, the output is connected to either of the inputs. Since there are two input signals only two ways are possible to connect the inputs to the outputs, so one select is needed to do these operations.



E	S	Y
1	X	0
0	0	D0
0	1	D1

Function Table

Here 74157 is a quad 2 to 1 multiplexer with one select input (S) i.e. it contains four 2:1 multiplexers. Select input S is common to all the four the multiplexers.

a0,a1 are the inputs and Ya is the output to the MUX1.

b0,b1 are the inputs and Yb is the output to the MUX2.

c0,c1 are the inputs and Yc is the output to the MUX3.

d0,d1 are the inputs and Yd is the output to the MUX4.

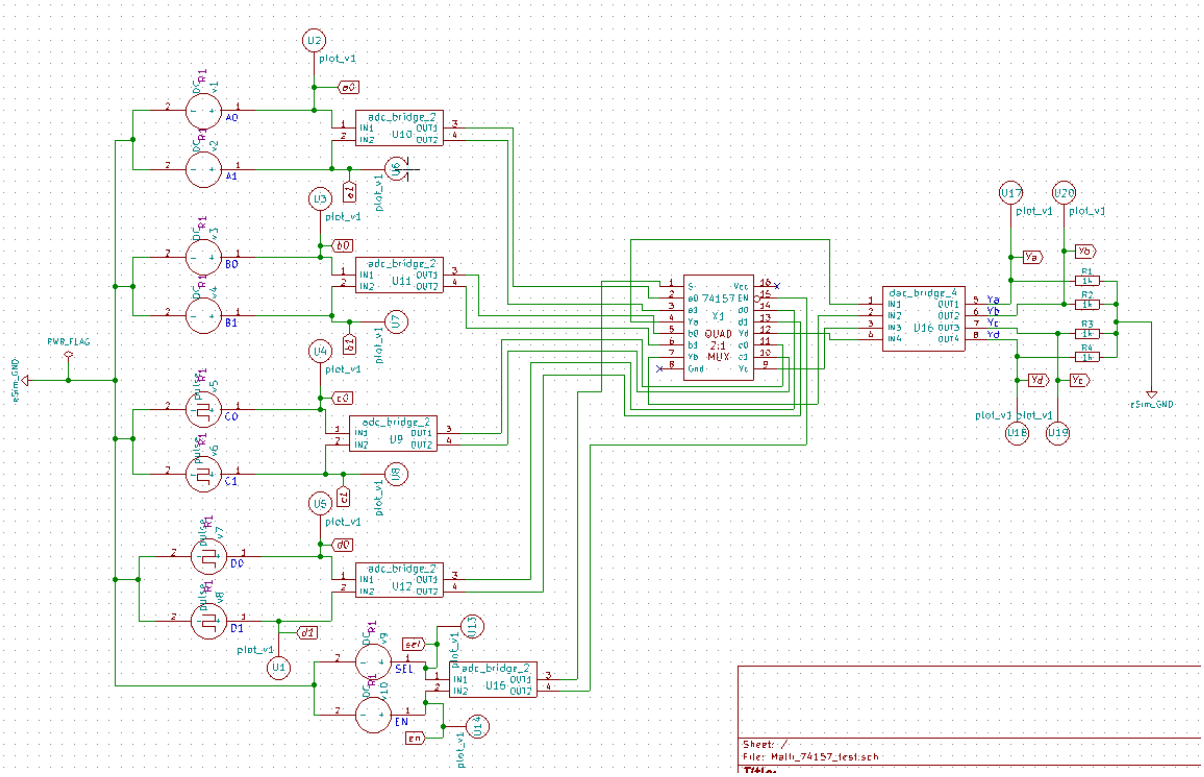
E is the active low enable input common to all the multiplexers.

Function Table of 74157:-

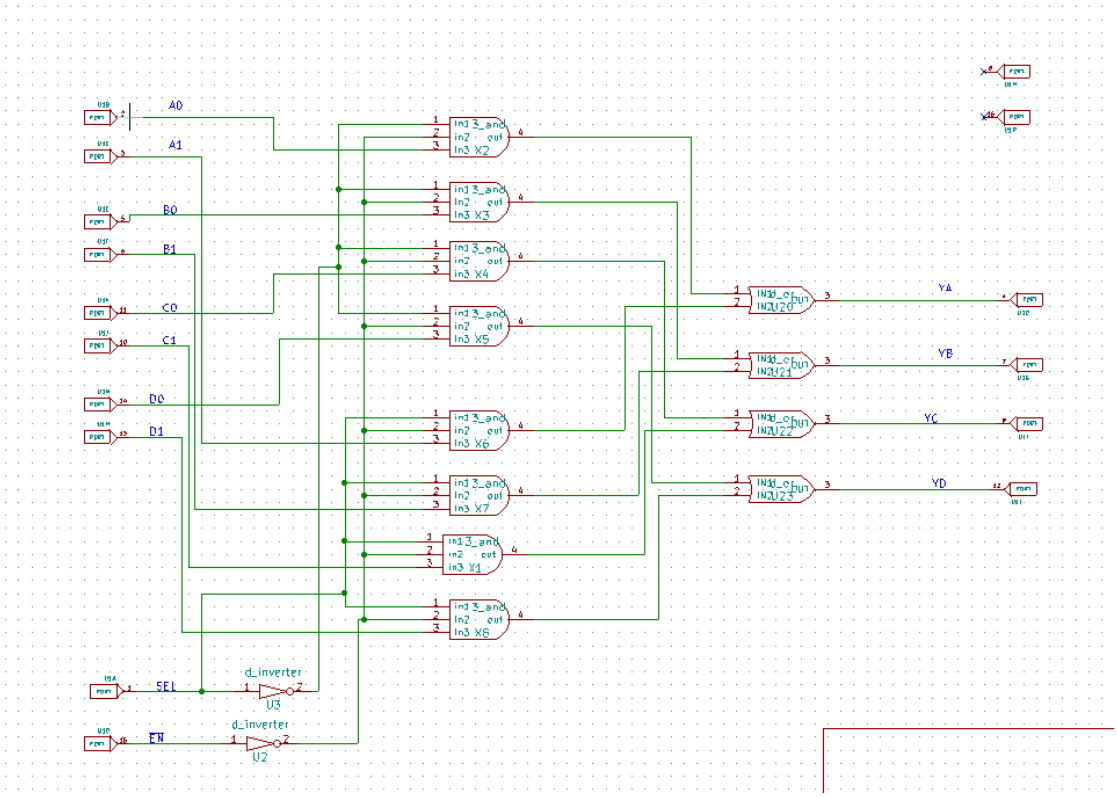
E	S	Ya	Yb	Yc	Yd
1	X	0	0	0	0
0	0	a0	b0	c0	d0
0	1	a1	b1	c1	d1

NOTE :- Here in E-SIM software, no need to connect Vcc(pin 16) and GND (pin 8) pins to Dc source and gnd respectively , you can leave them unconnected using NO CONNECT symbol . This is because in circuit simulation softwares , we use BASIC GATES (AND, NAND etc.) they don’t need Vcc and GND. As in manufacturing an IC , they use MOSFETs to implement those GATES ,there MOSFETs require Vcc and Gnd

Schematic Diagram :-



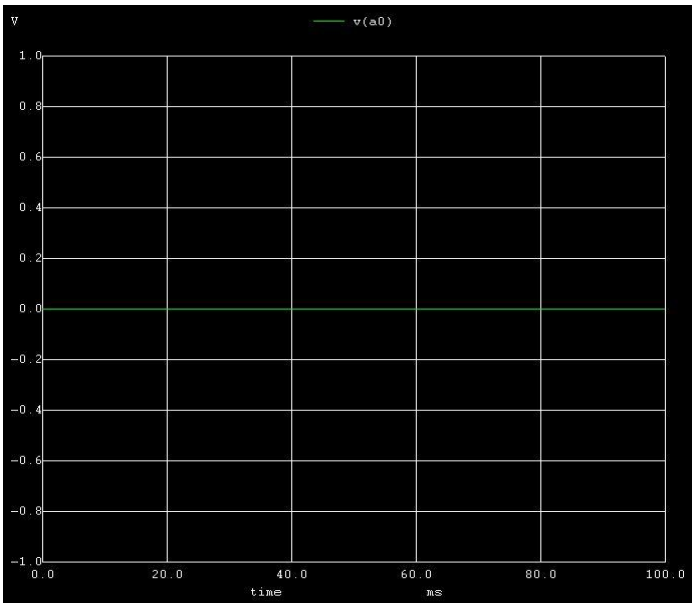
Subcircuit Schematic for 74157 :-



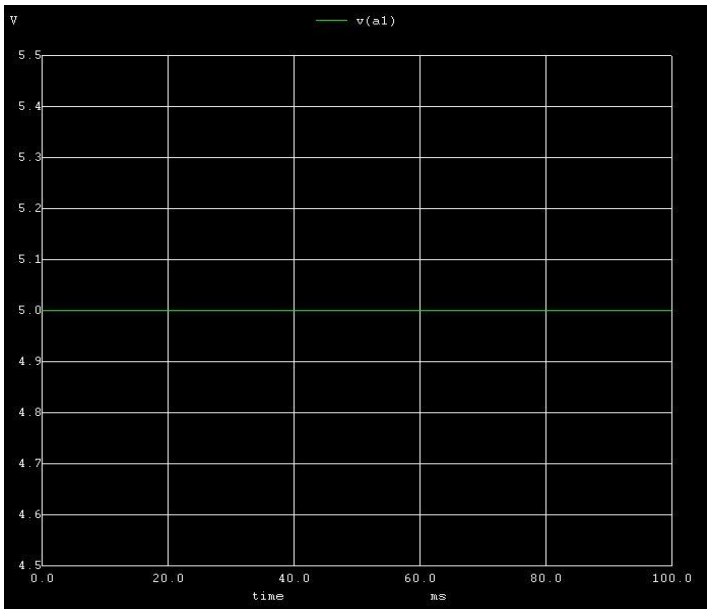
Simulation Results :- Ngspice plots

Inputs to MUX 1

a0(v1)

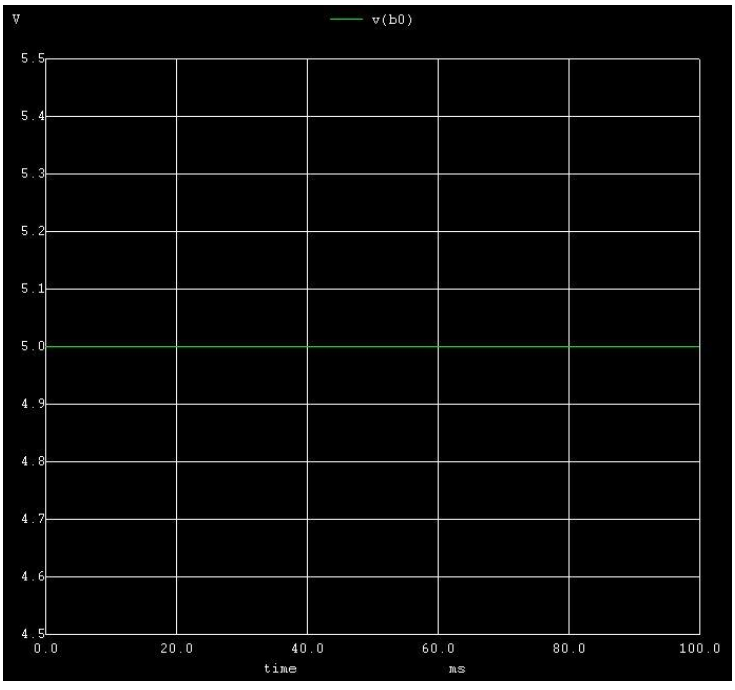


a1(v2)

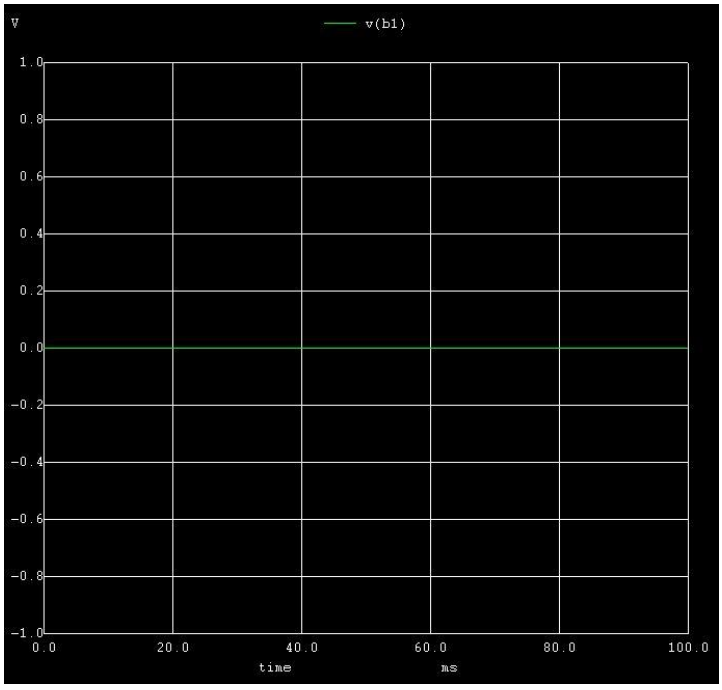


Inputs to MUX 2

b0(v3)

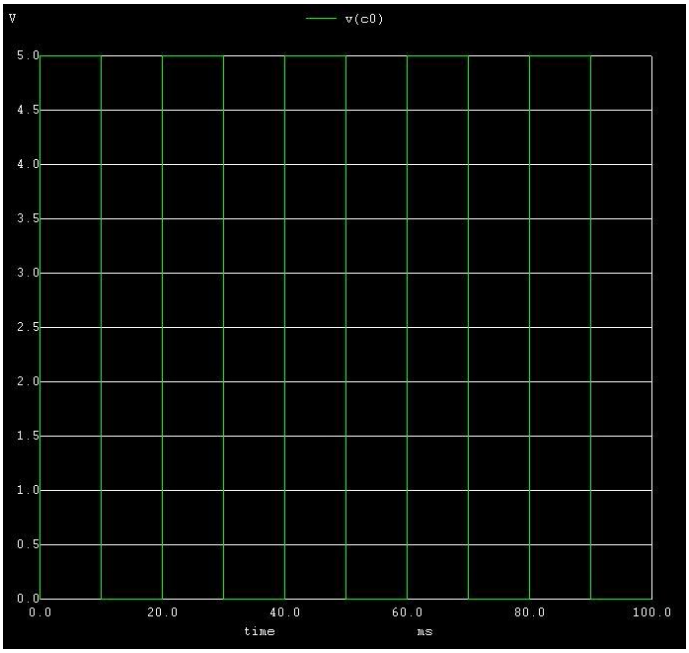


b1(v4)

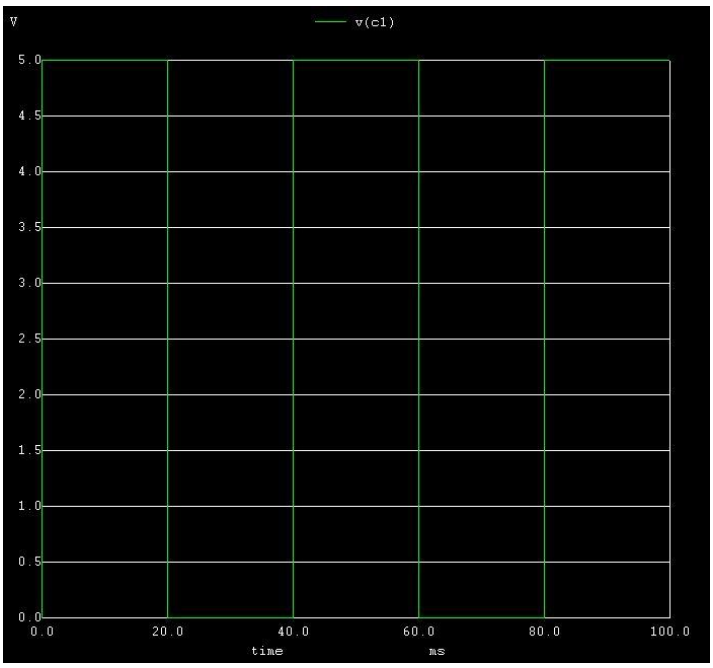


Inputs to MUX 3

c0(v5)

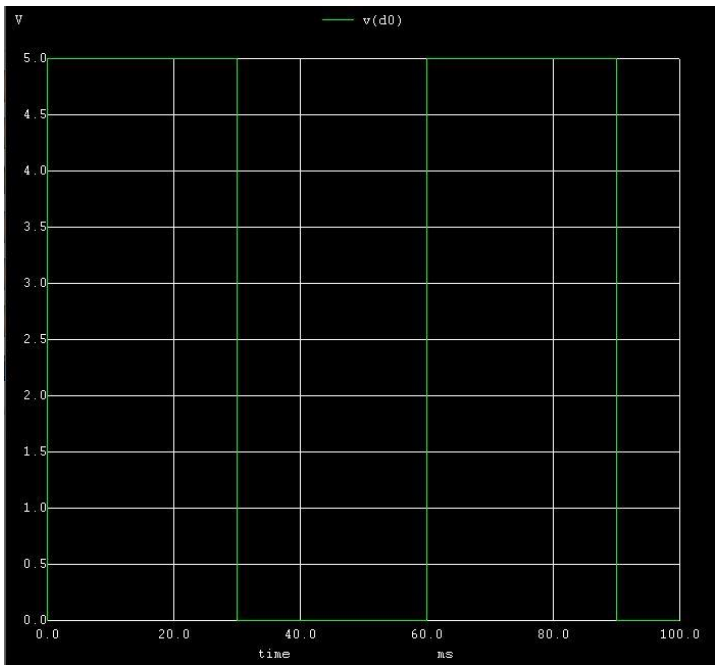


c1(v6)

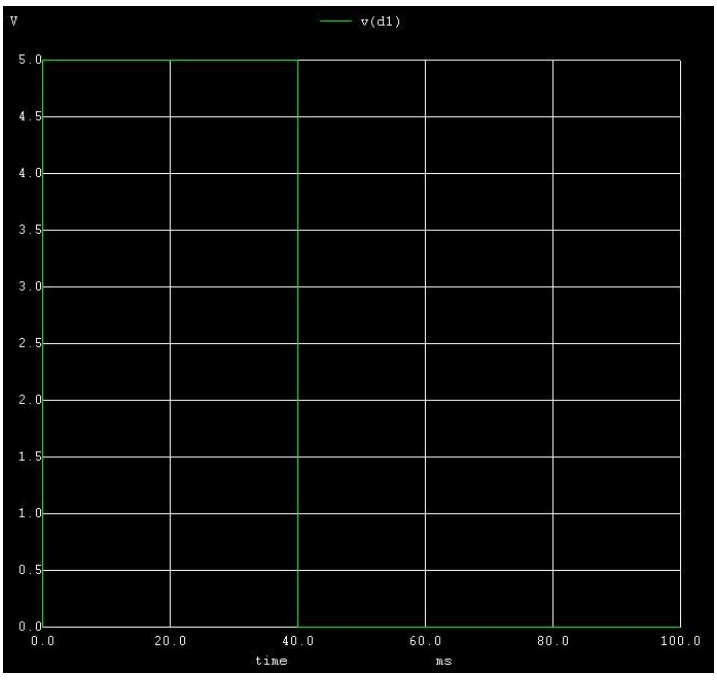


Inputs to MUX 4

d0(v7)

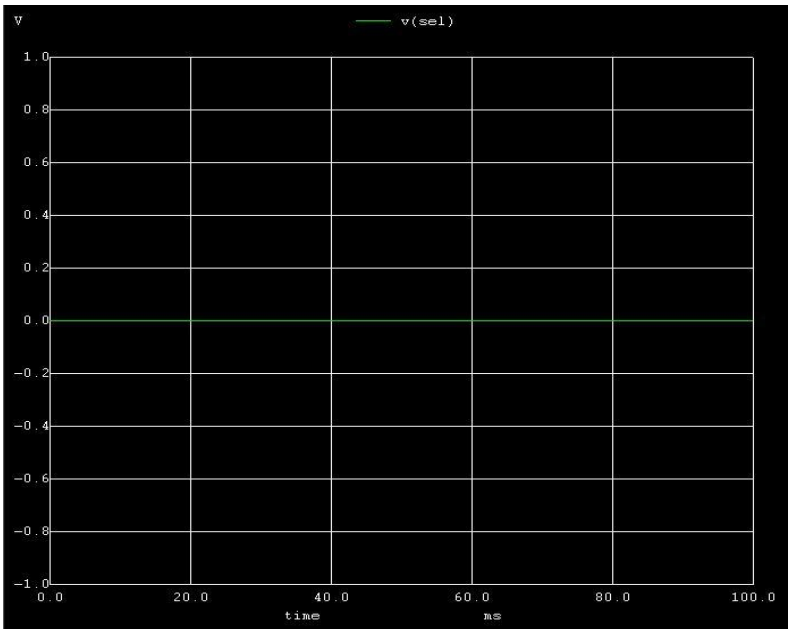


d1(v8)

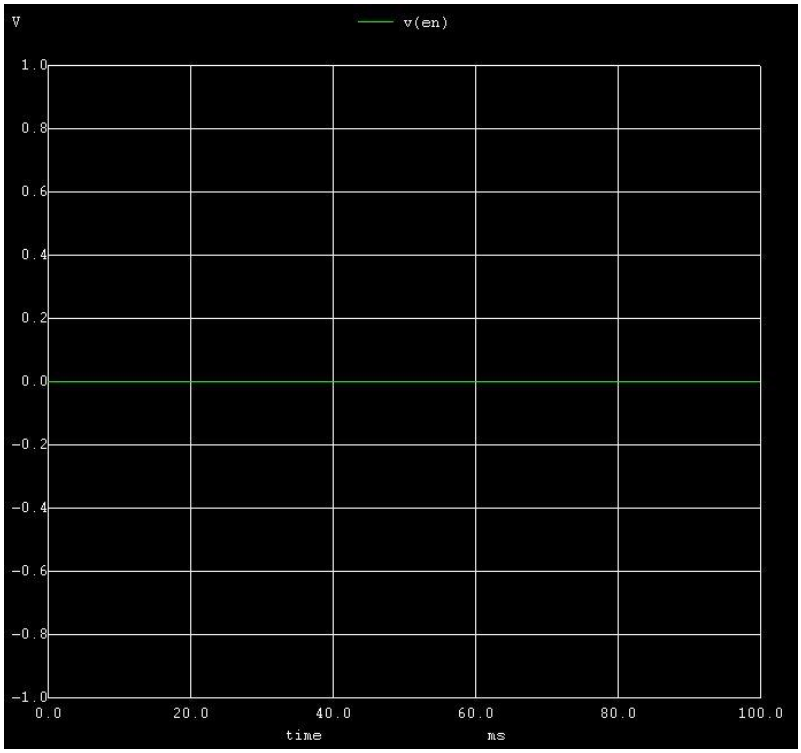


OUTPUT when SEL(S)=’0’ EN=’0

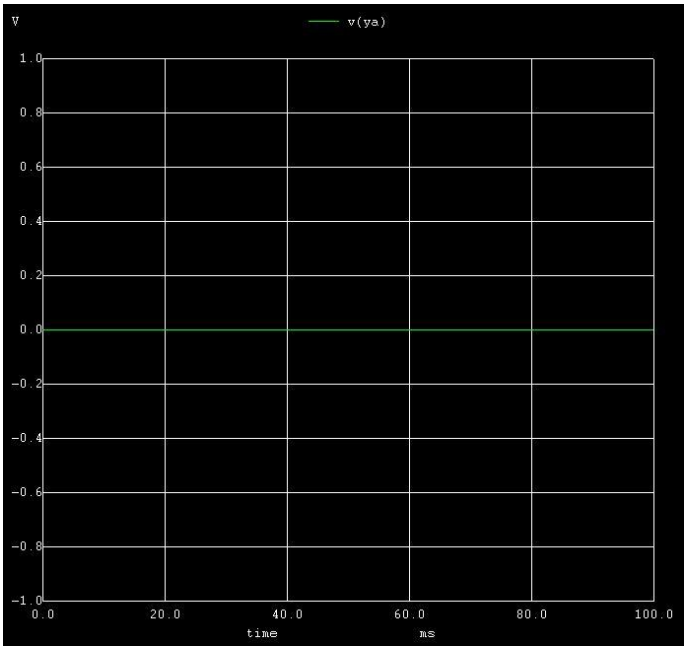
SEL S (V9=0v)



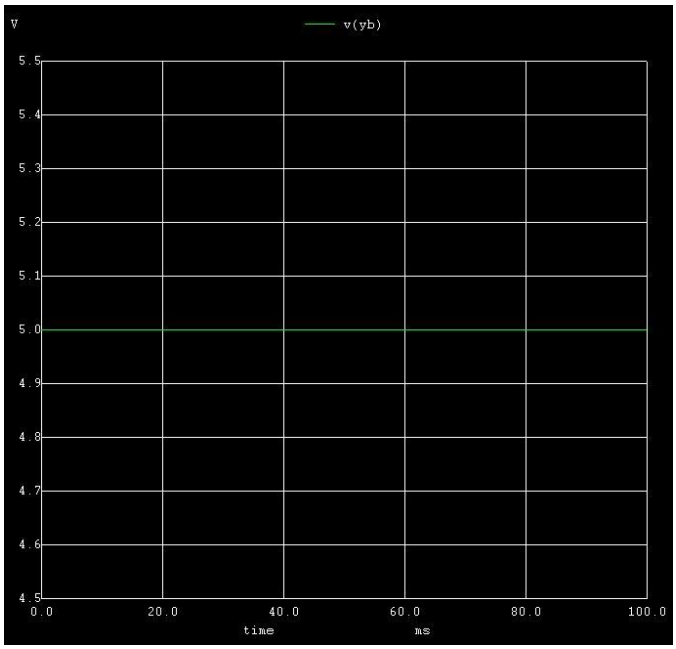
EN(v10 = 0v)



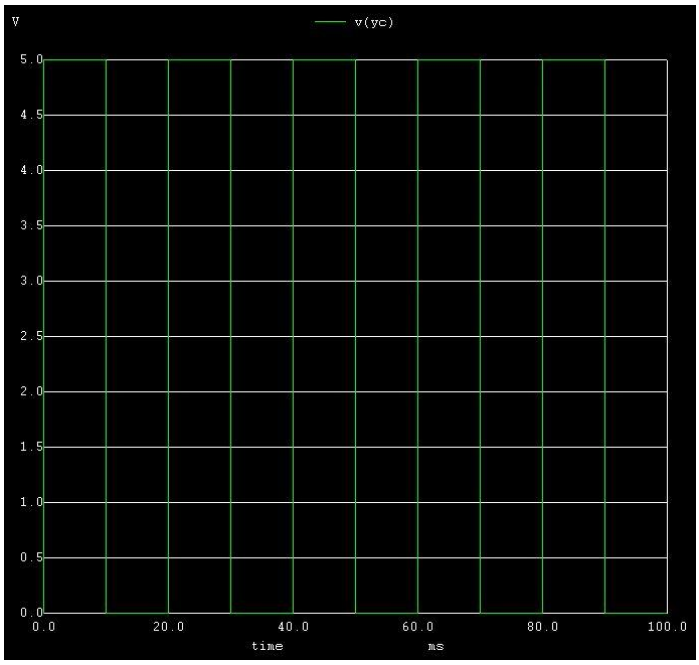
Ya


V
v(ya)
1.0
0.8
0.6
0.4
0.2
0.0
-0.2
-0.4
-0.6
-0.8
-1.0
0.0
20.0
40.0
60.0
80.0
100.0
time
ms

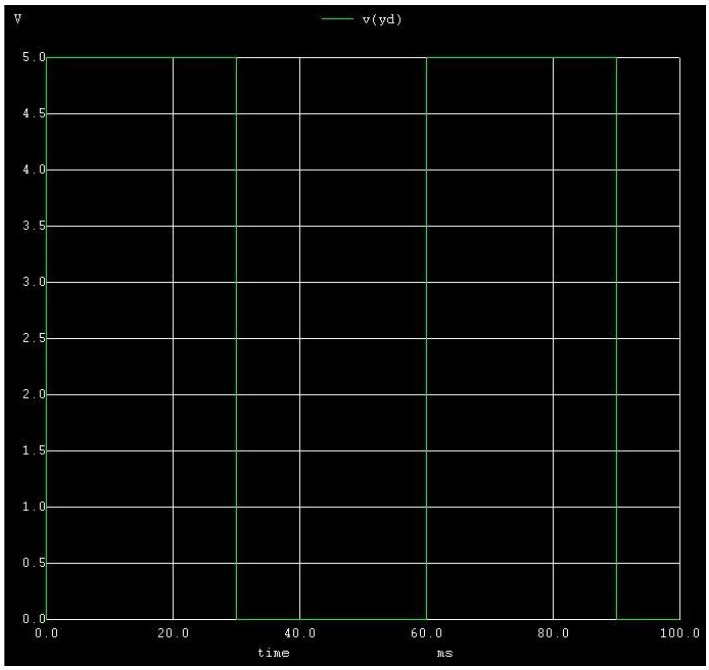
Yb


V
v(yb)
5.5
5.4
5.3
5.2
5.1
5.0
4.9
4.8
4.7
4.6
4.5
0.0
20.0
40.0
60.0
80.0
100.0
time
ms

Yc

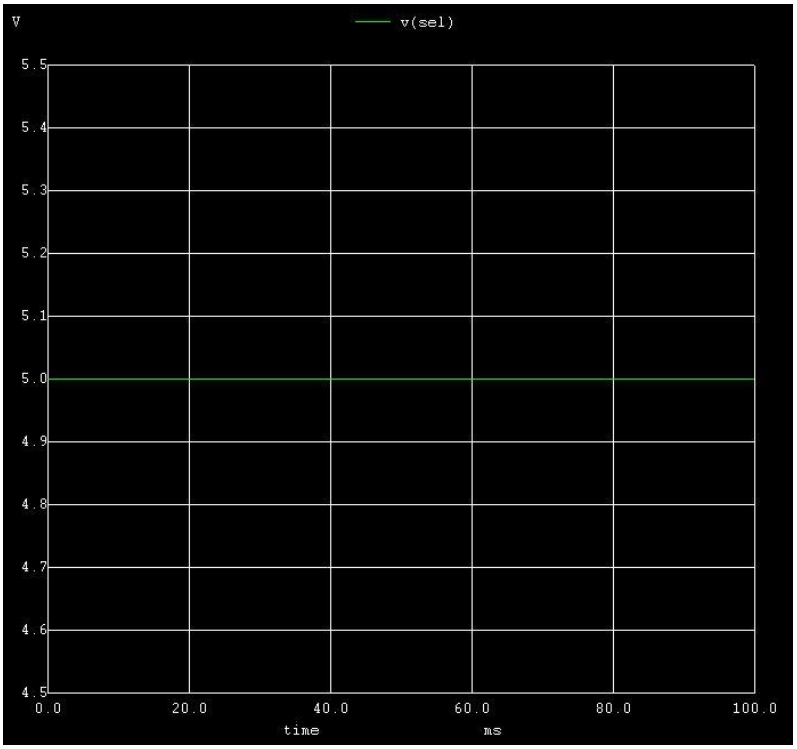

V
v(yc)
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0.0
20.0
40.0
60.0
80.0
100.0
time
ms

Yd

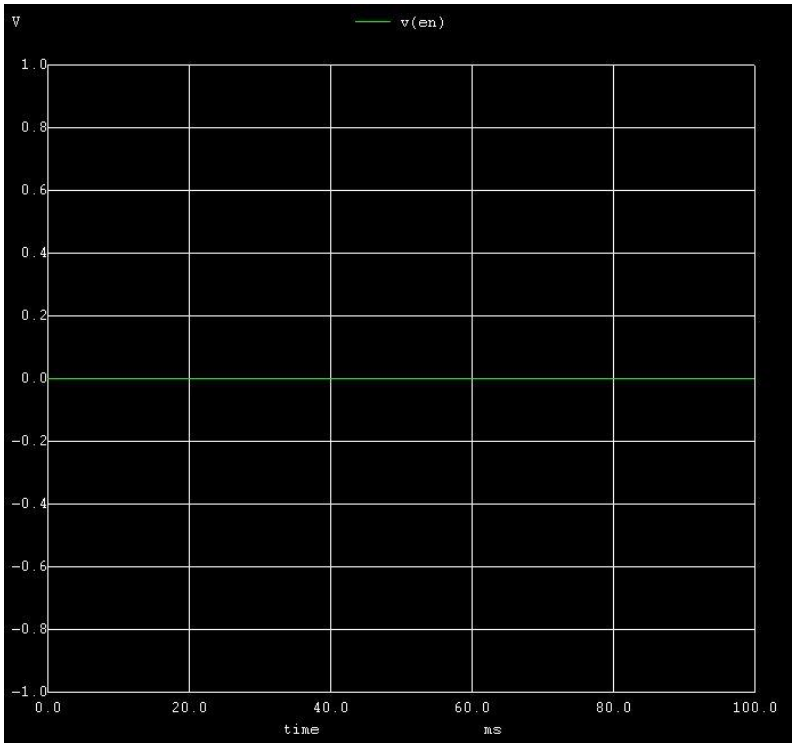

V
v(yd)
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0.0
20.0
40.0
60.0
80.0
100.0
time
ms

OUTPUT when SEL(S)=’1’ EN=’0’

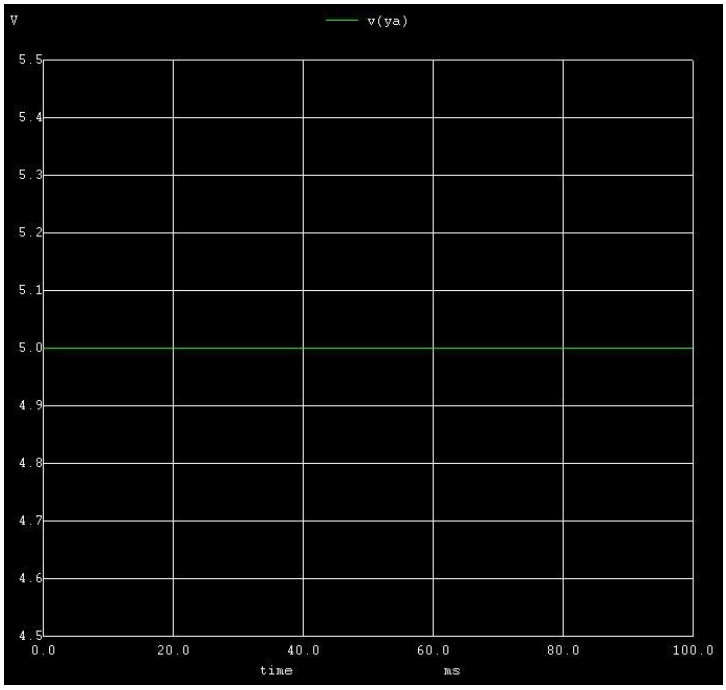
SEL S (V9=5v)



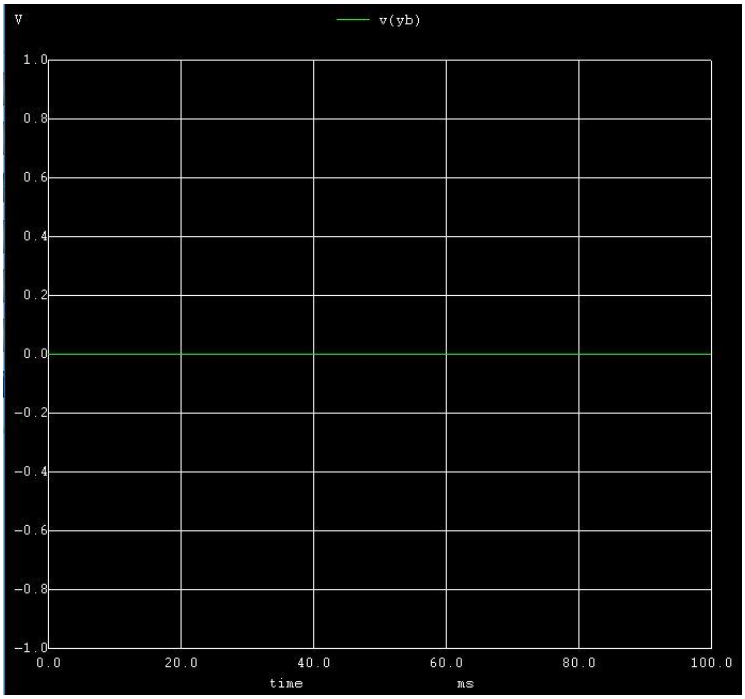
EN(v10 = 0v)



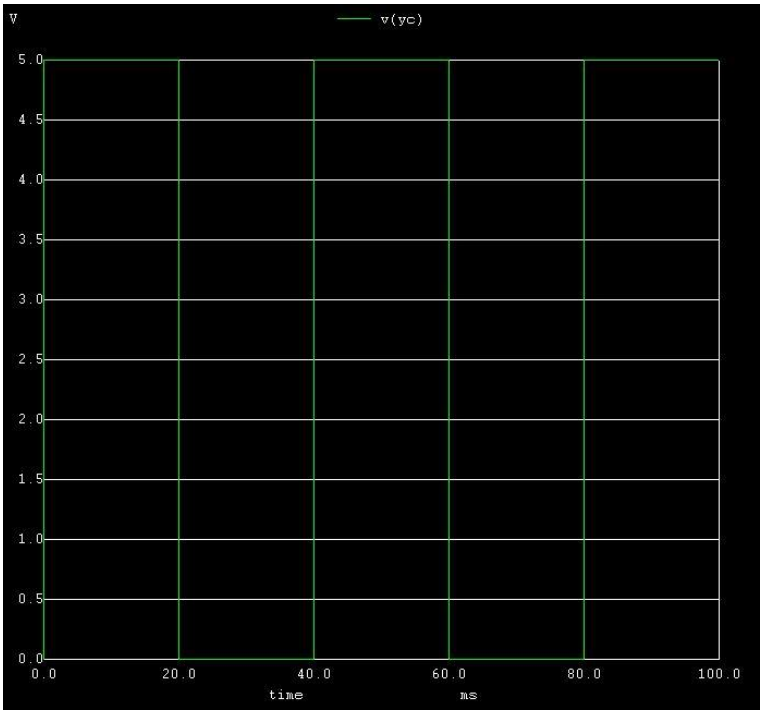
Ya


V
v(ya)
5.5
5.4
5.3
5.2
5.1
5.0
4.9
4.8
4.7
4.6
4.5
0.0
20.0
40.0
60.0
80.0
100.0
time
ms

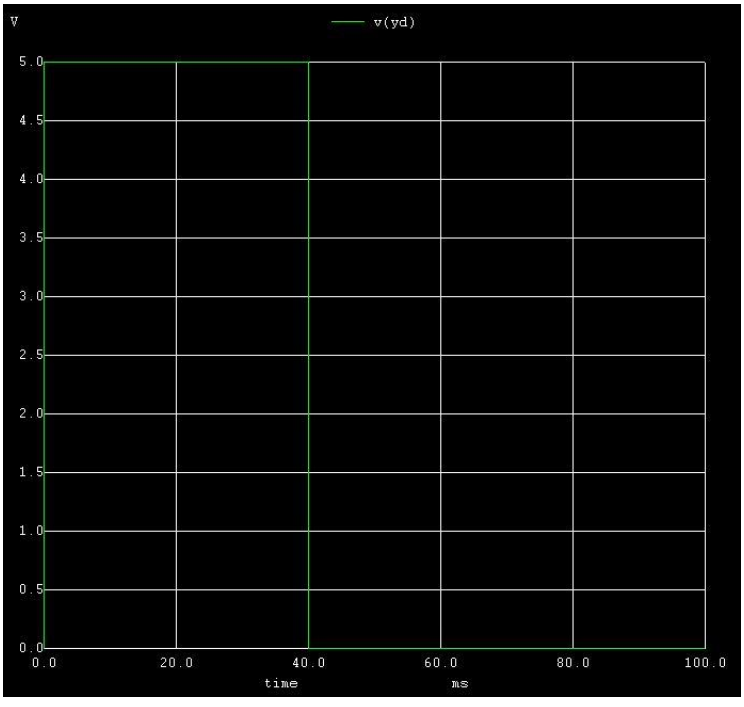
Yb


V
v(yb)
1.0
0.8
0.6
0.4
0.2
0.0
-0.2
-0.4
-0.6
-0.8
-1.0
0.0
20.0
40.0
60.0
80.0
100.0
time
ms

Yc


V
v(yc)
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0.0
20.0
40.0
60.0
80.0
100.0
time
ms

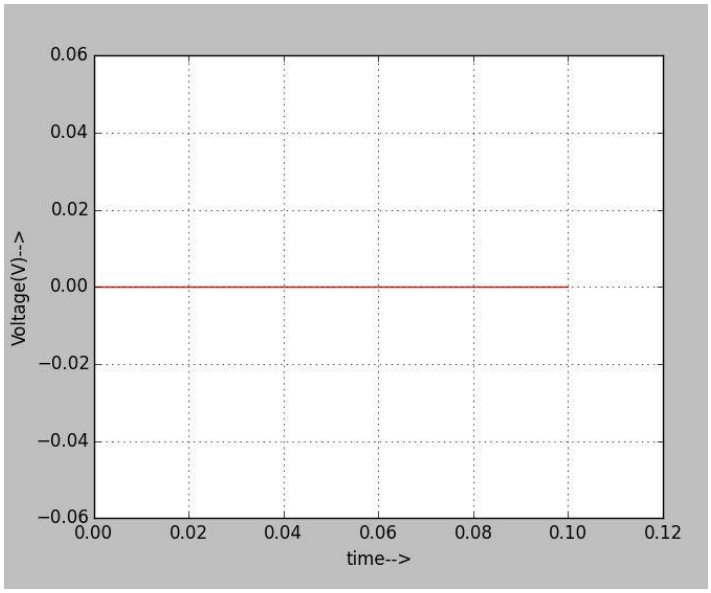
Yd


V
v(yd)
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0.0
20.0
40.0
60.0
80.0
100.0
time
ms

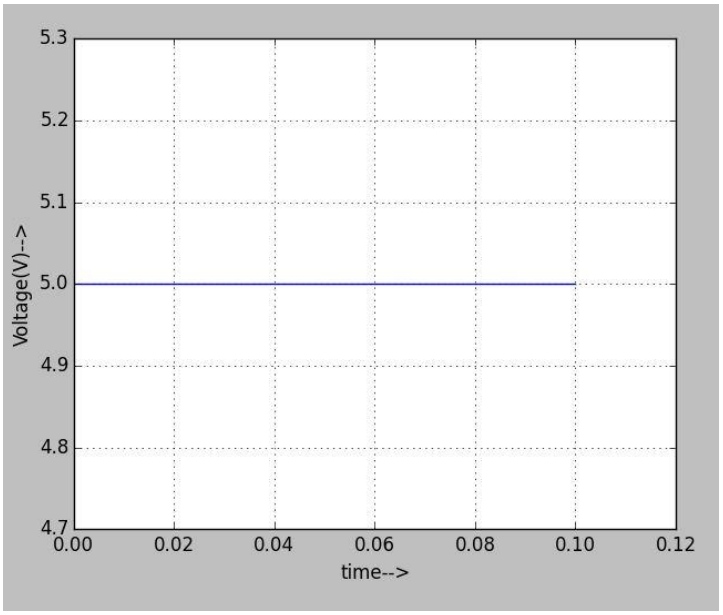
PYTHON PLOTS

Inputs to MUX 1

a0(v1)

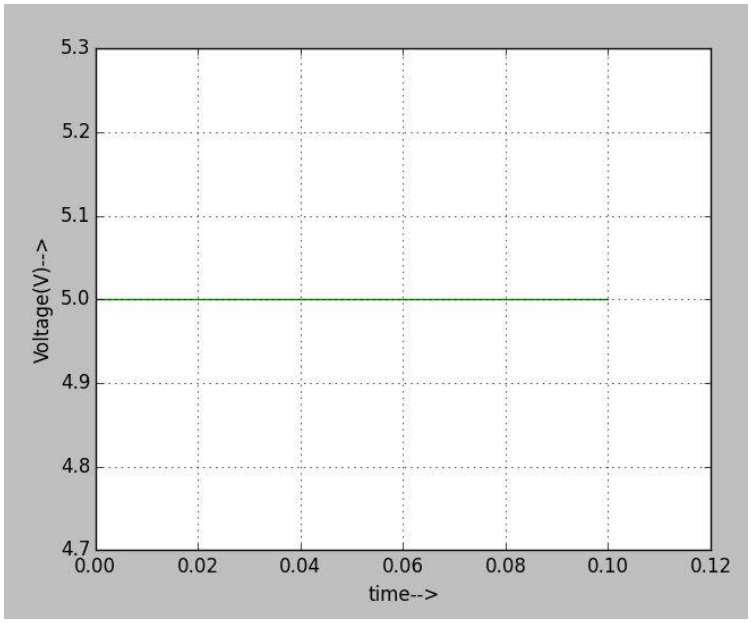


a1(v2)

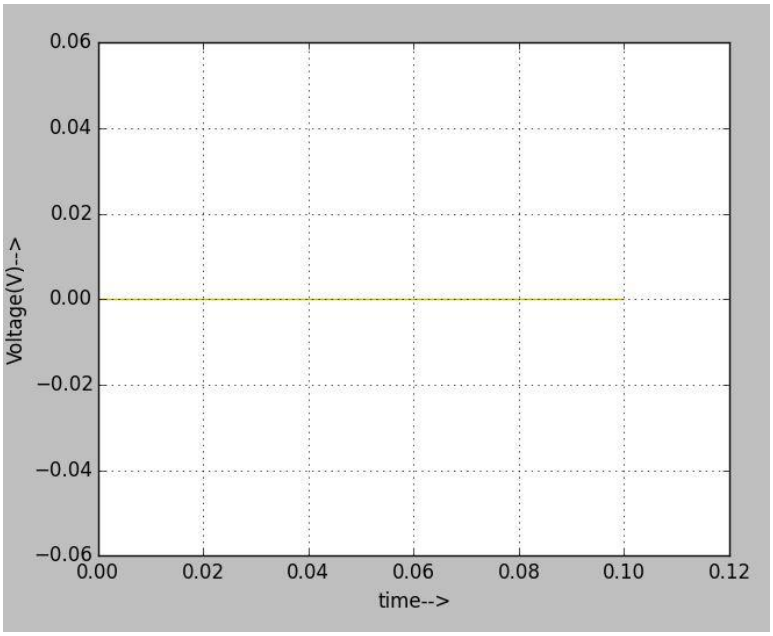


Inputs to MUX 2

b0(v3)

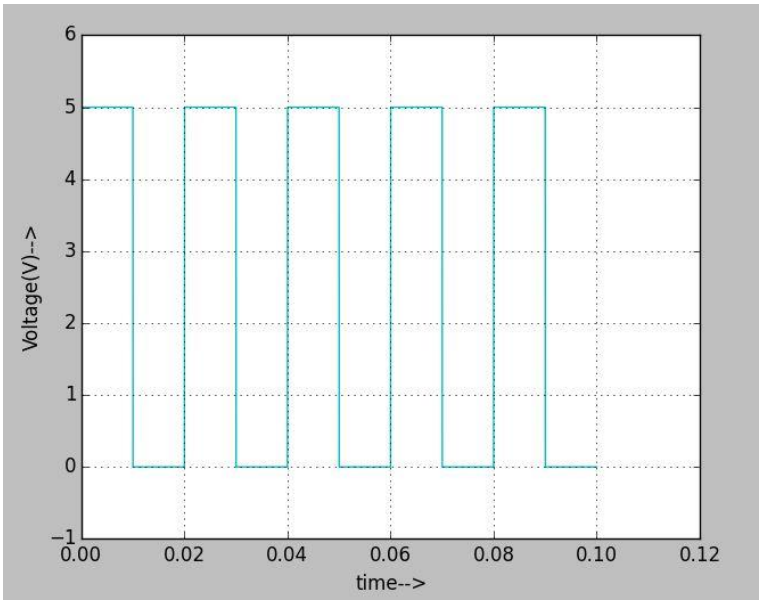


b1(v4)

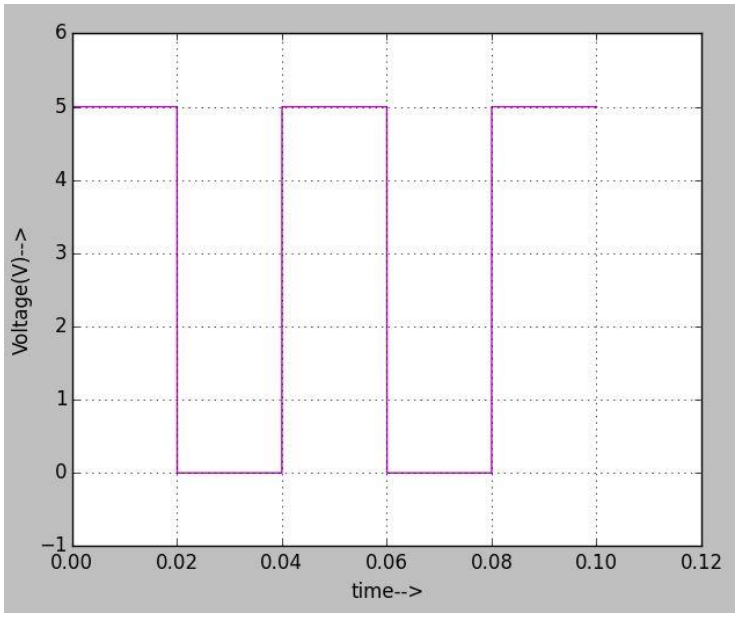


Inputs to MUX 3

c0(v5)

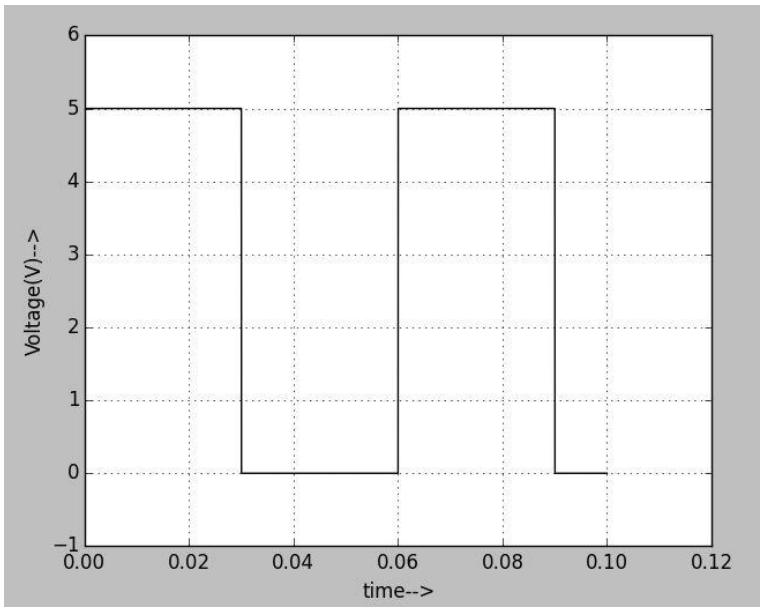


c1(v6)

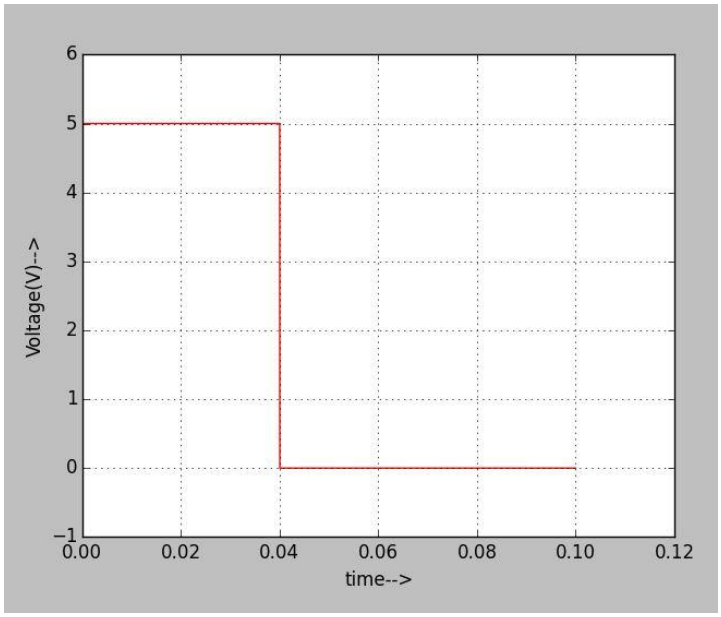


Inputs to MUX 4

d0(v7)

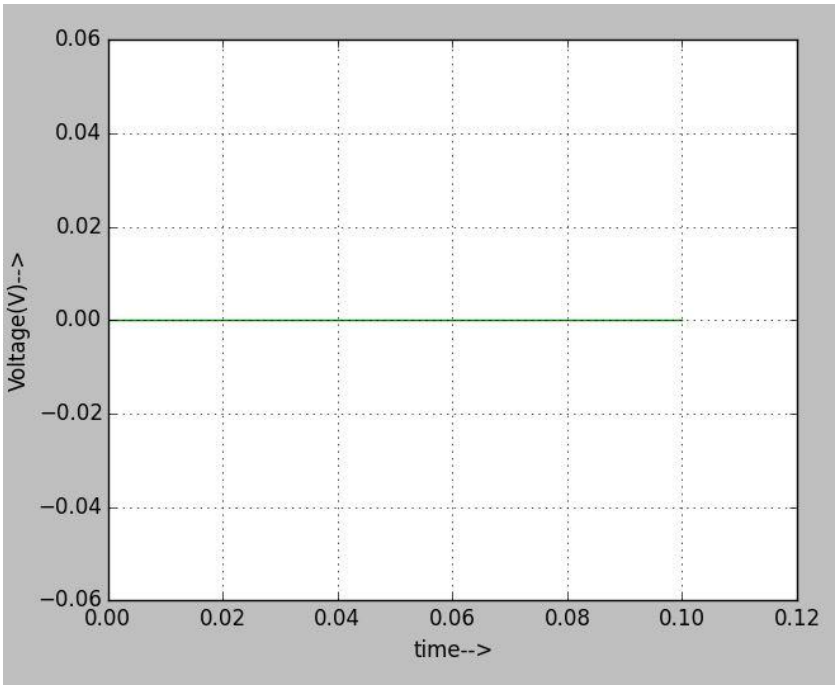


d1(v8)

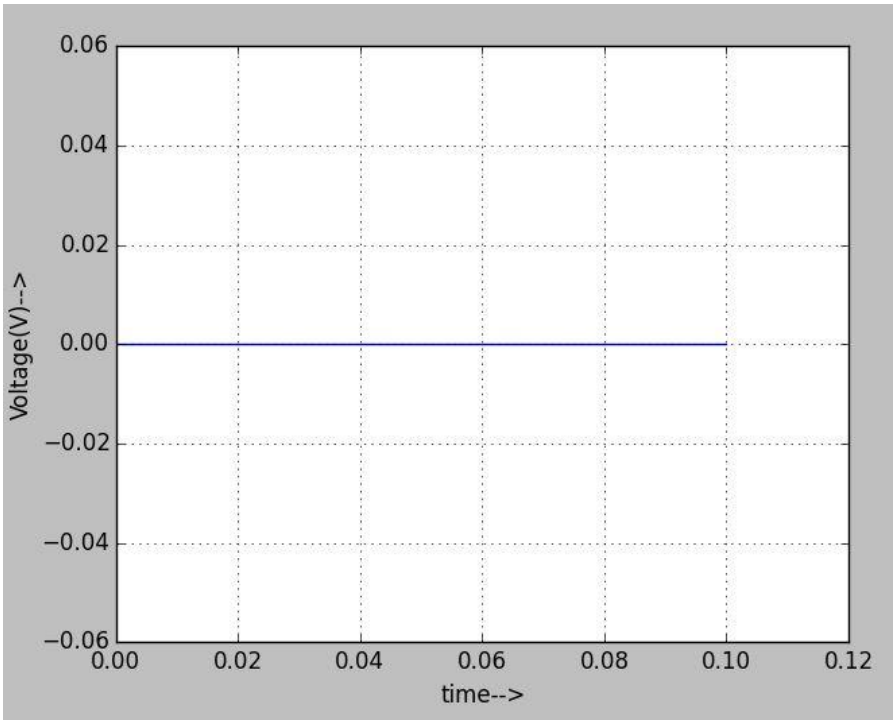


OUTPUT when SEL(S)=’0’ EN=’0’

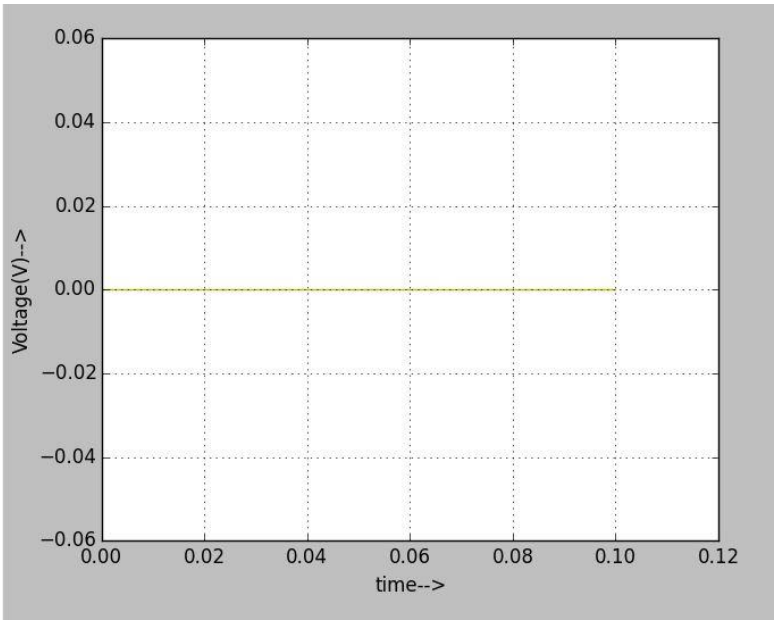
SEL S (V9=0v)



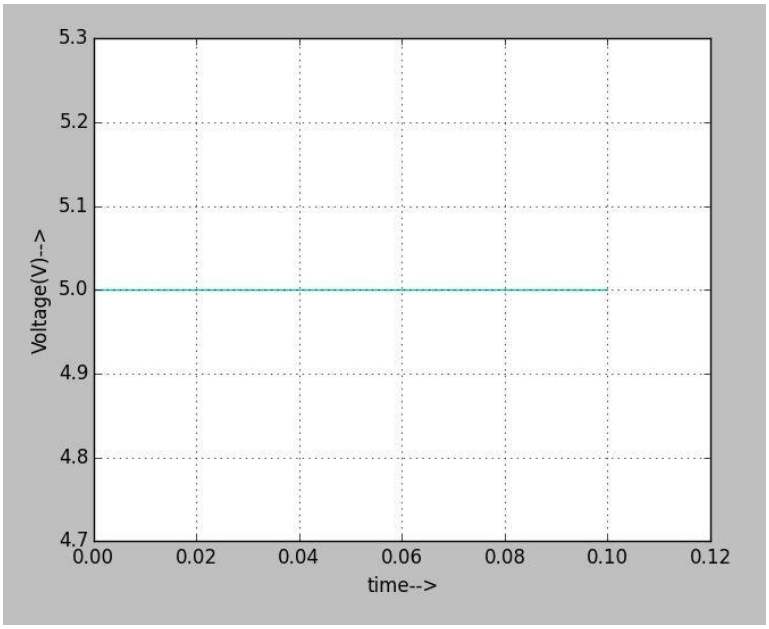
EN(v10 = 0v)



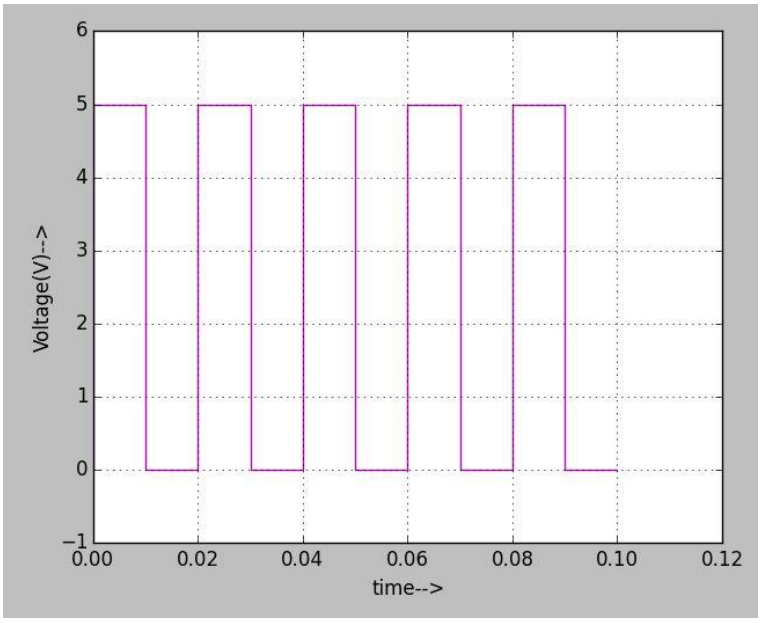
Ya


0.06
0.04
0.02
0.00
−0.02
−0.04
−0.06
Voltage(V)-->
0.00
0.02
0.04
0.06
0.08
0.10
0.12
time-->

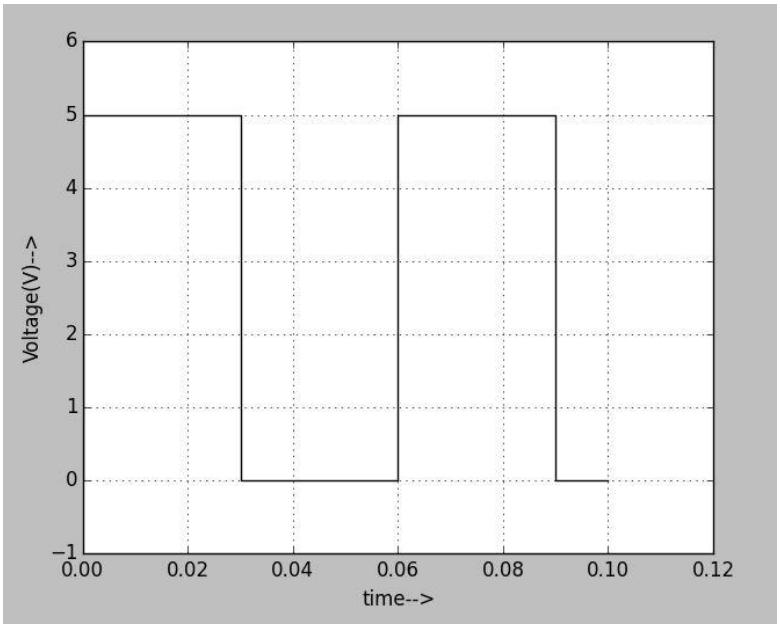
Yb


5.3
5.2
5.1
5.0
4.9
4.8
4.7
Voltage(V)-->
0.00
0.02
0.04
0.06
0.08
0.10
0.12
time-->

Yc

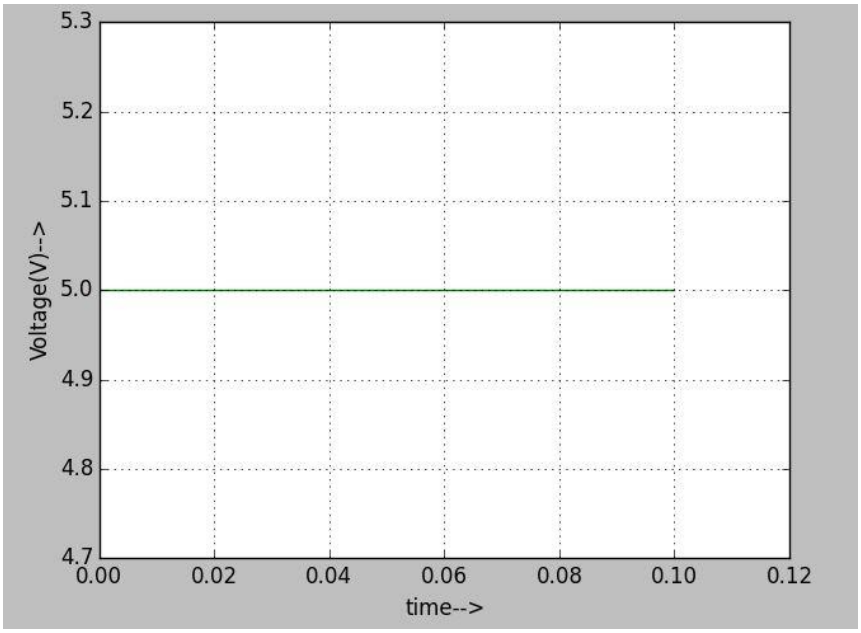

6
5
4
3
2
1
0
−1
Voltage(V)-->
0.00
0.02
0.04
0.06
0.08
0.10
0.12
time-->

Yd

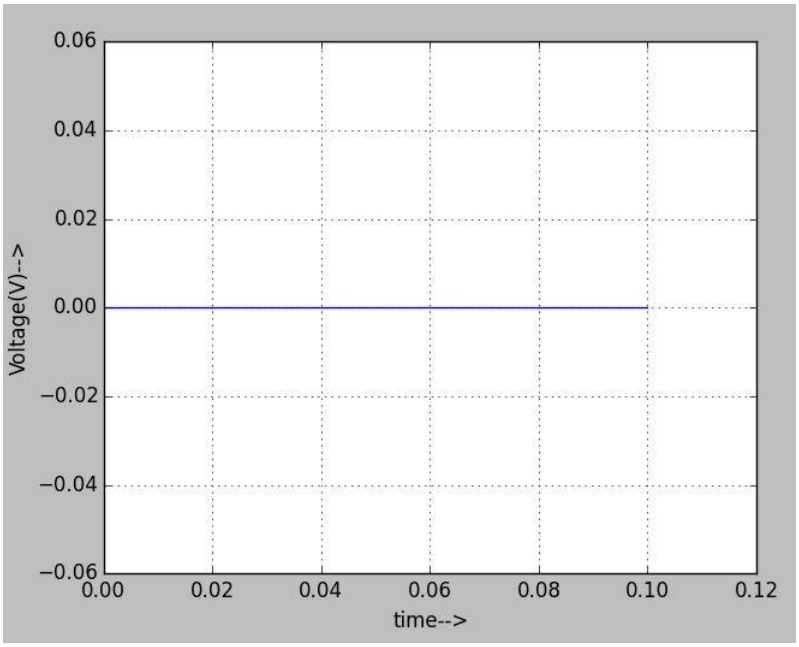

6
5
4
3
2
1
0
−1
Voltage(V)-->
0.00
0.02
0.04
0.06
0.08
0.10
0.12
time-->

OUTPUT when SEL(S)=’1’ EN=’0’

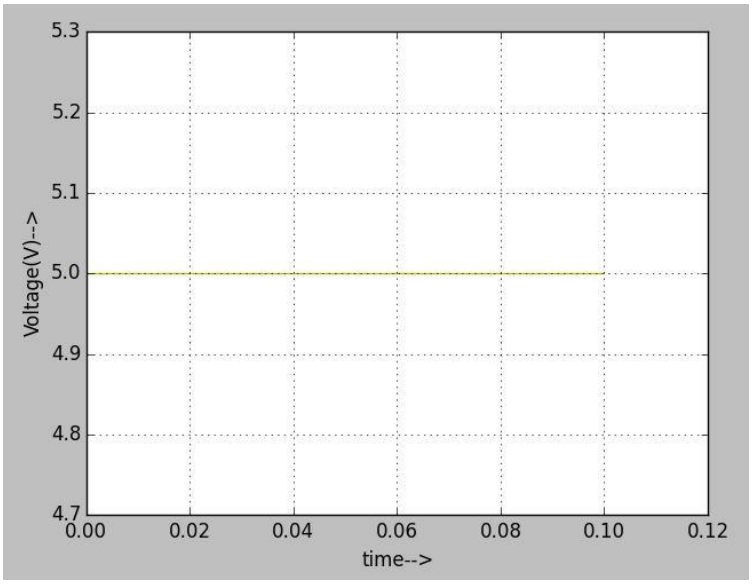
SEL S (V9=0v)



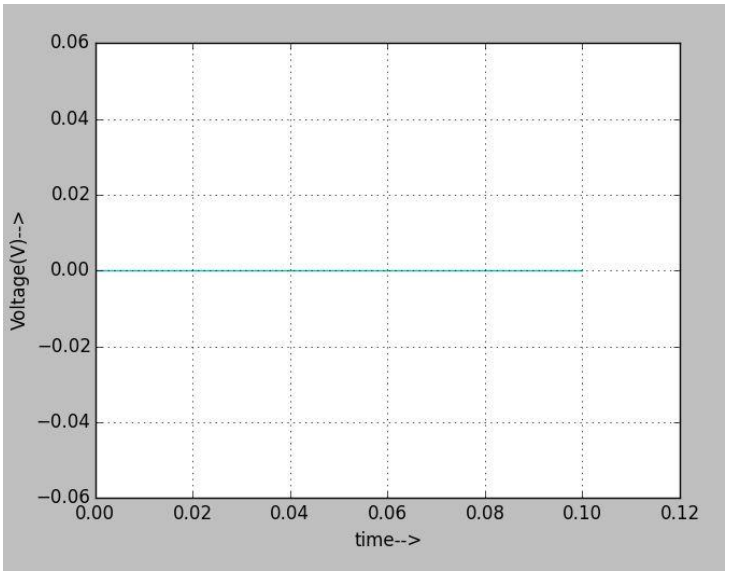
EN(v10 = 0v)



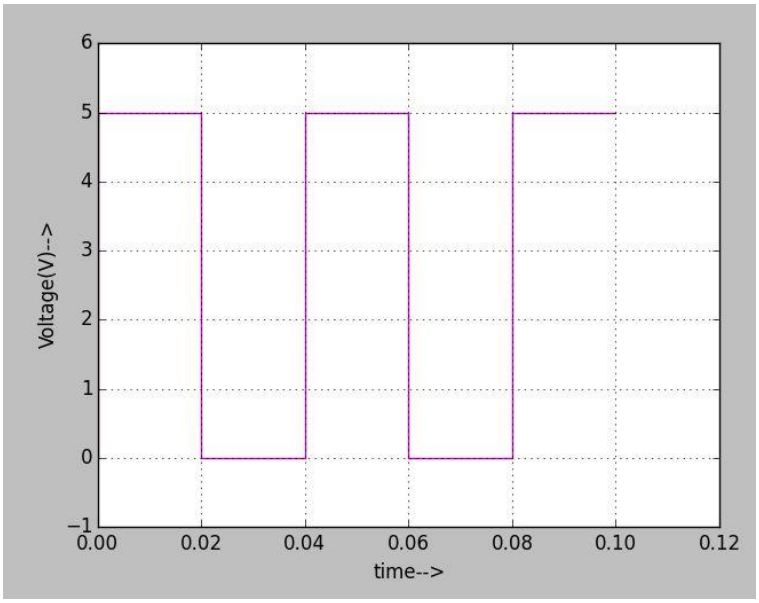
Ya


5.3
5.2
5.1
5.0
4.9
4.8
4.7
Voltage(V)-->
0.00
0.02
0.04
0.06
0.08
0.10
0.12
time-->

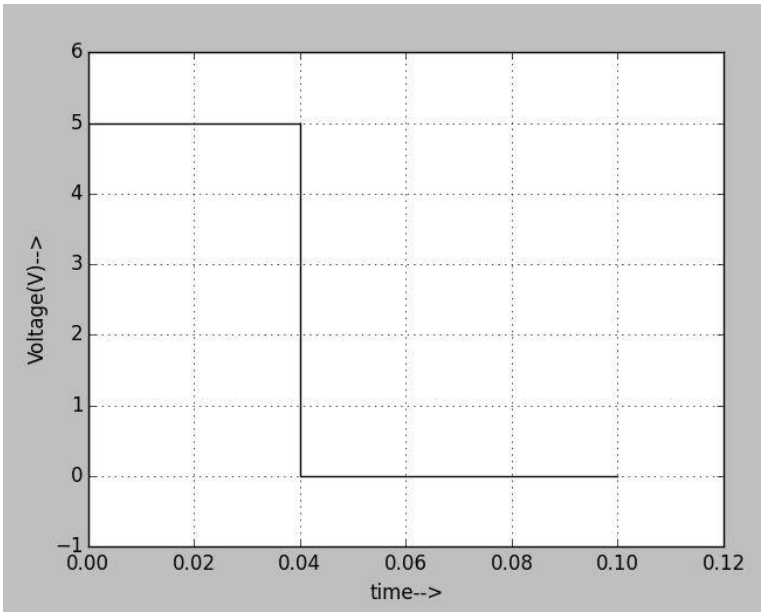
Yb


0.06
0.04
0.02
0.00
−0.02
−0.04
−0.06
Voltage(V)-->
0.00
0.02
0.04
0.06
0.08
0.10
0.12
time-->

Yc


6
5
4
3
2
1
0
−1
Voltage(V)-->
0.00
0.02
0.04
0.06
0.08
0.10
0.12
time-->

Yd


6
5
4
3
2
1
0
−1
Voltage(V)-->
0.00
0.02
0.04
0.06
0.08
0.10
0.12
time-->

REFERENCES:-

1) https://www.electronicshub.org/multiplexerandmultiplexing/