Title :- 4 BIT BINARY FULL ADDER

Theory:-

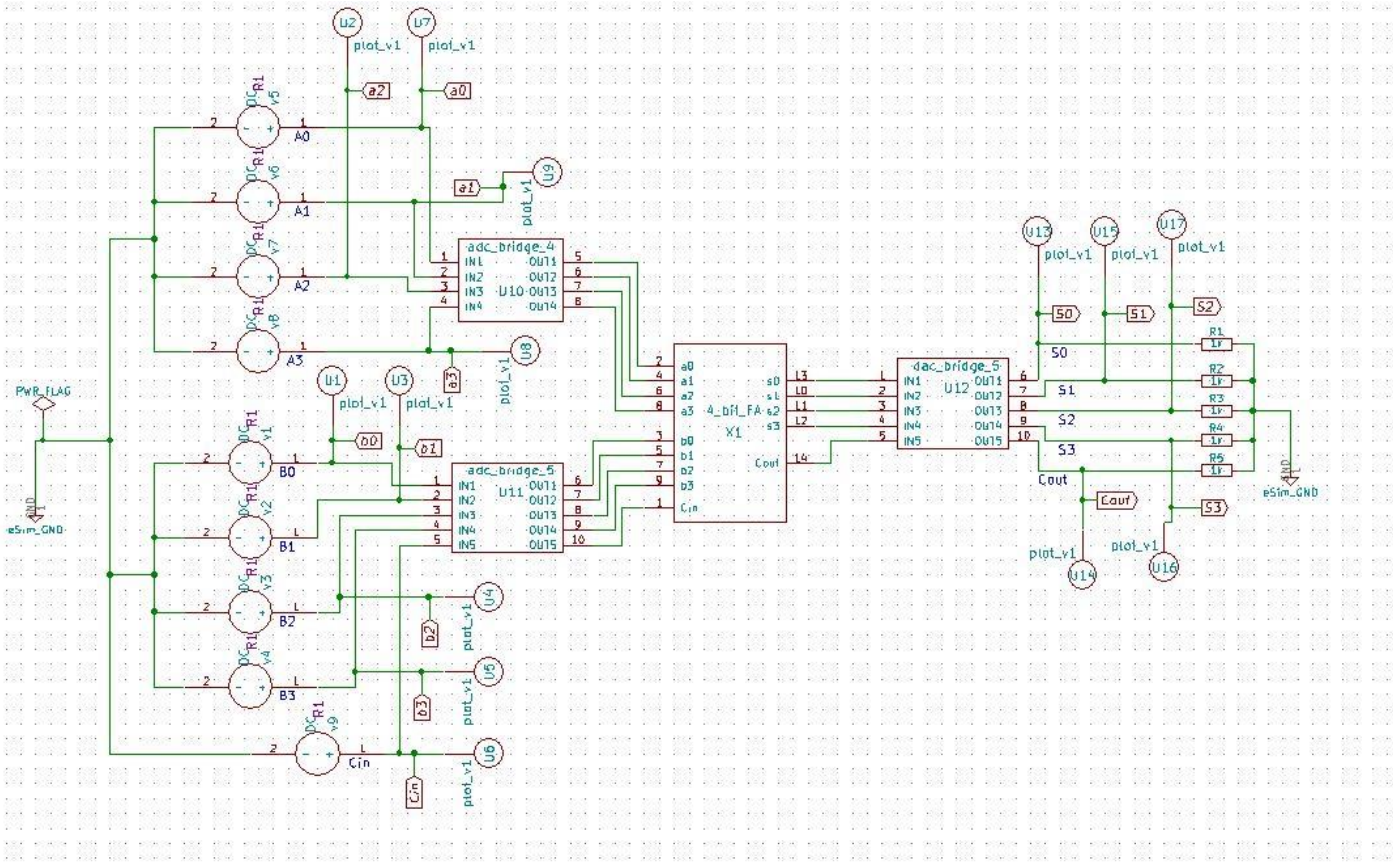
These full adders perform the addition of two 4-bit binary numbers.

The sum S outputs are provided for each bit and the resultant carry (Cout) is obtained from the fourth bit.

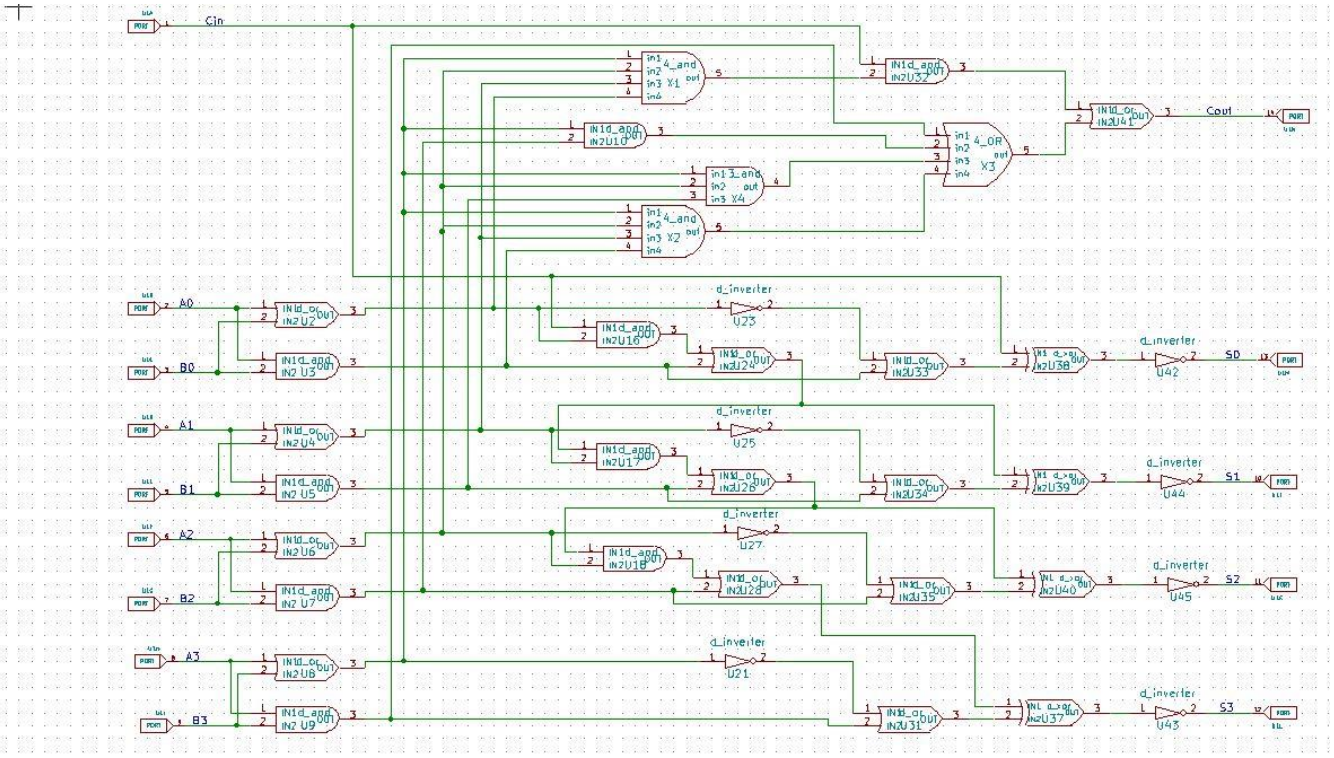
But these adderscontain one special block for the carry bit which feature full internal look ahead across all four bits. This provides the system designer with partial lookahead performance at the economy and reduced package count of a ripple-carry implementation. The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

Here a0,a1,a2,a3 and b0,b1,b2,b3 are the 4 bit binary numbers to be added. Cin is the input carry bit. s0,s1,s2,s3 are the result bits and Cout is the output carry bit.

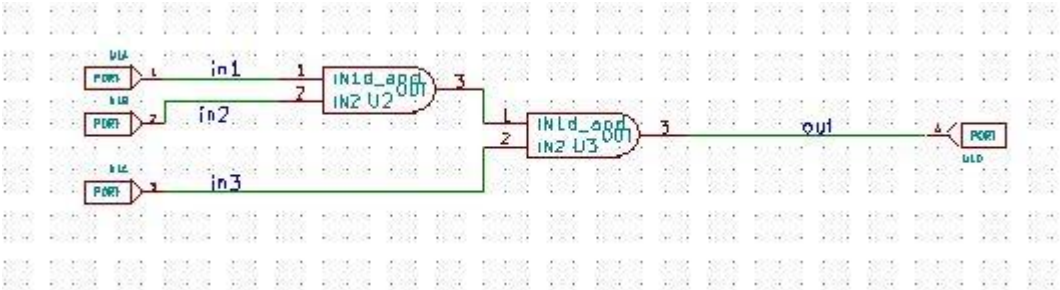
Schematic Diagram:-



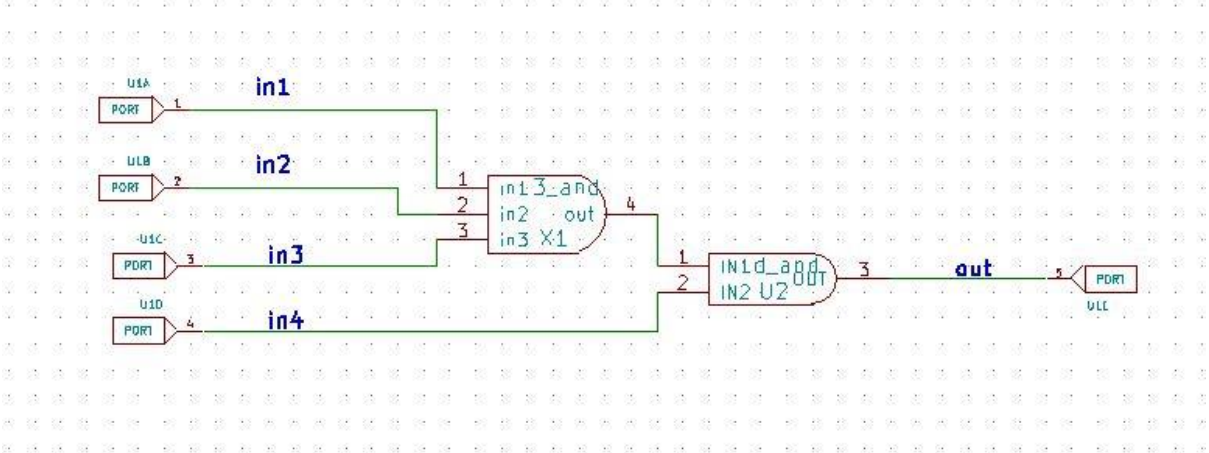
Subcircuit schematic for 4_bit_FA block:-



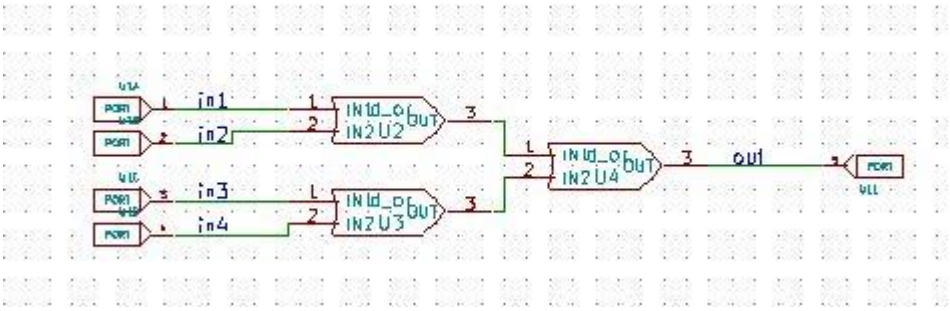
Subcircuit schematic for “3_and” gate :-



Subcircuit schematic for “4_and “ gate :-



Subcircuit Schematic for “4_OR” gate :-

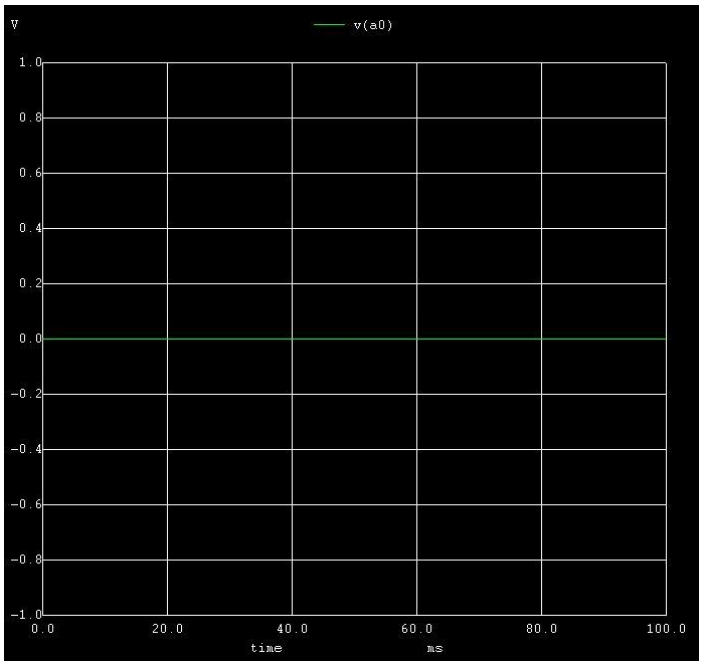


Simulation Results:-

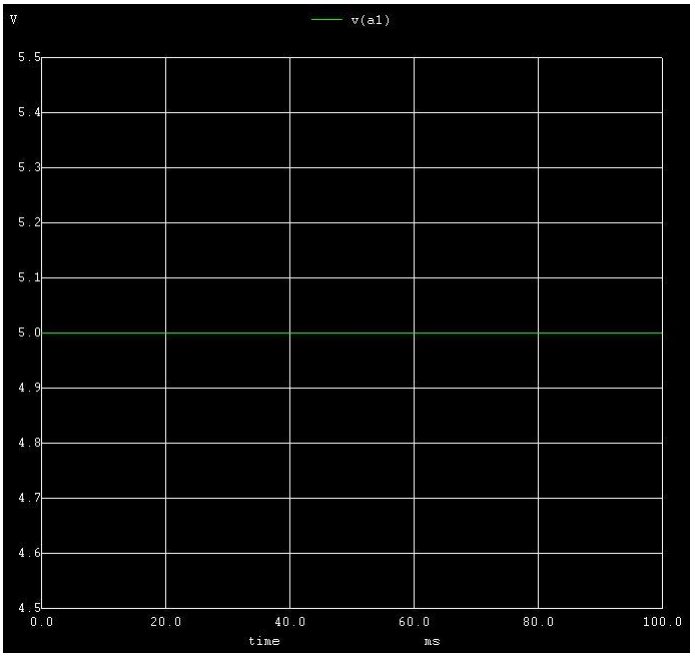
NGSPICE PLOTS:-

Input:-

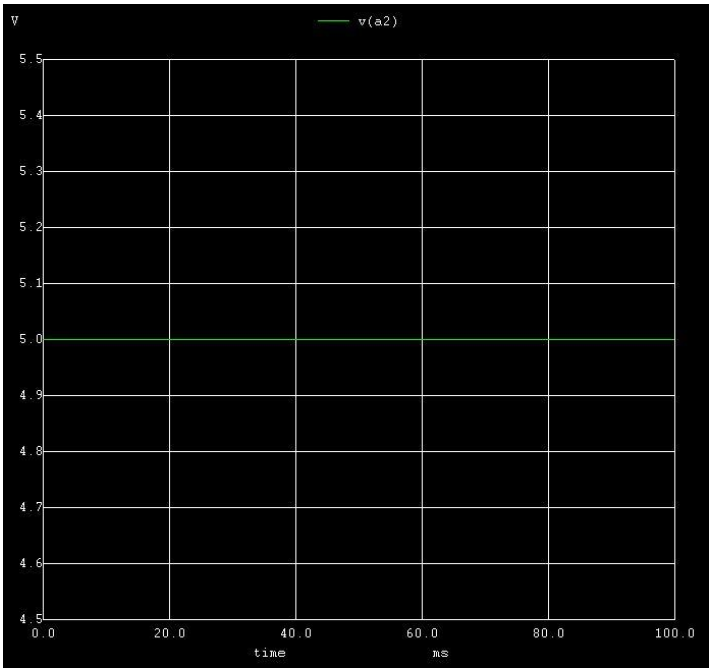
a0(v5)



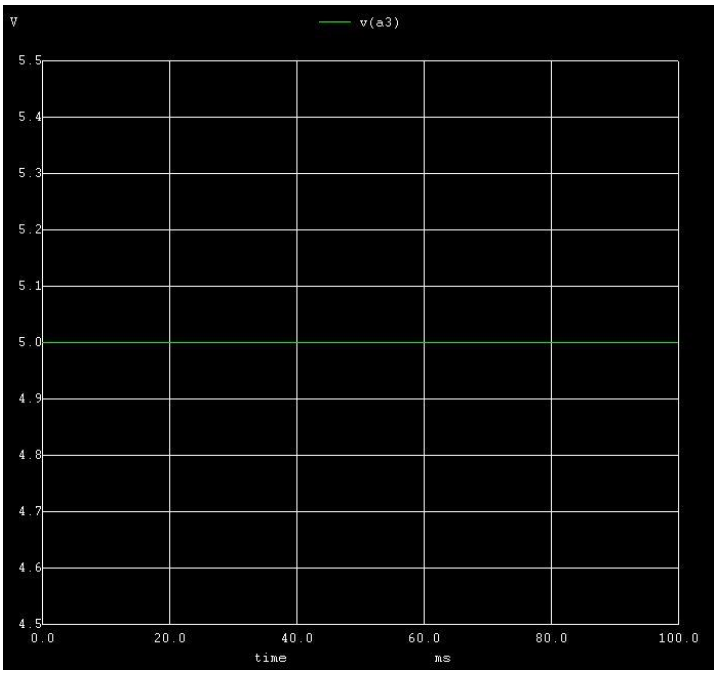
a1 (v6)



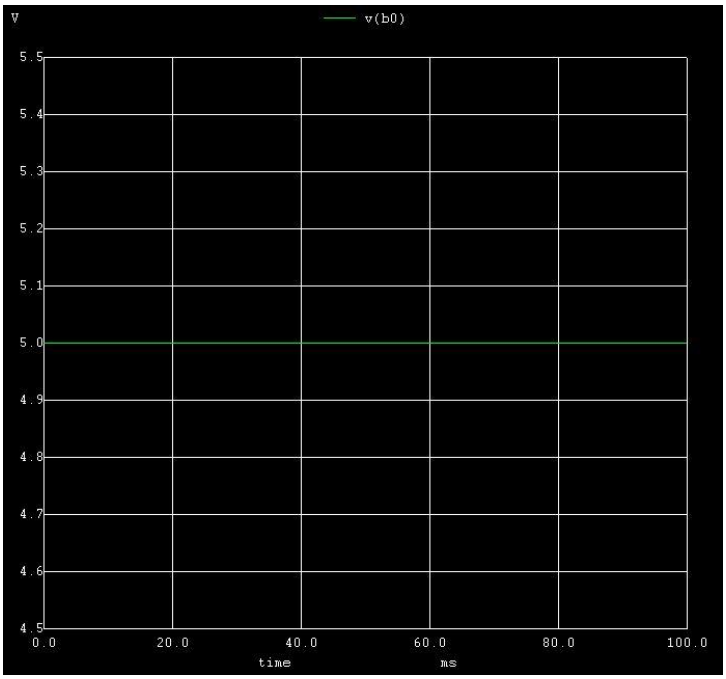
a2 (v7)



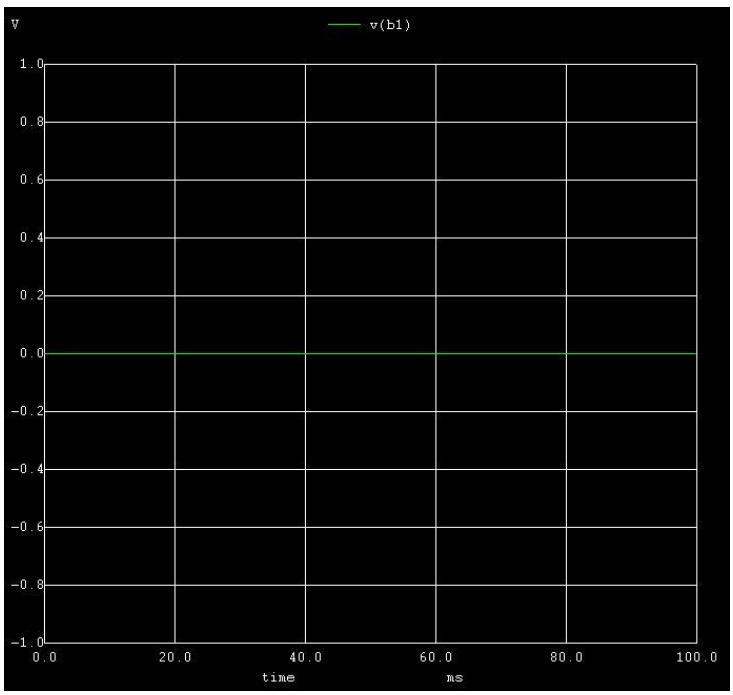
a3 (v8)



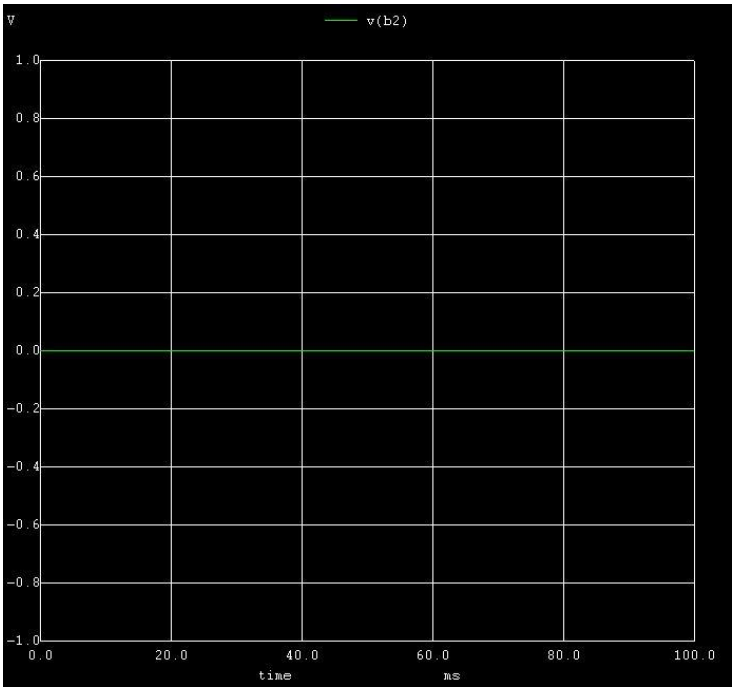
b0 (v1)



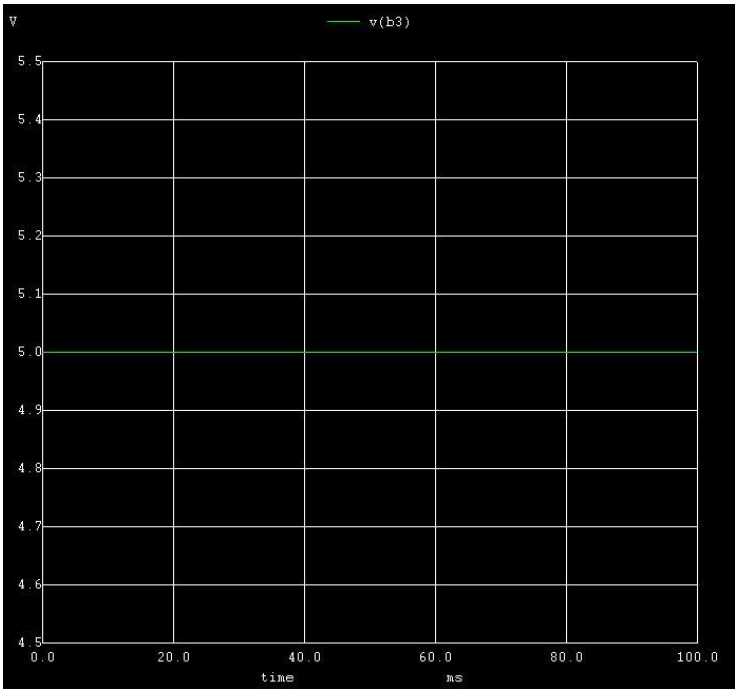
b1 (v2)



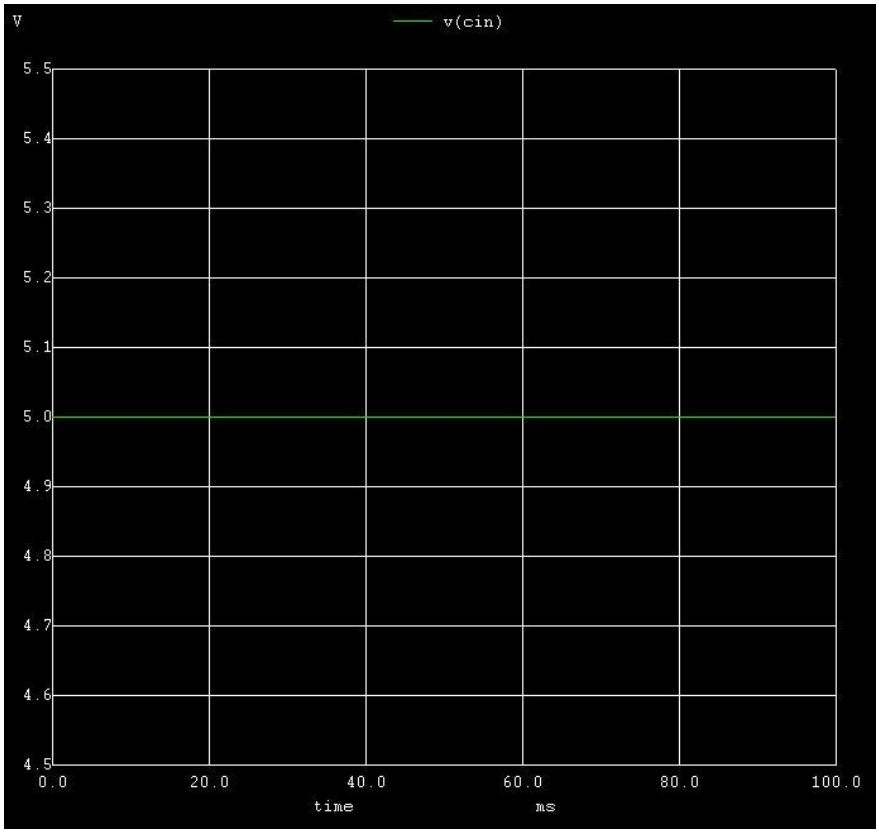
b2 (v3)



b3 (v4)

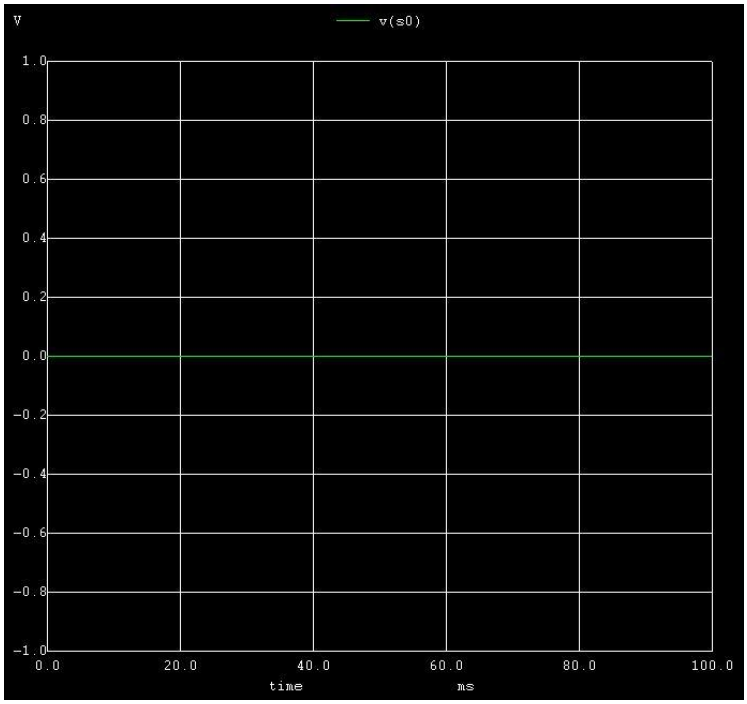


Cin (v9)

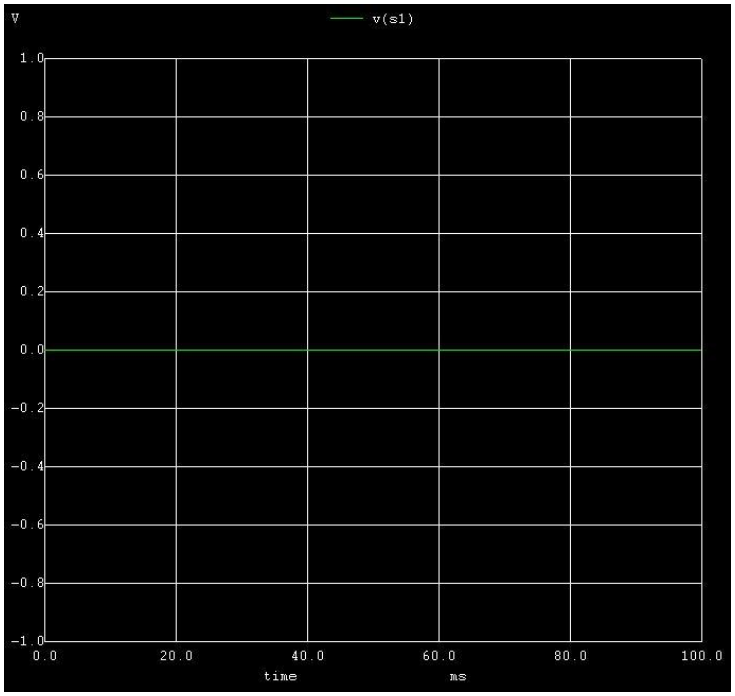


Output:-

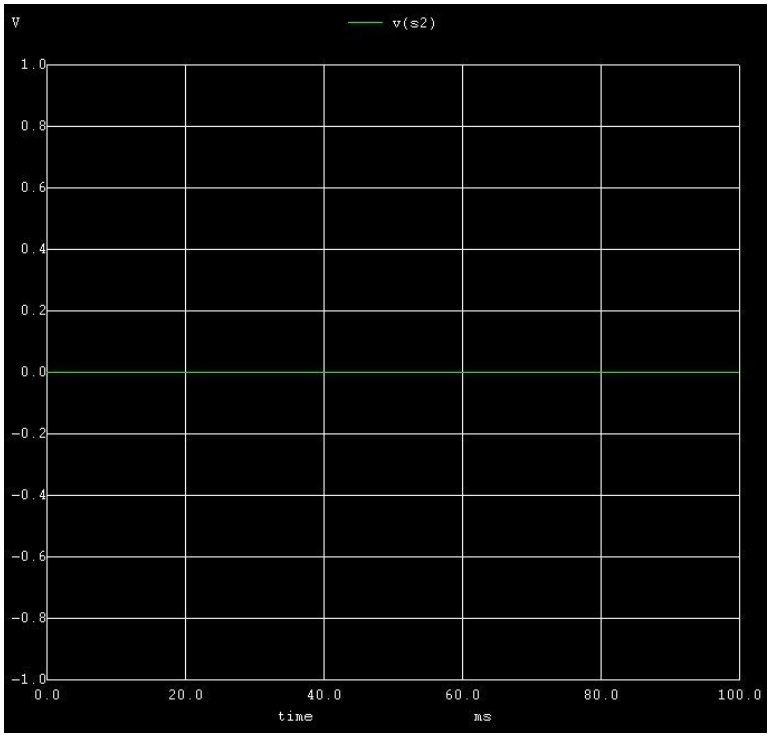
s0



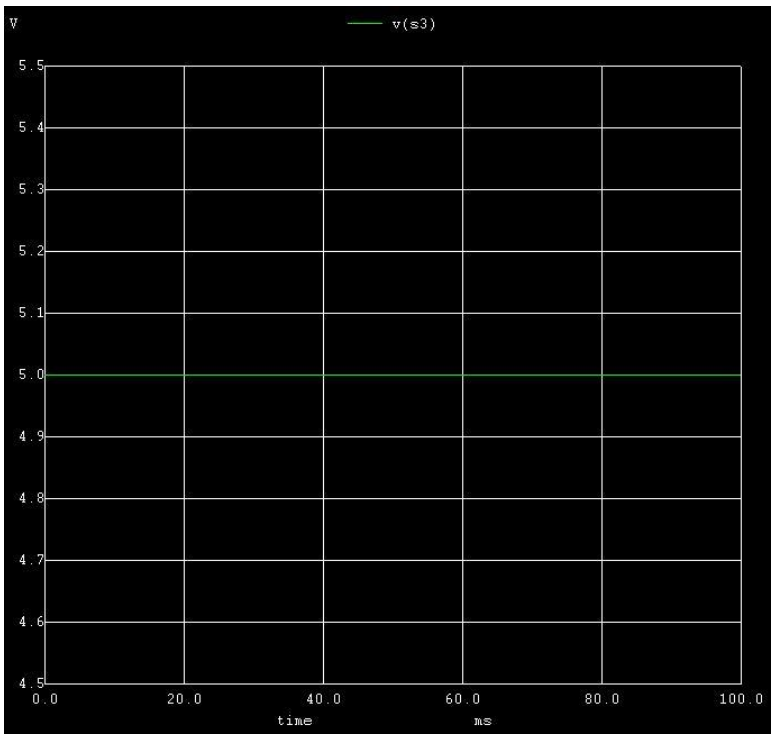
s1



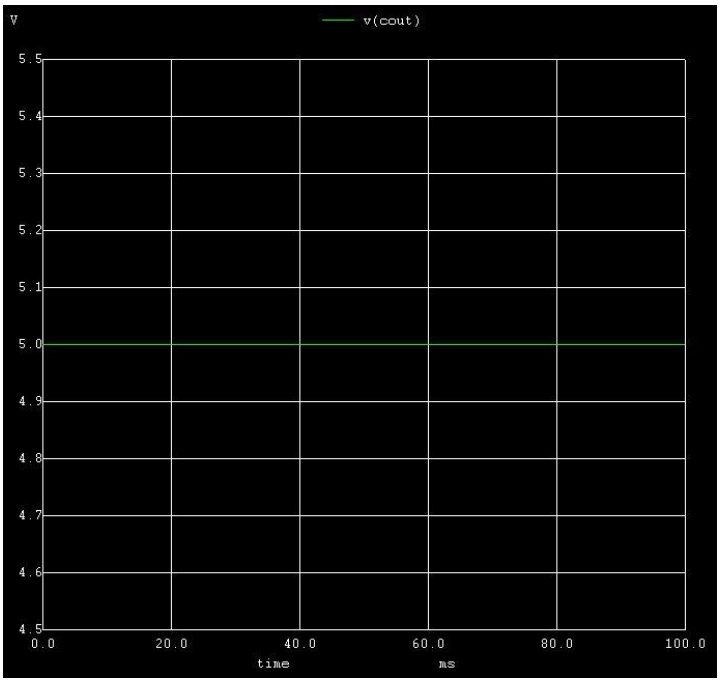
s2



s3



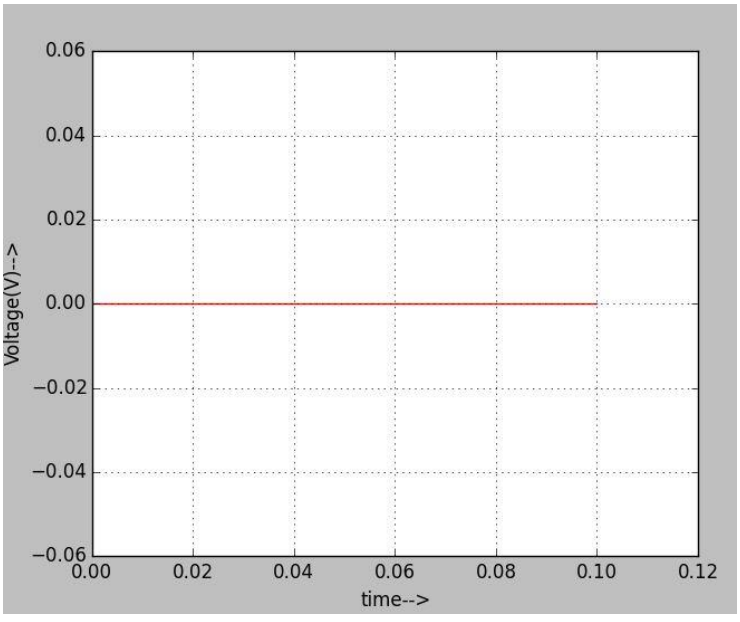
Cout



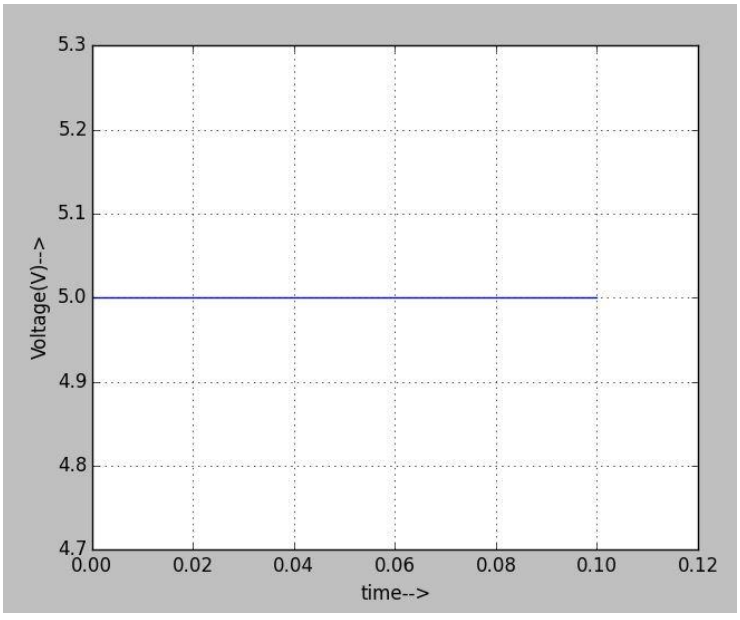
PYTHON PLOTS:-

Input:-

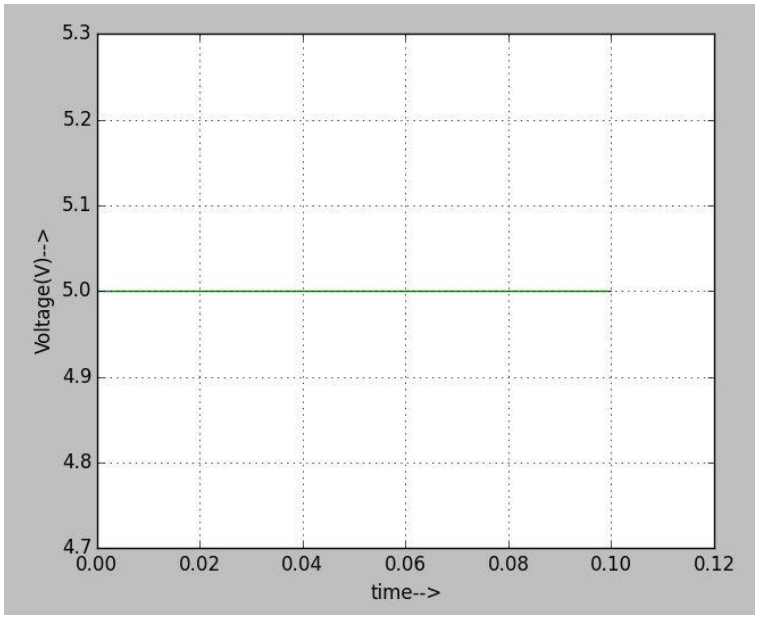
a0(v5)



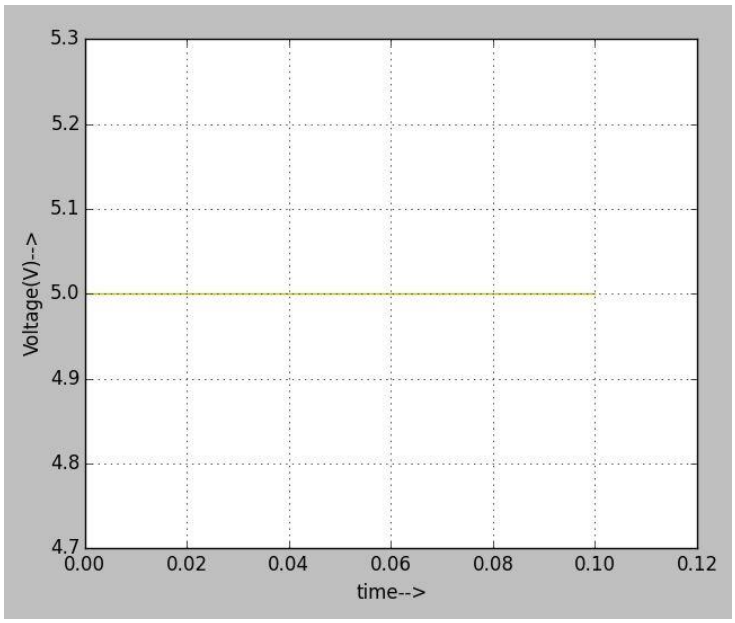
a1 (v6)



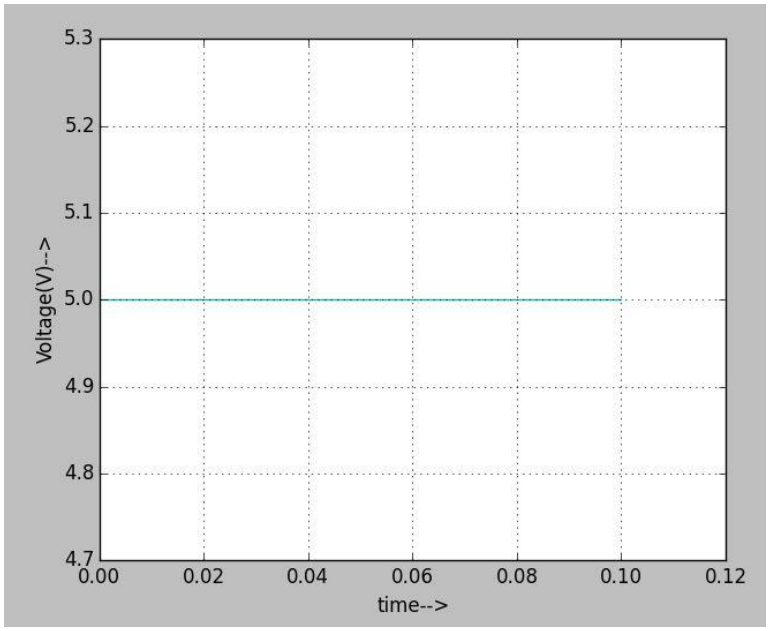
a2 (v7)



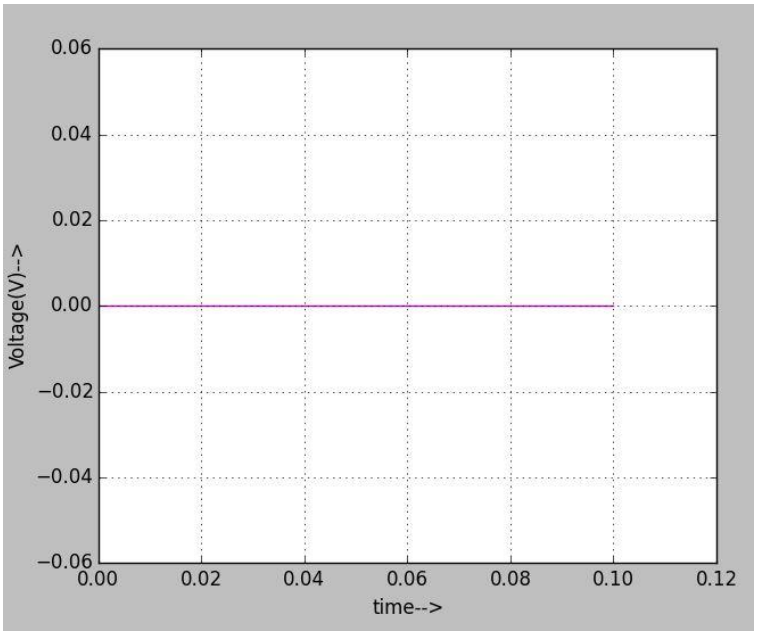
a3 (v8)



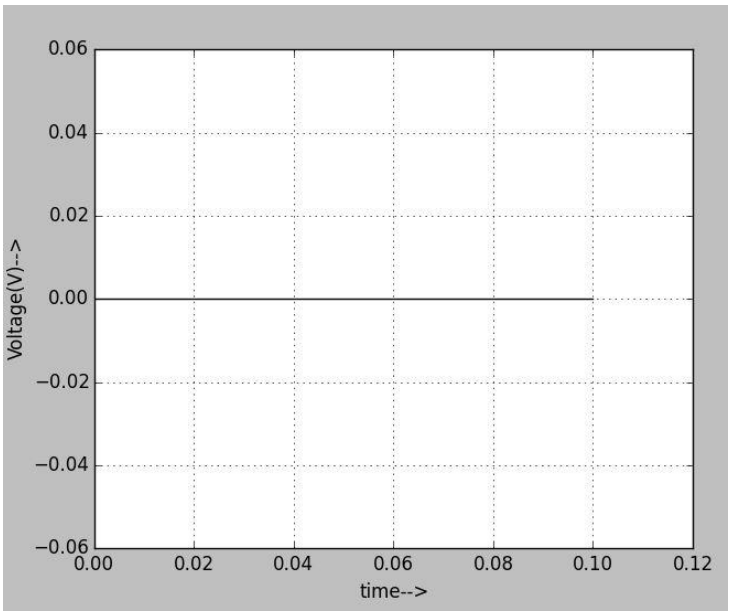
b0 (v1)



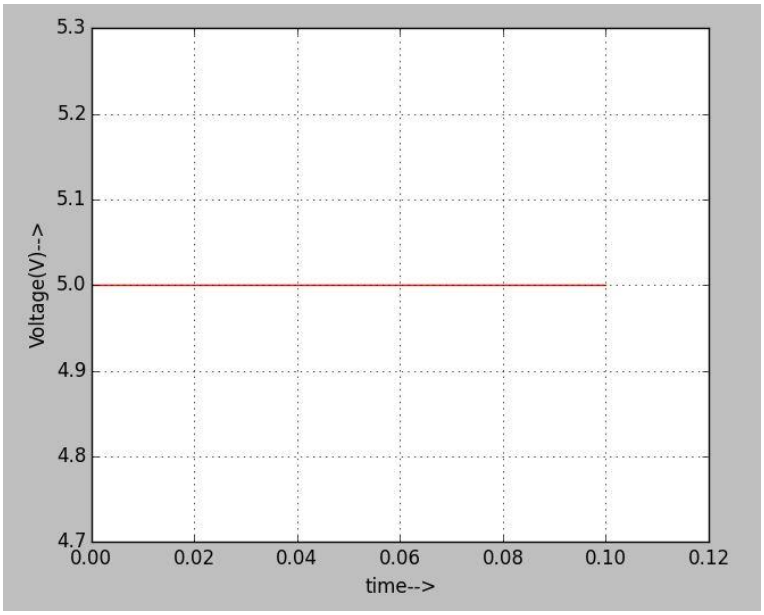
b1 (v2)



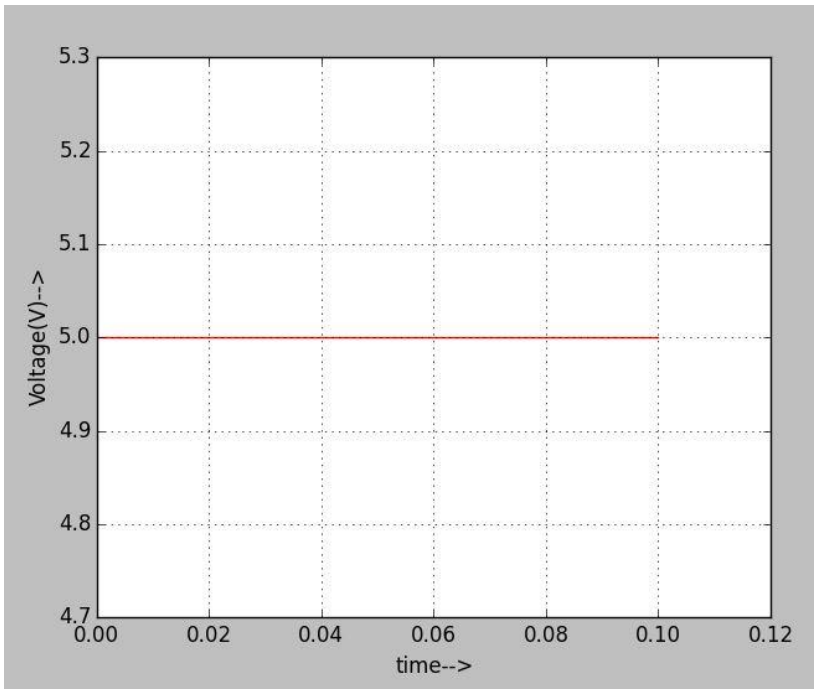
b2 (v3)



b3 (v4)

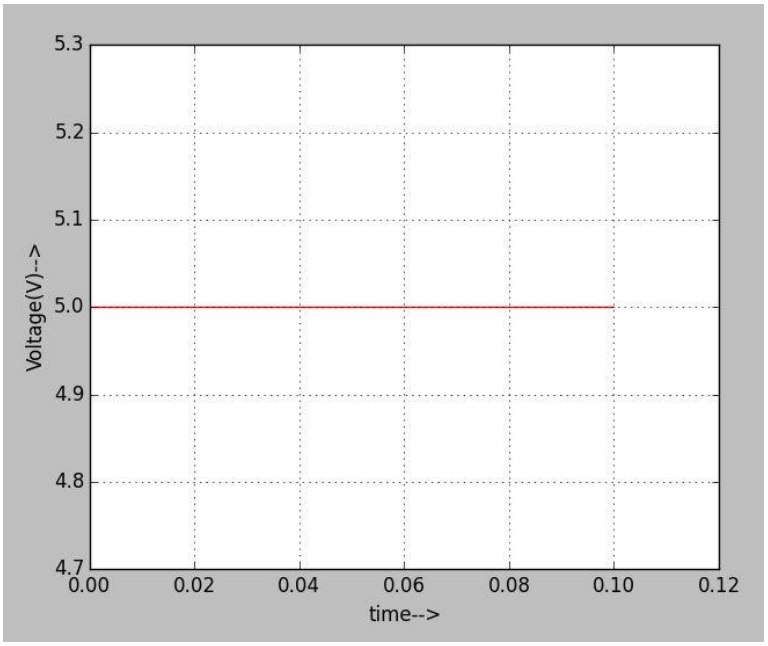


Cin (v9)

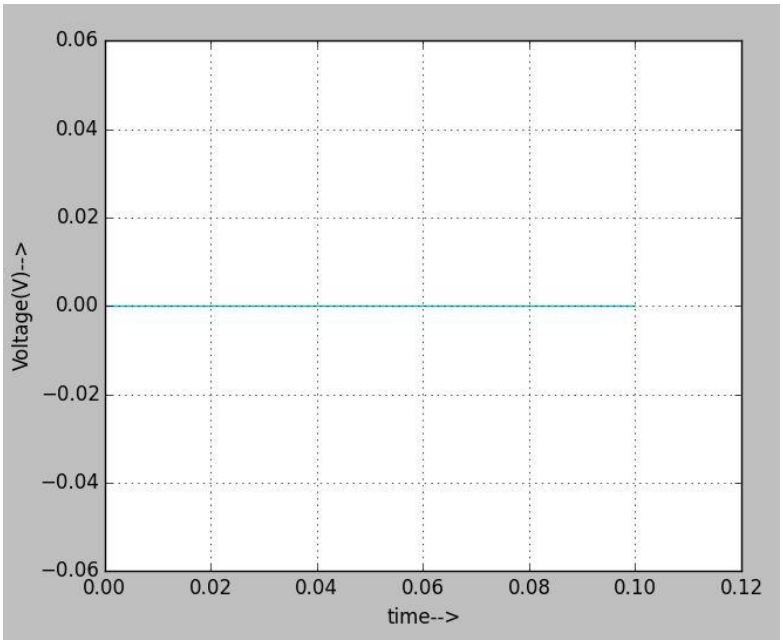


Output:-

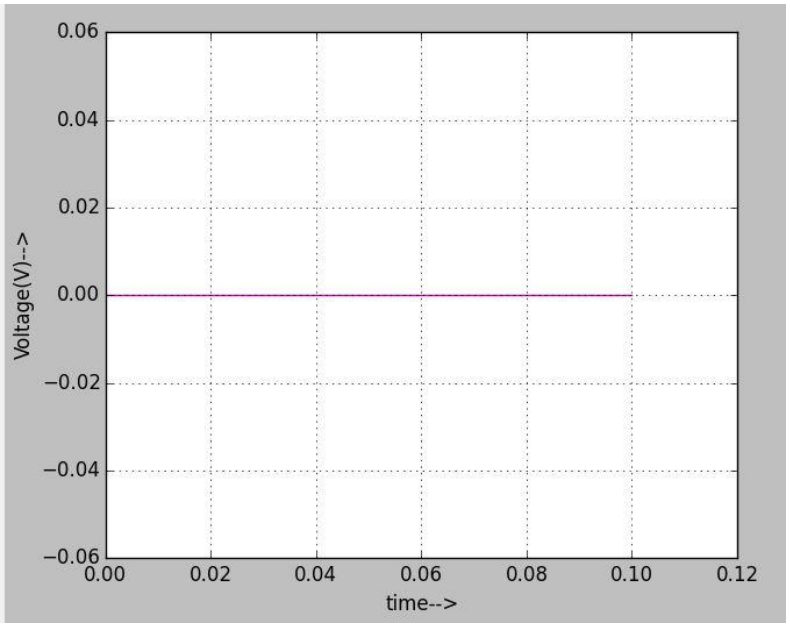
s0



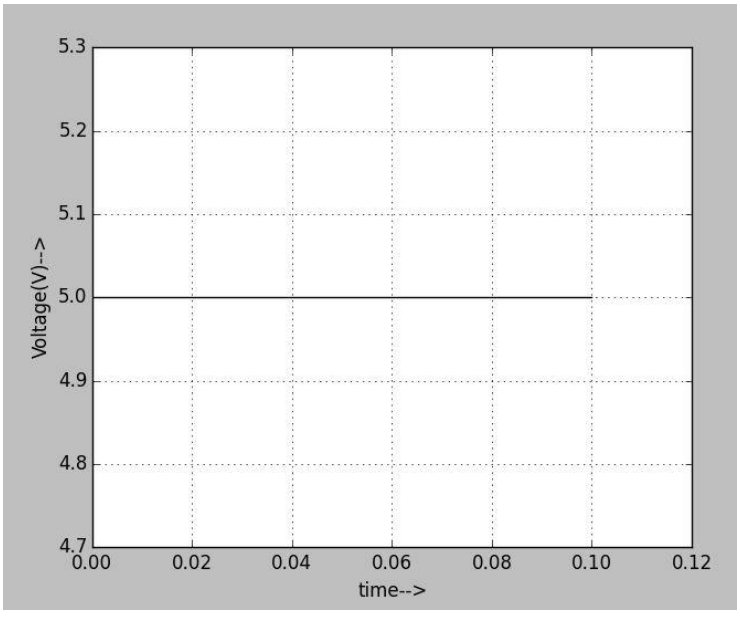
s1



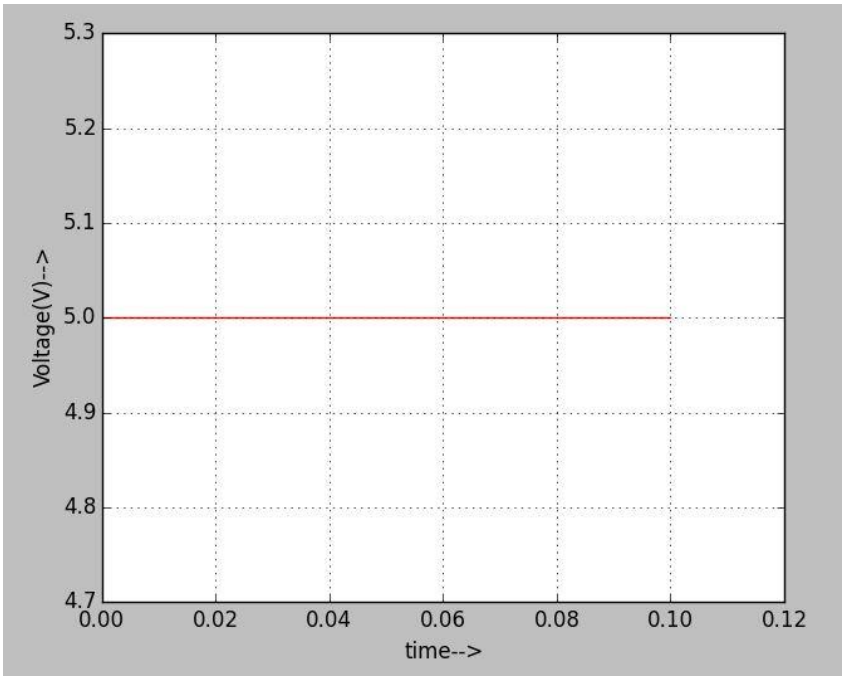
s2



s3



Cout



INPUT :-

a[3:0] : 1 1 1 0

b[3:0] : 1 0 0 1

Cin : 1

OUTPUT :-

Cout : 1

s[3:0] : 1 0 0 1

REFERENCES:-

1) https://en.wikibooks.org/wiki/Practical_Electronics/IC/4008#/media/File:4008_Gate-level_Diagram.svg