TITLE OF THE EXPERIMENT

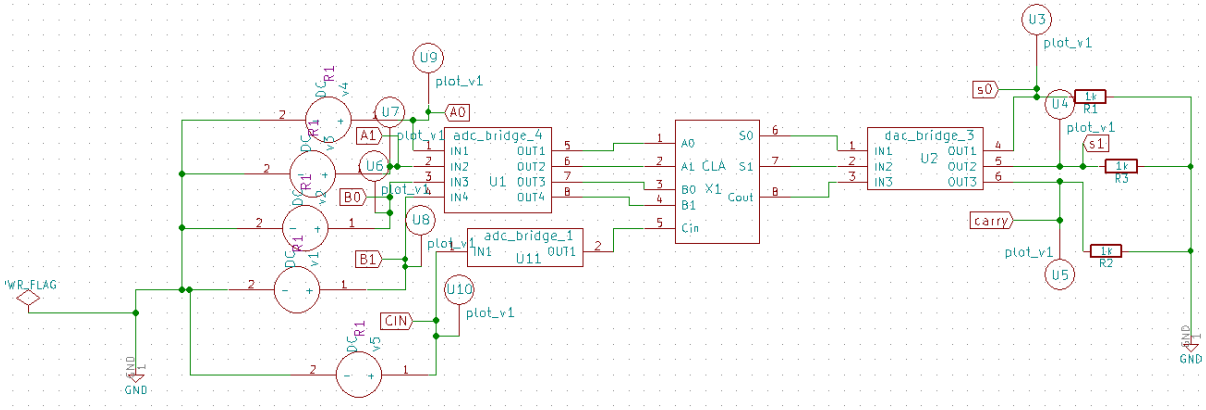
DESIGN OF TWO BIT CARRY LOOK AHEAD ADDER USING SUBCIRCUIT BUILDER

THEORY

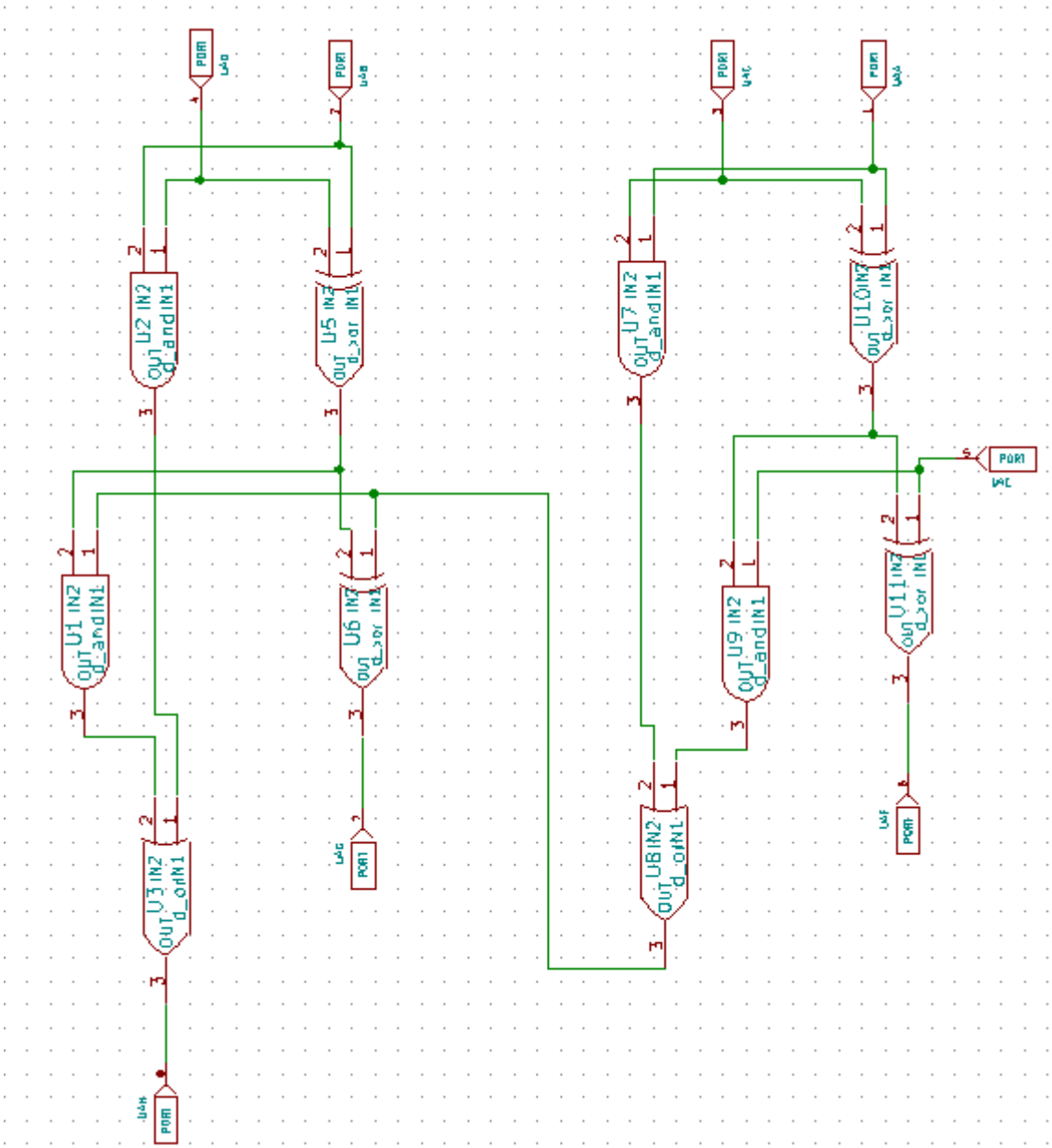
In case of parallel adders, the binary addition of two numbers is initiated when all the bits of the augend and the addend must be available at the same time to perform the computation. In a parallel adder circuit, the carry output of each full adder stage is connected to the carry input of the next higher-order stage, hence it is also called as ripple carry type adder.In such adder circuits, it is not possible to produce the sum and carry outputs of any stage until the input carry occurs. So there will be a considerable time delay in the addition process , which is known as , carry propagation delay. In any combinational circuit , signal must propagate through the gates before the correct output sum is available in the output terminals.

Schematic Diagram

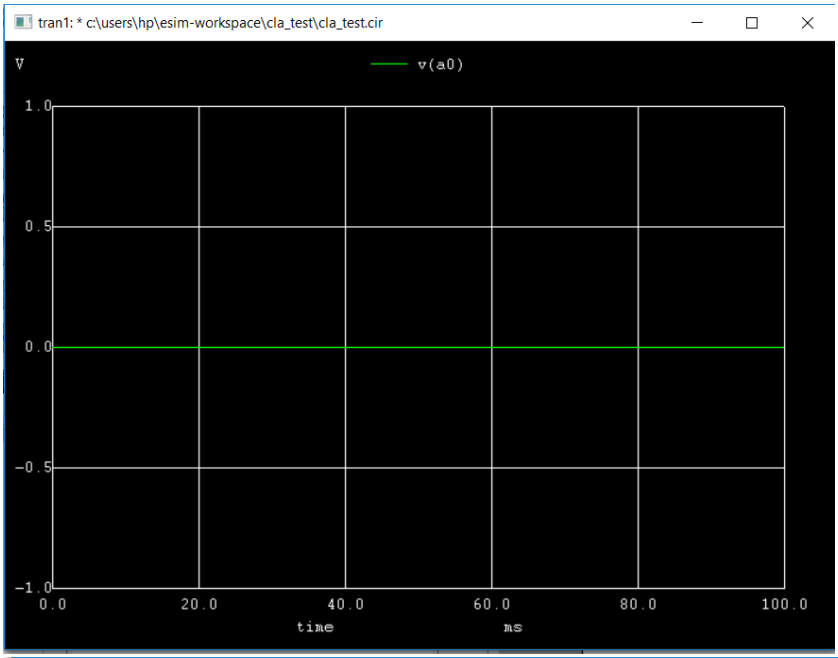
The schematic diagram of two bit carry look ahead adder is.

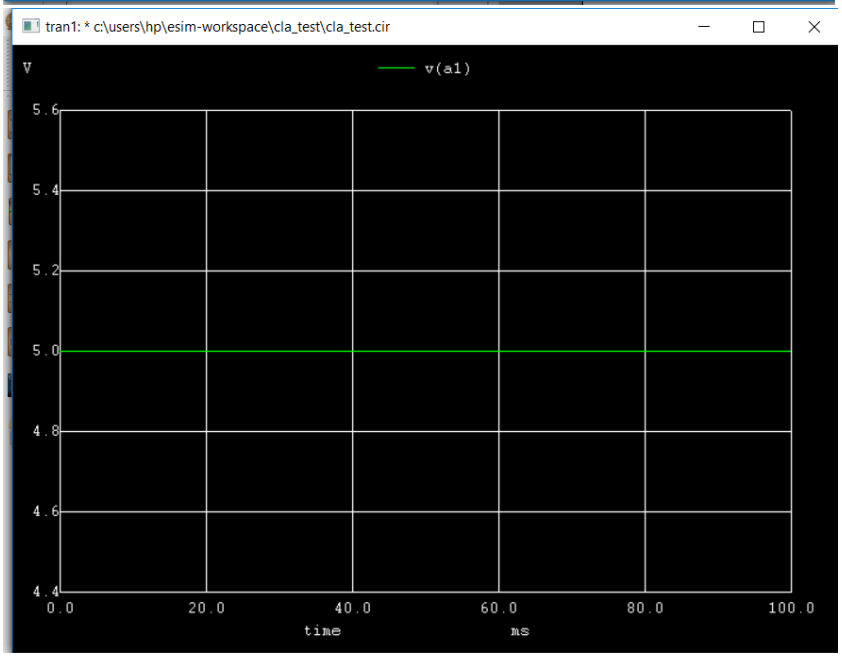


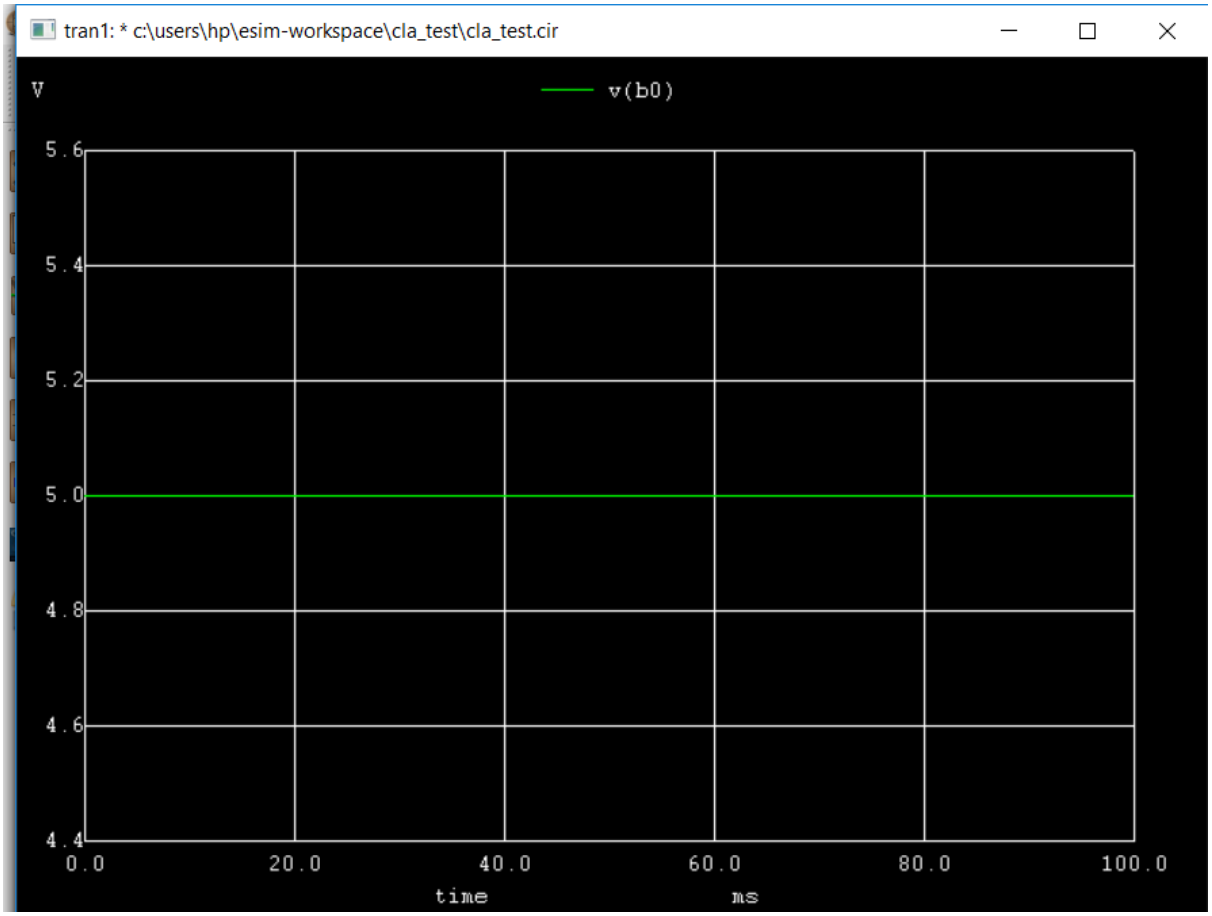
Here I used a subcircuit for two bit carry look ahead adder.The internal structure of carry look ahead adder is shown below.



Input Ngspice Plots:



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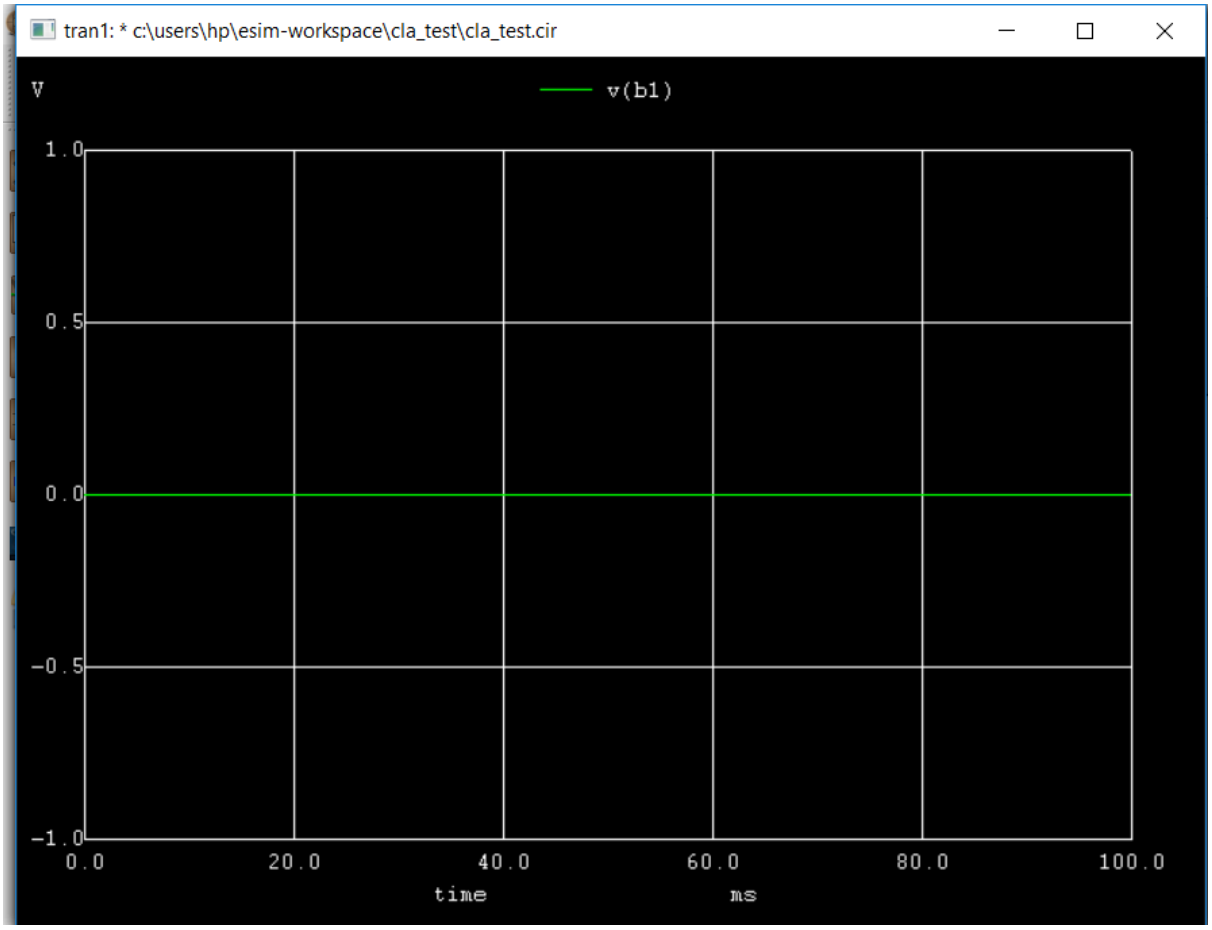
5.4
5.2
5.0
4.8
4.6
4.4
0.0
20.0
40.0
60.0
80.0
100.0
time
ms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0.0
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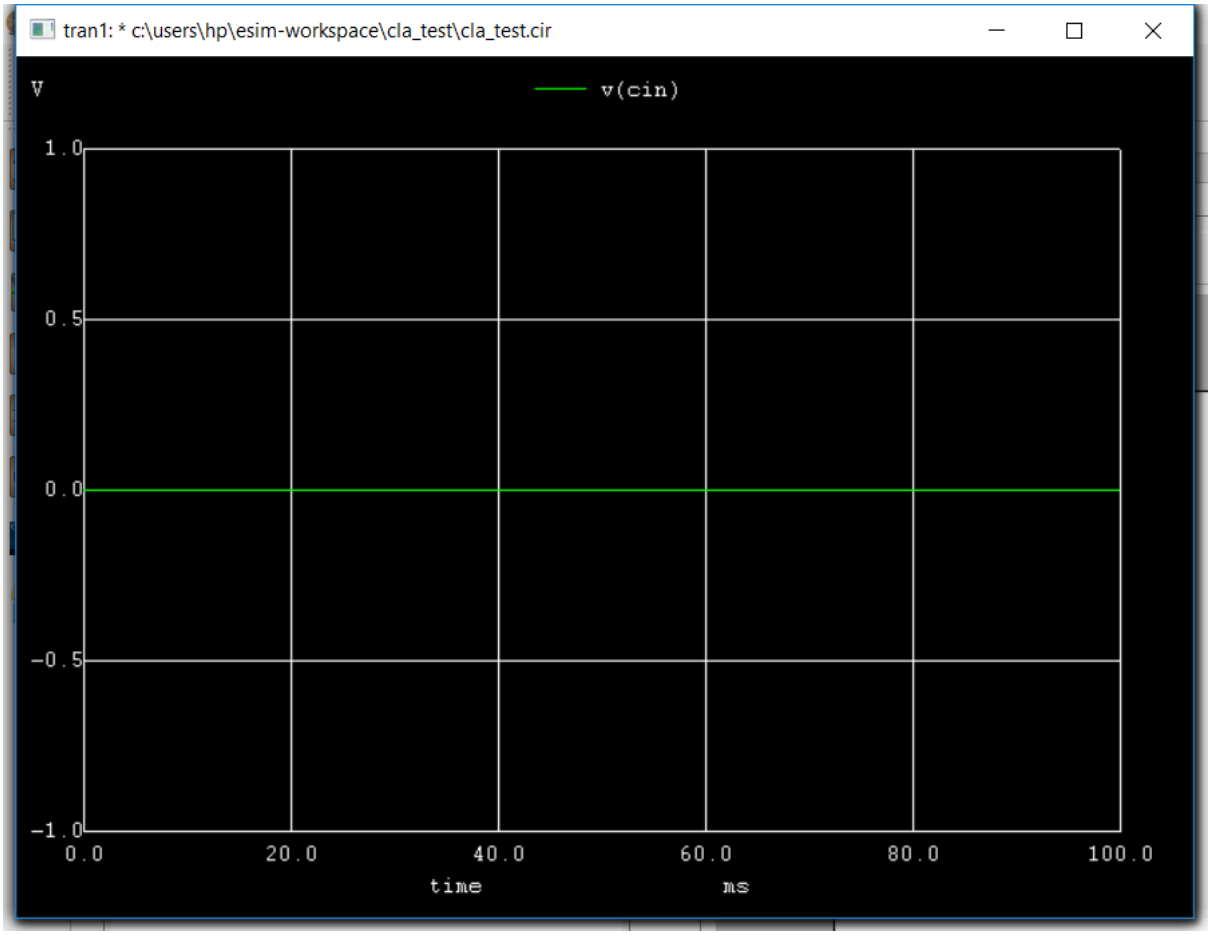
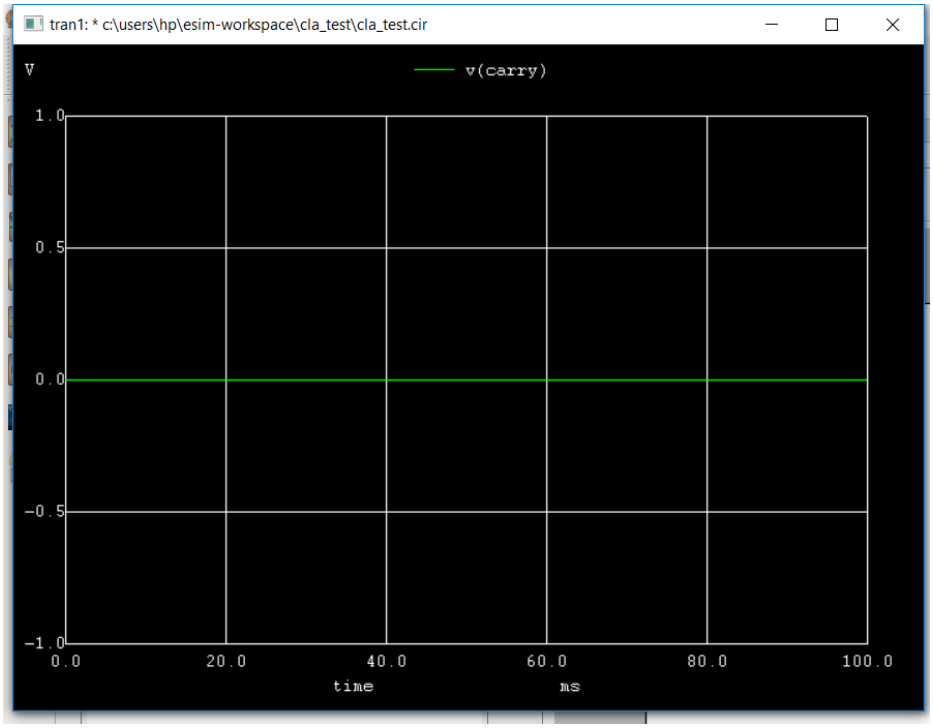
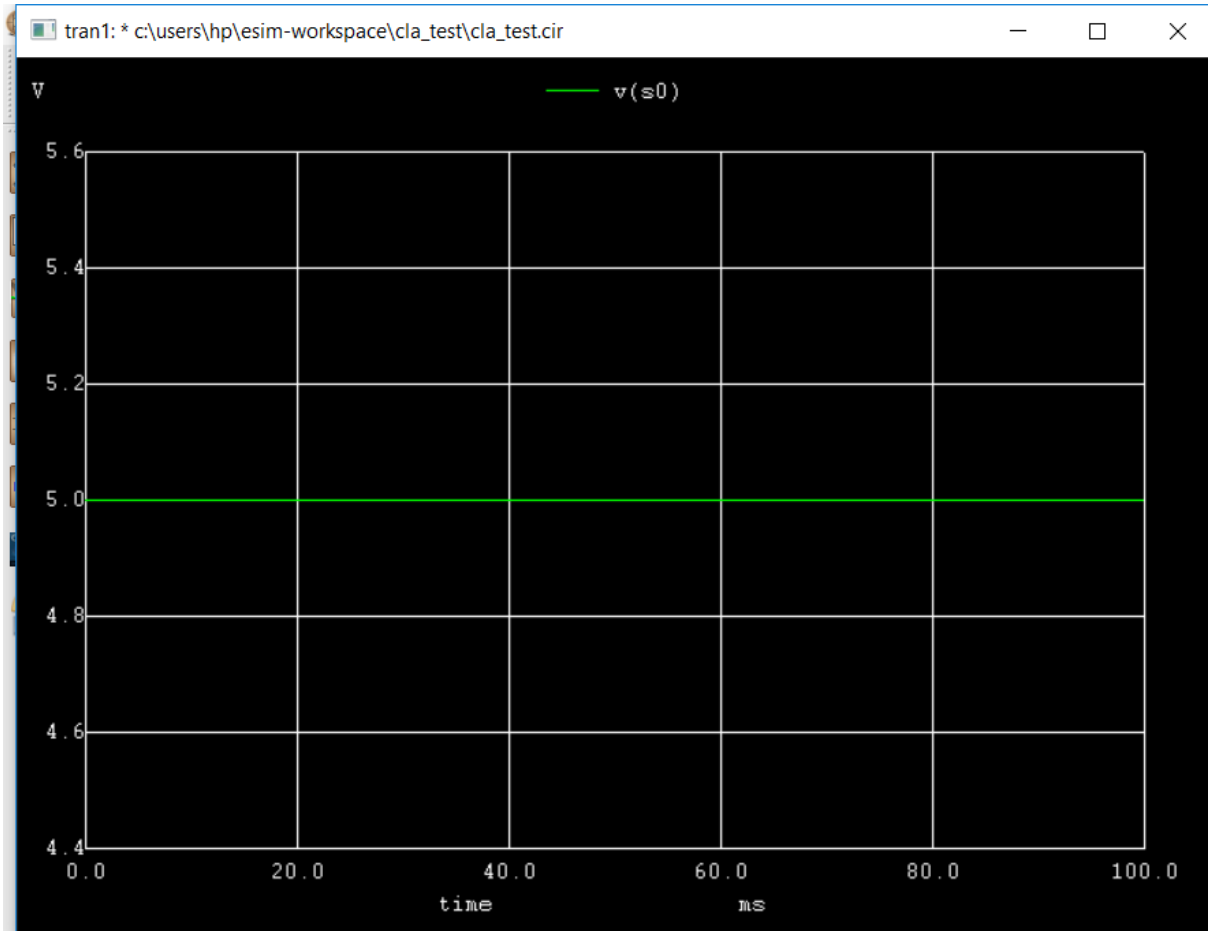
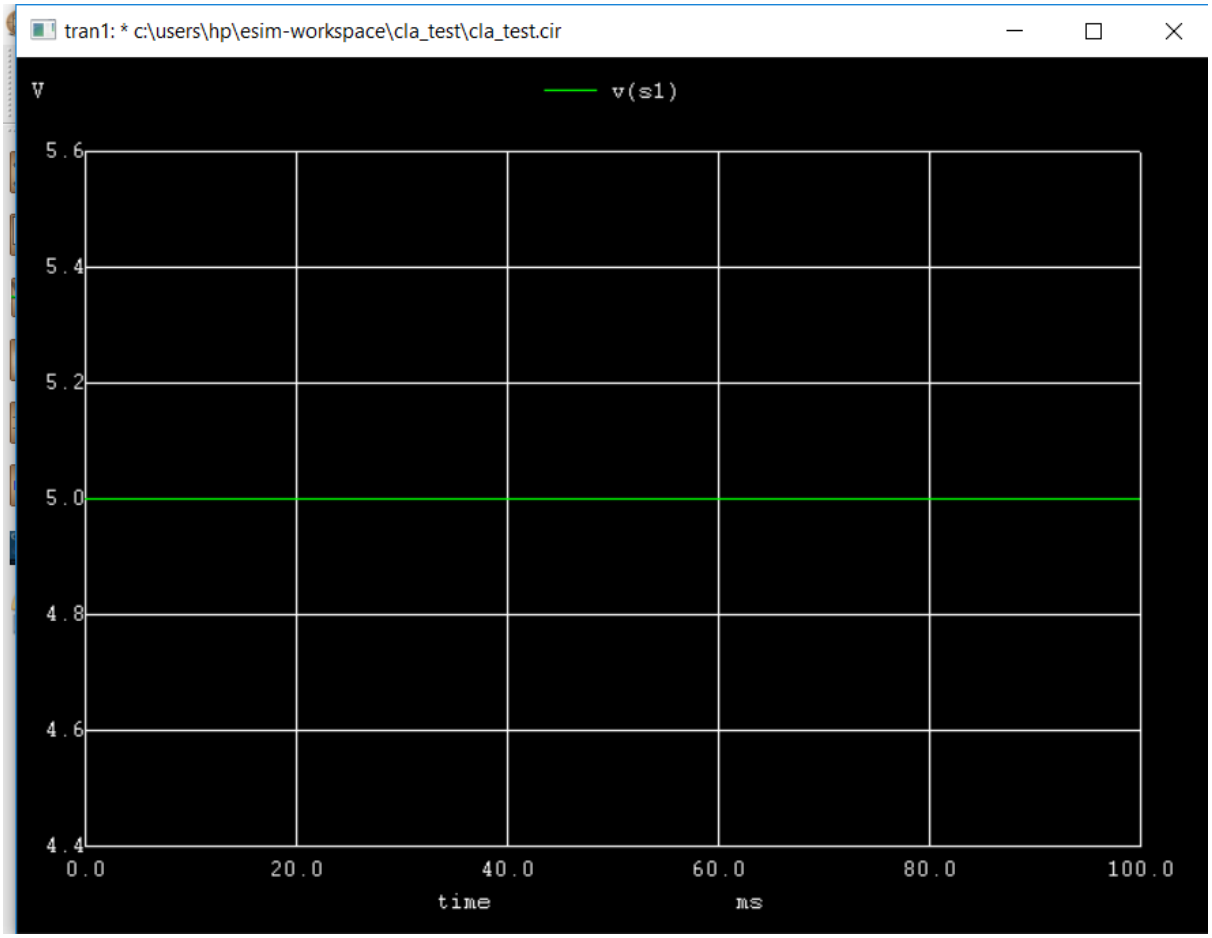
-1.0
0.0
20.0
40.0
60.0
80.0
100.0
time
ms



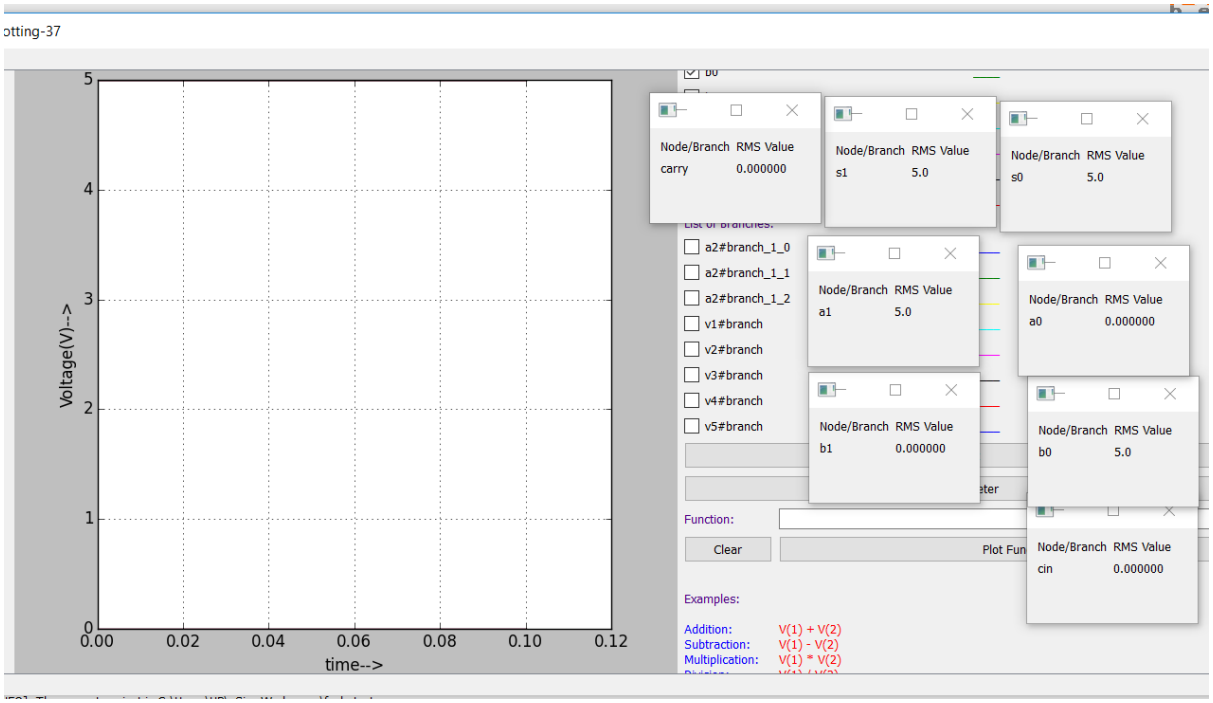
Output Ngspice Plots:




tran1: * c:\users\hp\esim-workspace\cla_test\cla_test.cir
V
v(s0)
5.6
5.4
5.2
5.0
4.8
4.6
4.4
0.0
20.0
40.0
60.0
80.0
100.0
time
ms


tran1: * c:\users\hp\esim-workspace\cla_test\cla_test.cir
V
v(s1)
5.6
5.4
5.2
5.0
4.8
4.6
4.4
0.0
20.0
40.0
60.0
80.0
100.0
time
ms

Python Plot:



References:

https://www.electronicshub.org/carry-look-ahead-adder/