TITLE OF THE EXPERIMENT

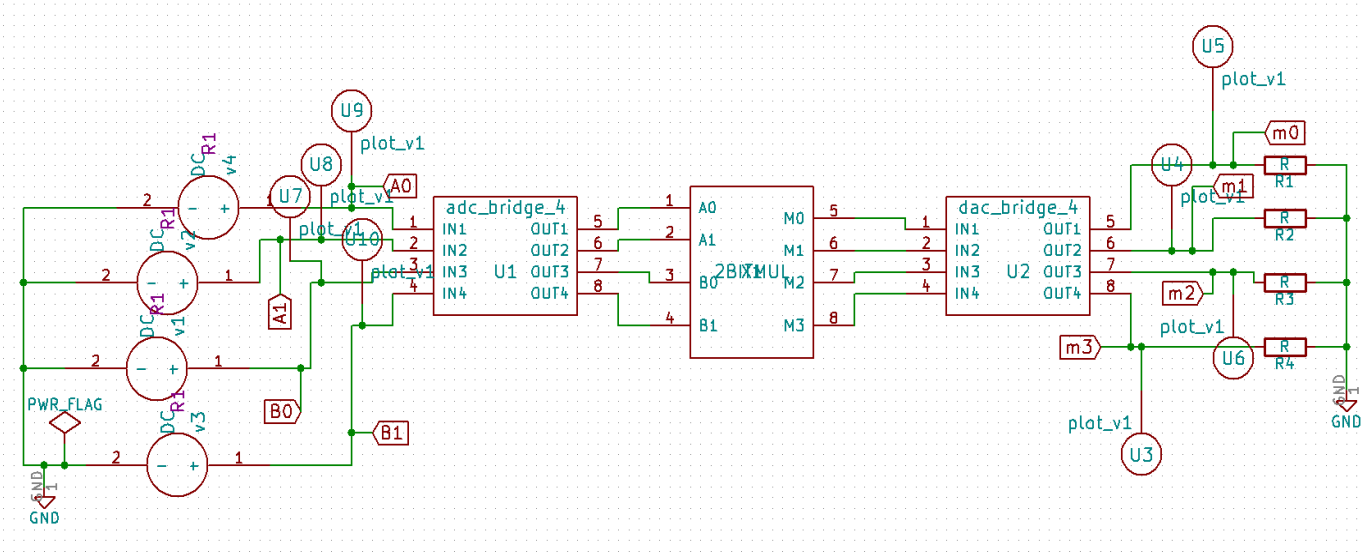
DESIGN OF TWO BIT MULTIPLIER USING SUBCIRCUIT BUILDER

THEORY

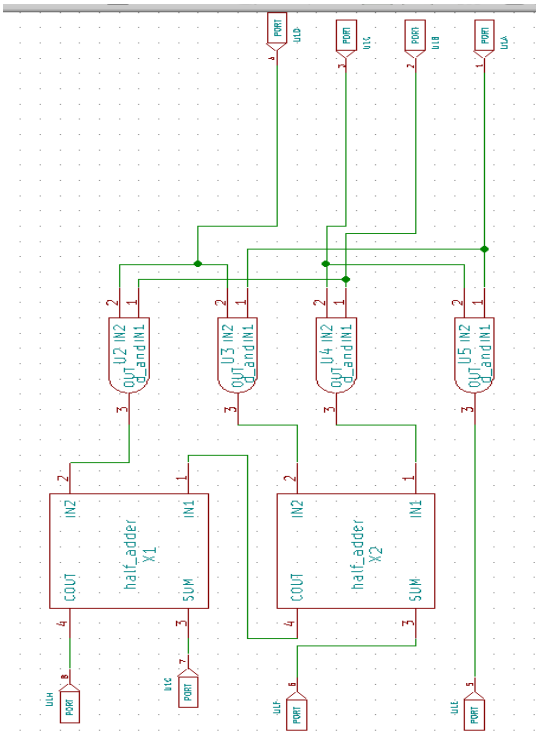
A 2-bit multiplier can be implemented as a straightforward combinational logic circuit using basic logic gates.It consists of 4 inputs and four outputs. The 4 inputs are the two pairs of two bits, call them A and B.

Schematic Diagram

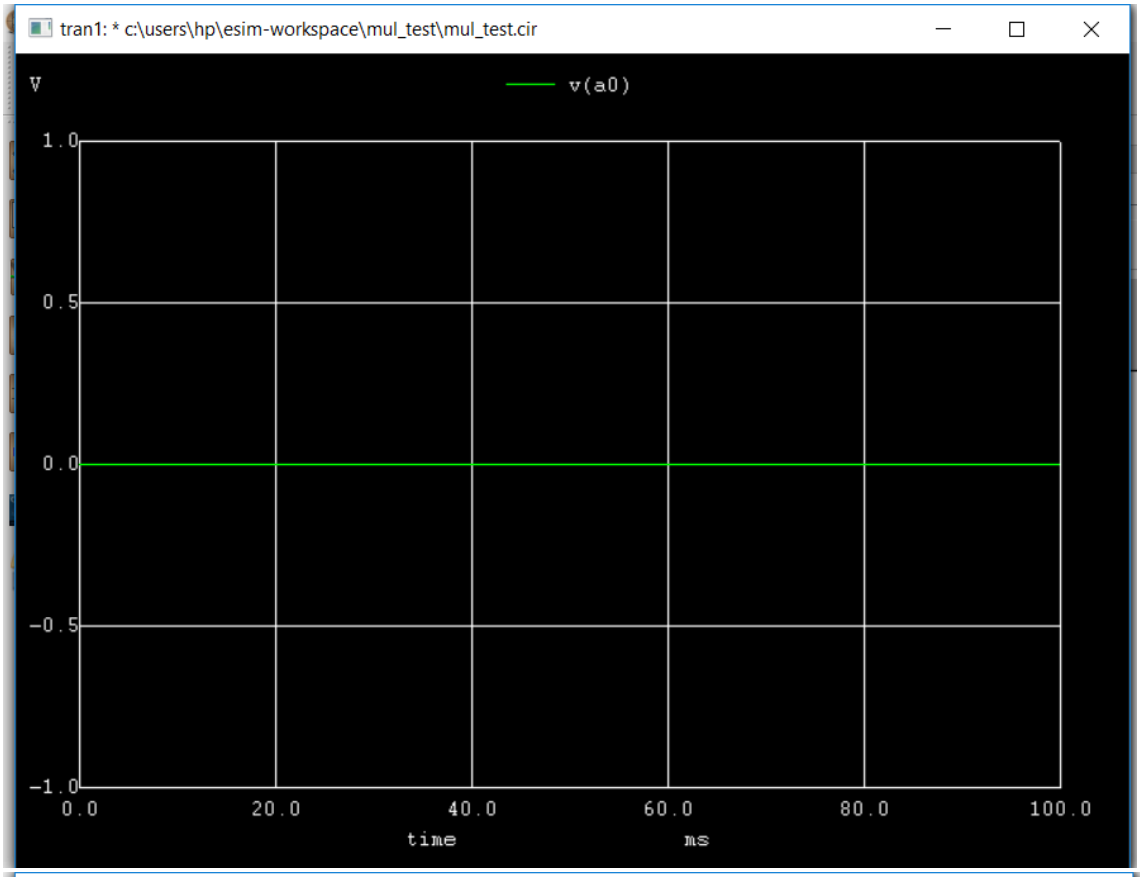
The schematic diagram of two bit multiplier is.

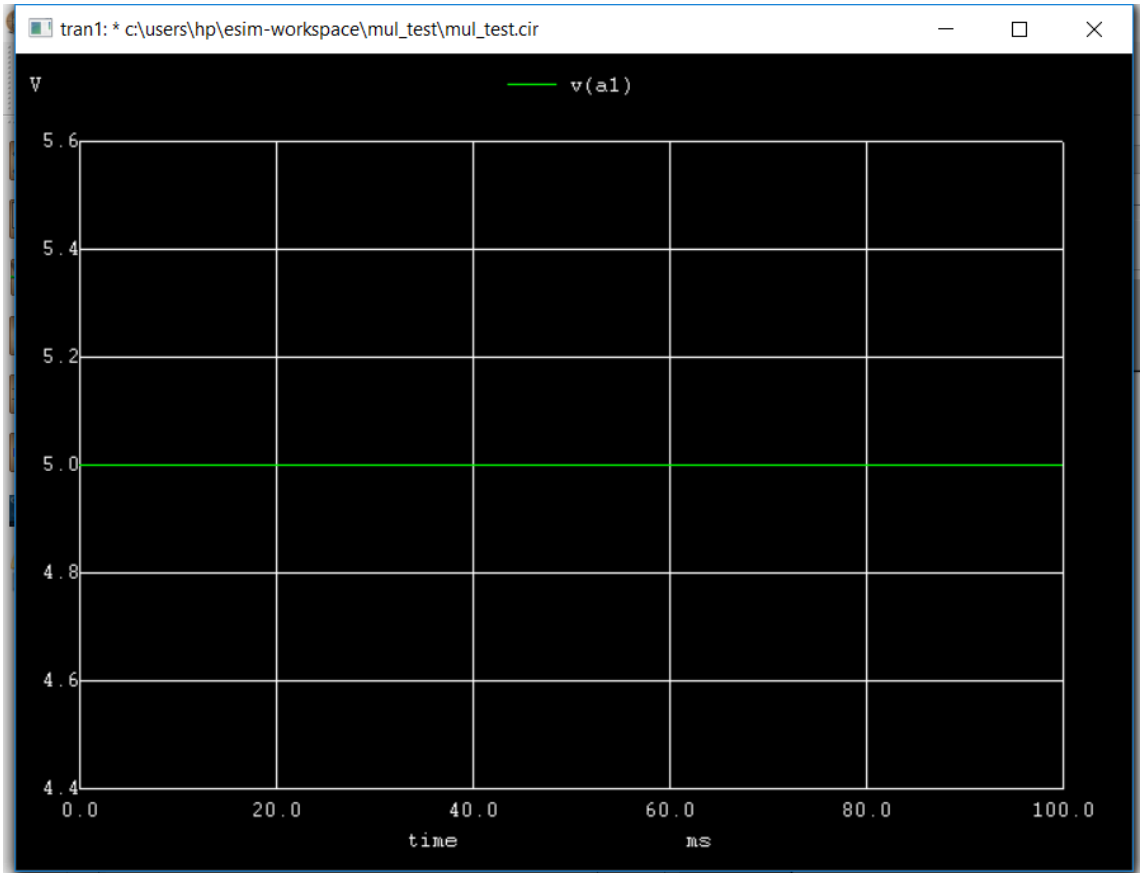


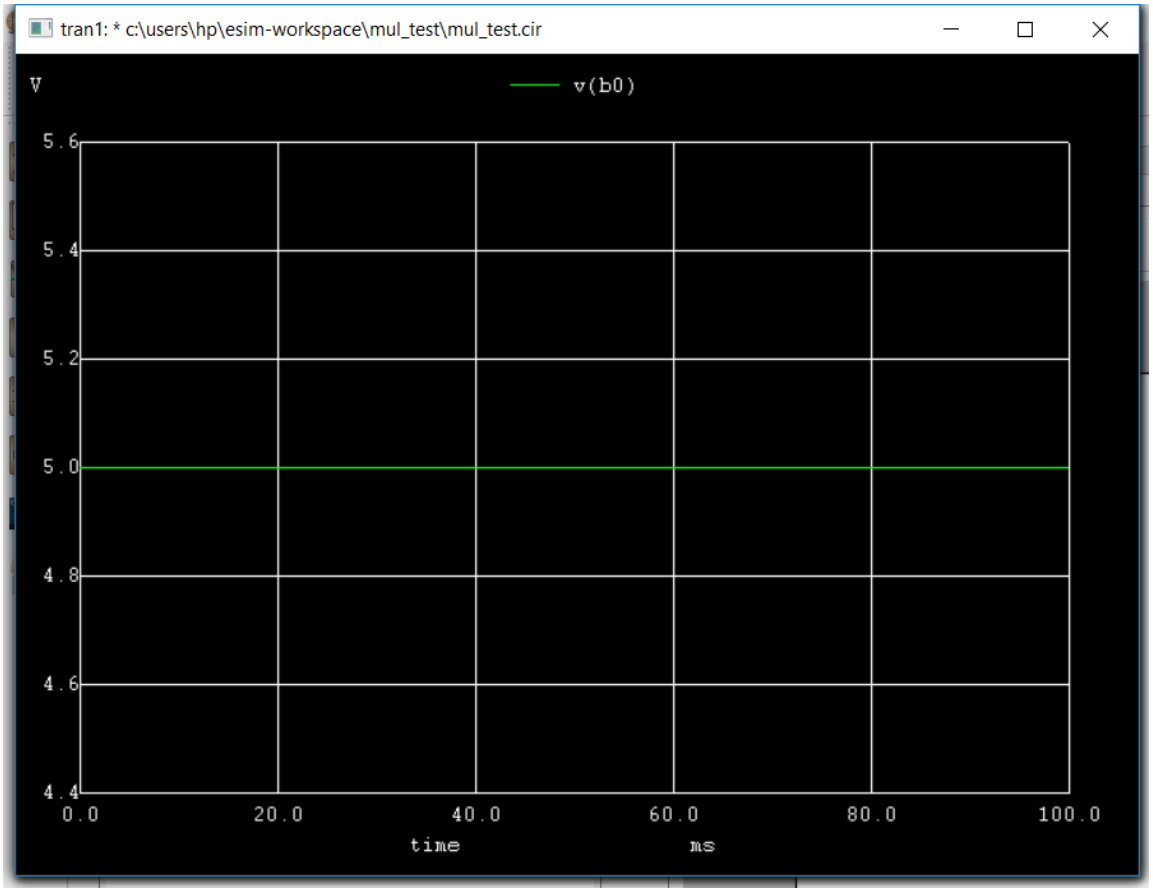
Here I used a subcircuit for two bit multiplication.The internal structure of 2 bit multiplier is shown below.

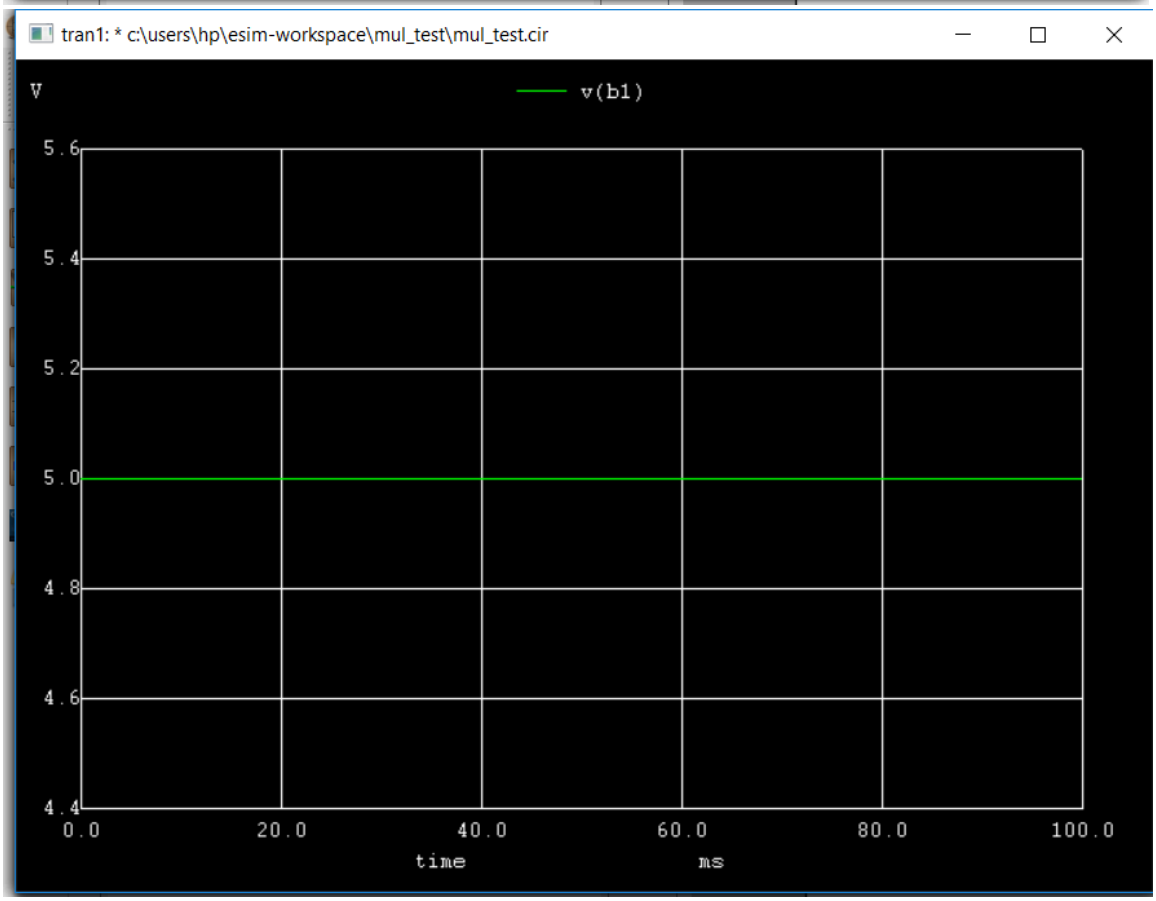


Input Ngspice Plots:

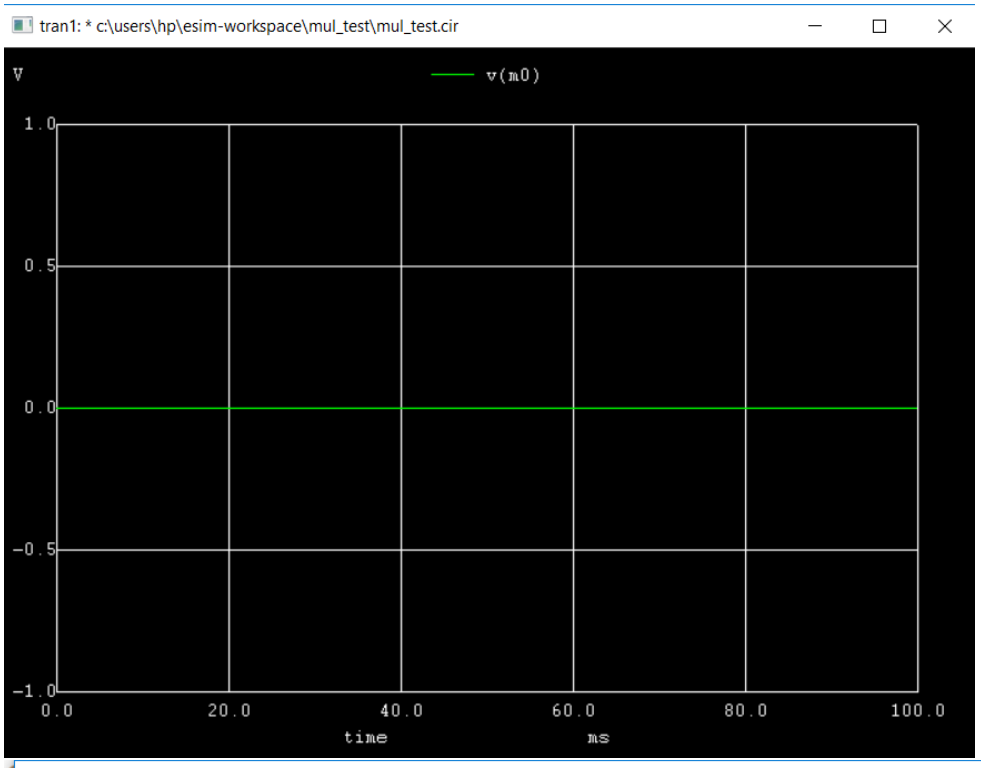


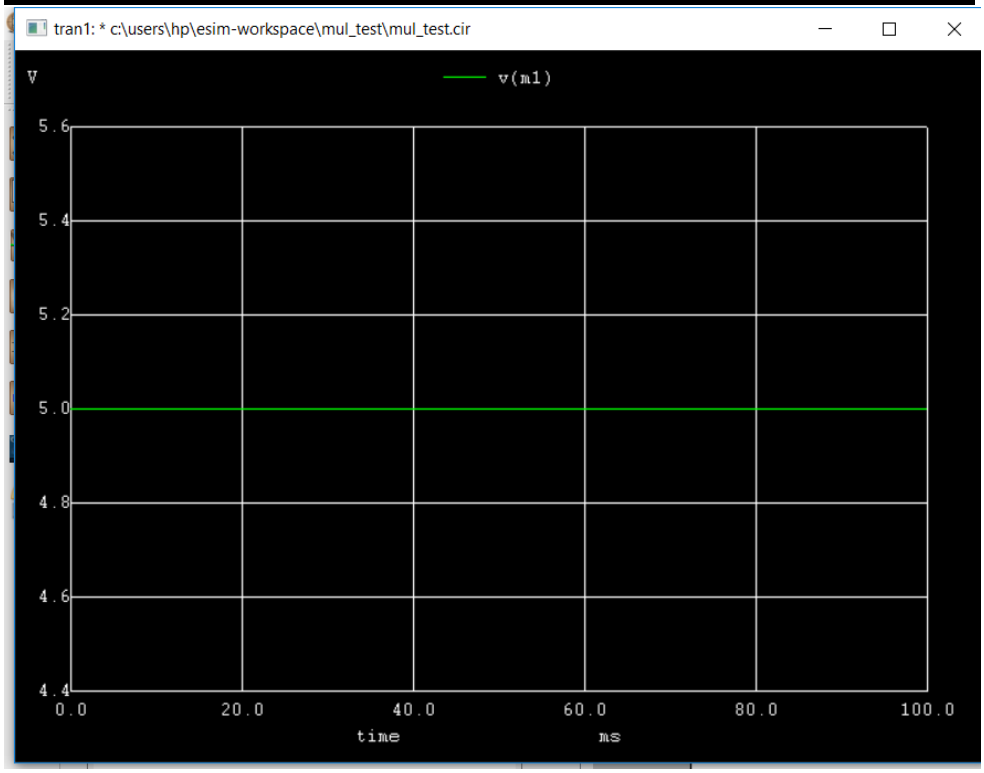


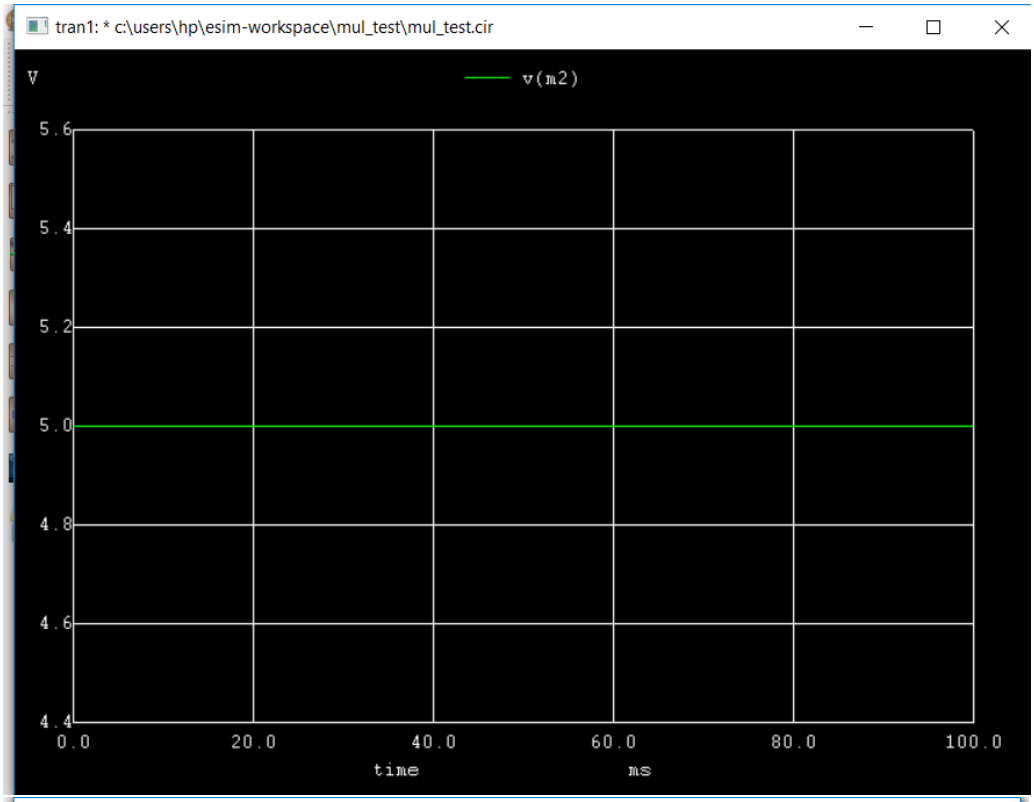

tran1: * c:\users\hp\esim-workspace\mul_test\mul_test.cir
V
v(b0)
5.6
5.4
5.2
5.0
4.8
4.6
4.4
0.0
20.0
40.0
60.0
80.0
100.0
time
ms

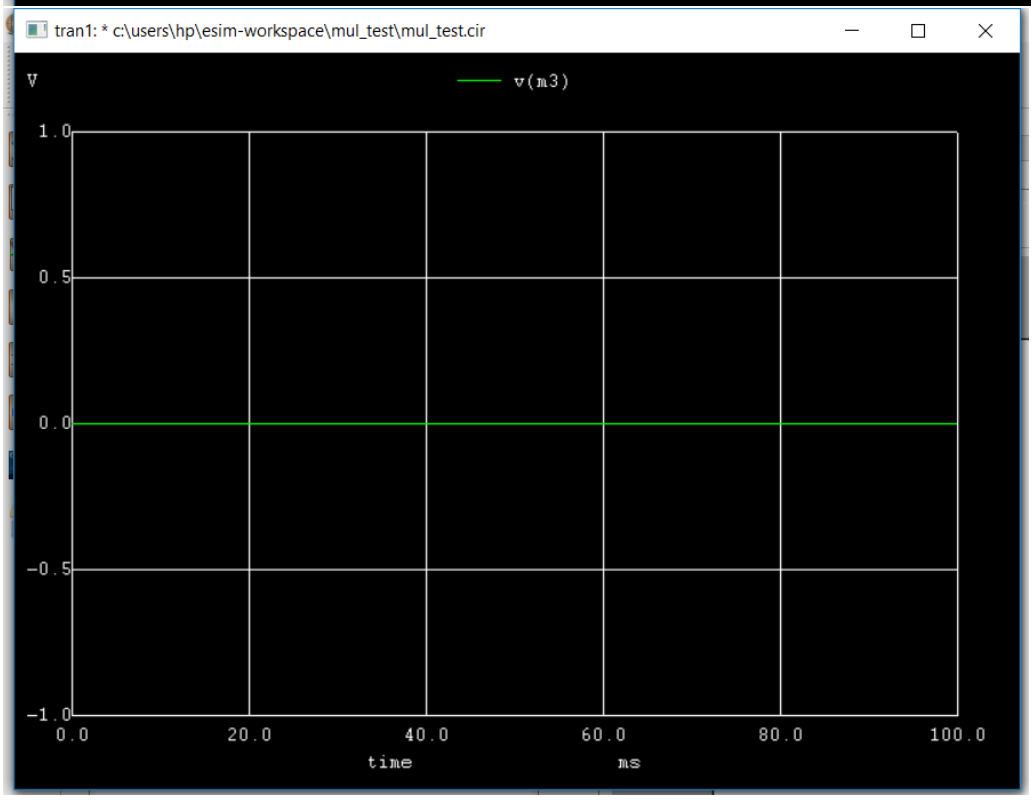

tran1: * c:\users\hp\esim-workspace\mul_test\mul_test.cir
V
v(b1)
5.6
5.4
5.2
5.0
4.8
4.6
4.4
0.0
20.0
40.0
60.0
80.0
100.0
time
ms

Output Ngspice Plots:

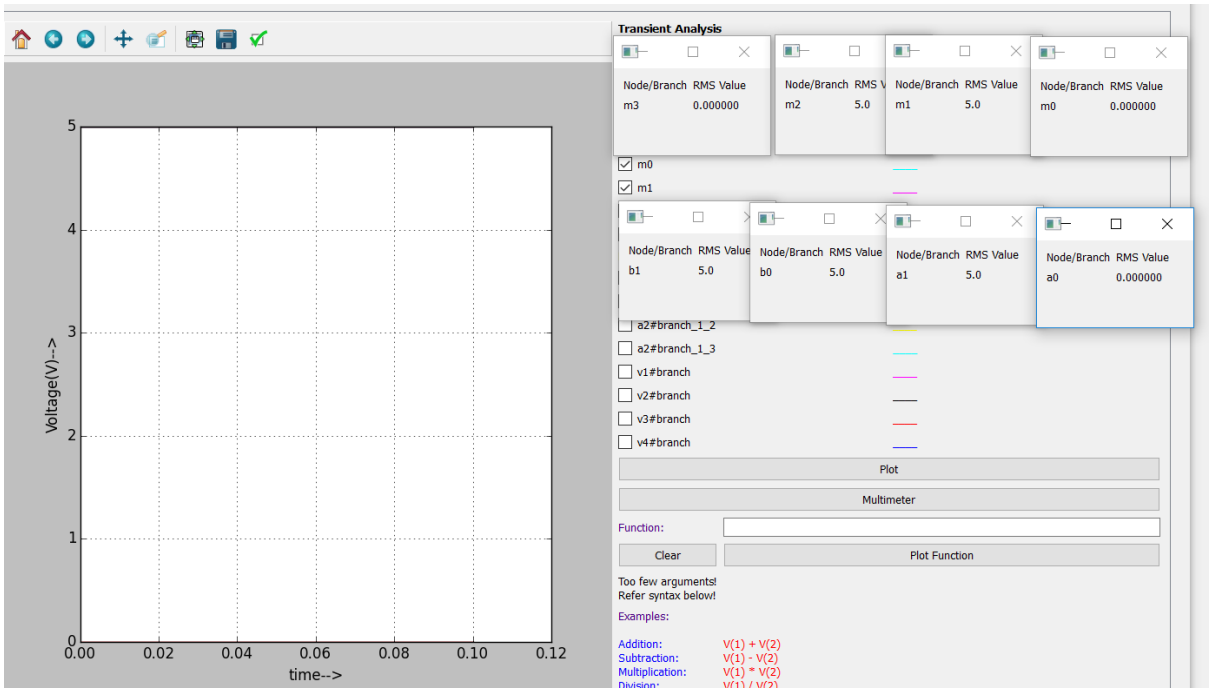





tran1: * c:\users\hp\esim-workspace\mul_test\mul_test.cir
V
v(m2)
5.6
5.4
5.2
5.0
4.8
4.6
4.4
0.0
20.0
40.0
60.0
80.0
100.0
time
ms


tran1: * c:\users\hp\esim-workspace\mul_test\mul_test.cir
V
v(m3)
1.0
0.5
0.0
-0.5
-1.0
0.0
20.0
40.0
60.0
80.0
100.0
time
ms

Python Plot:



References:

https://vlsiuniverse.blogspot.com/2013/05/binary-multiplier.html