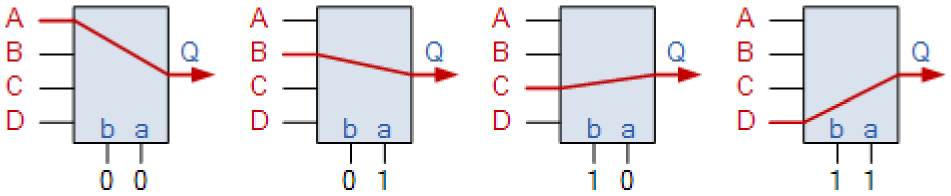
Title:- 74153 A Dual 4 line to 1 line Multiplexer

Theory :-

The multiplexer, shortened to “MUX” or “MPX”, is a combinational logic circuit designed to switch one of several input lines through to a single common output line by the application of a control signal.

The Function of a 4:1 Multiplexer with A,B,C,D as input lines and a,b as select inputs. Output Q is selected among A,B,C,D based on select inputs a,b.



b	a	Q
0	0	A
0	1	B
1	0	C
1	1	D

Here 74153 is a dual 4 to 1 multiplexer with two select inputs (S1,S0) common to both the multiplexers.

a0,a1,a2,a3 are the inputs and Ya is the output , EA is the enable to the MUX1.

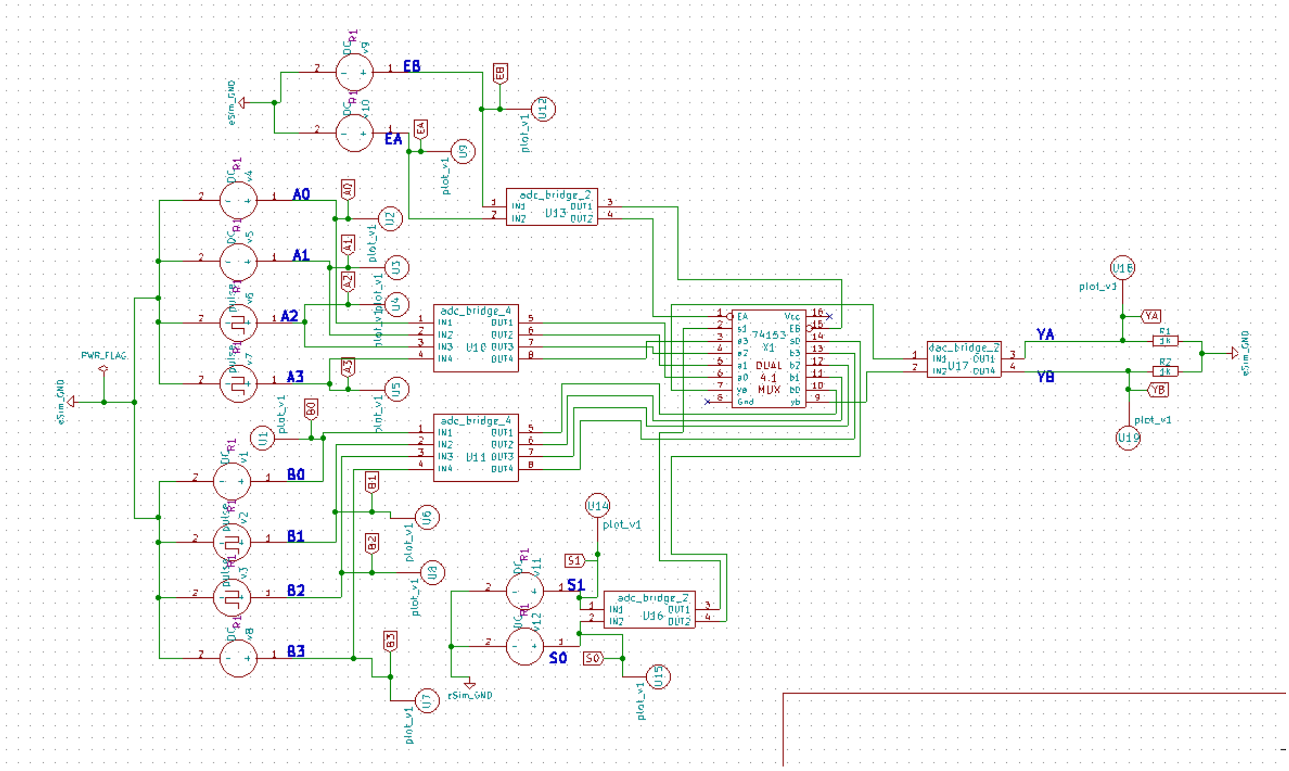
b0,b1,b2,b3 are the inputs and Yb is the output ,EB is the enable to the MUX2.

EA,EB are active low enable inputs.

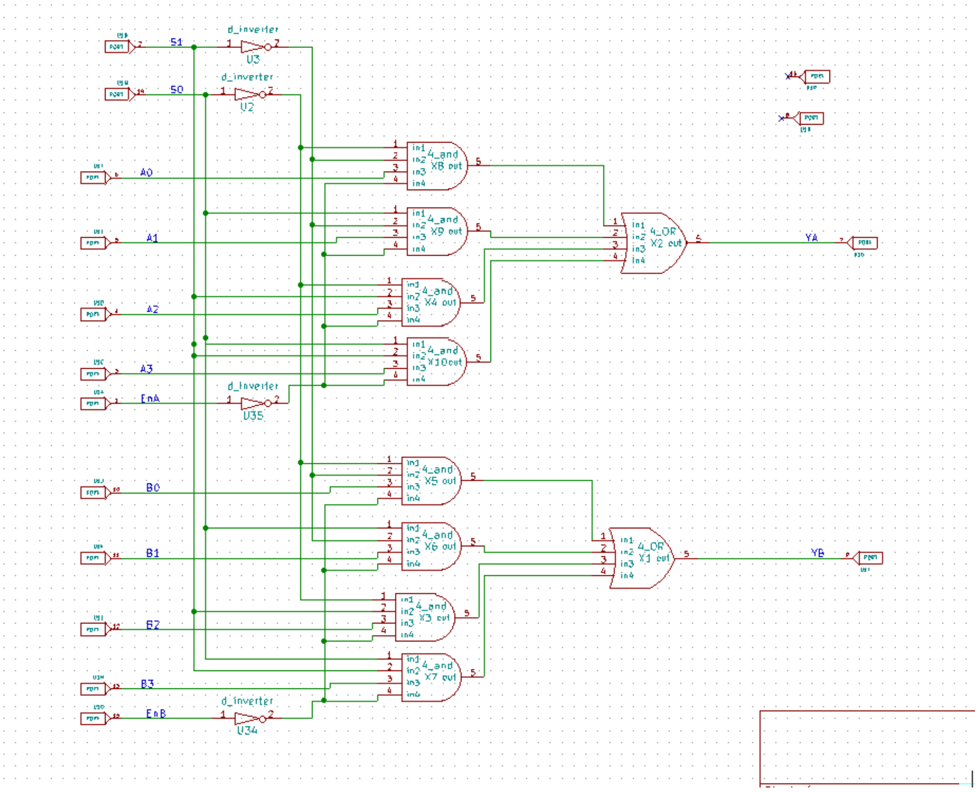
S1	S0	EA	Ya	EB	Yb
x	x	1	0	1	0
0	0	0	a0	0	b0
0	1	0	a1	0	b1
1	0	0	a2	0	b2
1	1	0	a3	0	b3

NOTE :- Here in E-SIM software, no need to connect Vcc(pin 16) and GND (pin 8) pins to Dc source and gnd respectively , you can leave them unconnected using NO CONNECT symbol . This is because in circuit simulation softwares , we use BASIC GATES (AND, NAND etc.) they don’t need Vcc and GND. As in manufacturing an IC , they use MOSFETs to implement those GATES ,there MOSFETs require Vcc and Gnd

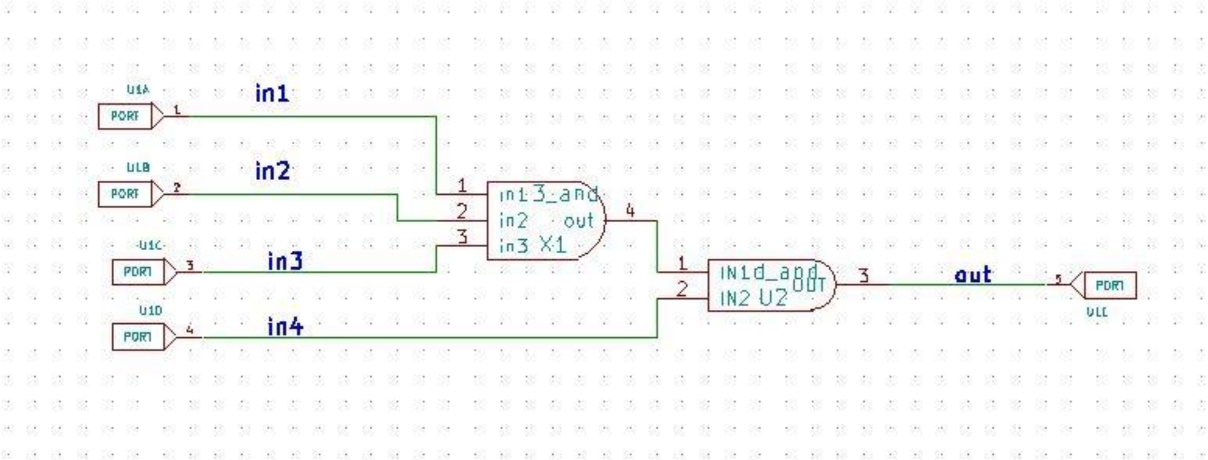
Schematic Diagram :-



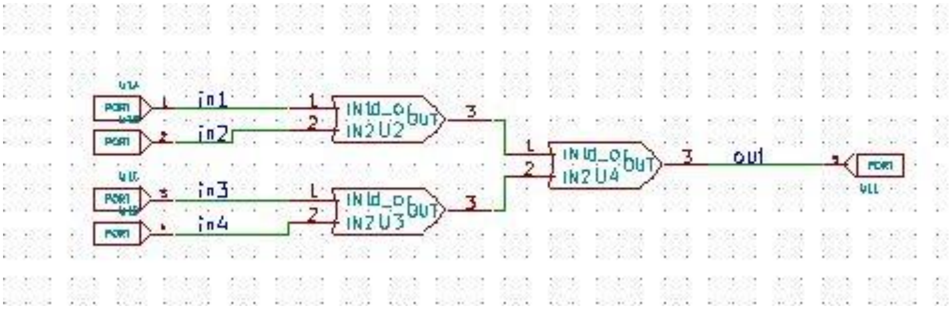
Subcircuit Schematic for 74153 :



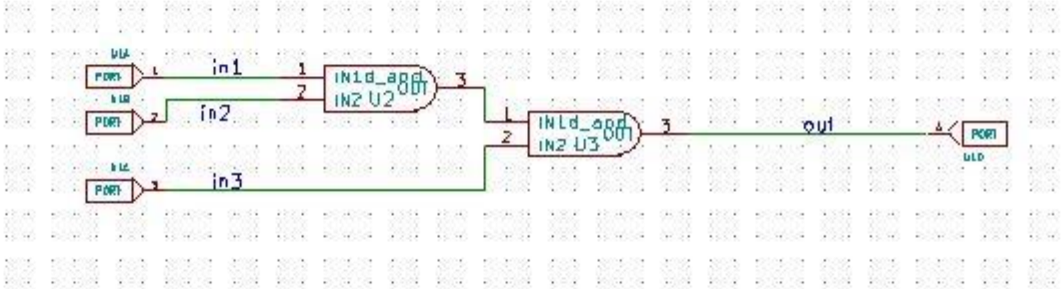
Subcircuit Schematic for ” 4_and” gate used in 74153 subcircuit :



Subcircuit Schematic for ” 4_OR” gate used in 74153 subcircuit :



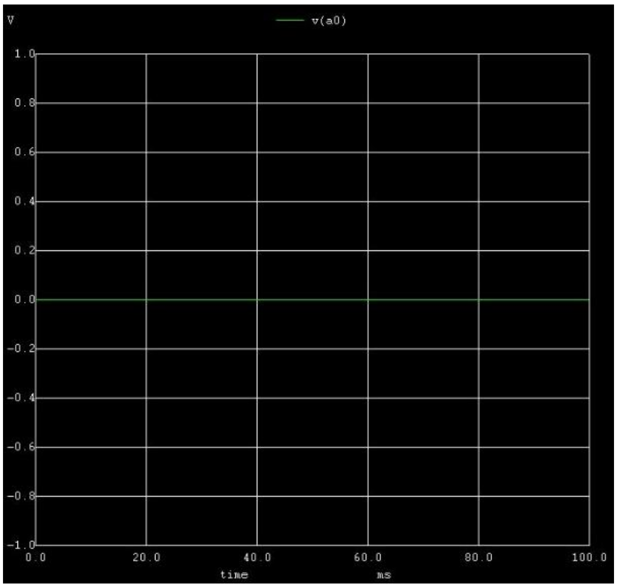
Subcircuit Schematic for ” 3_and” gate used in 4_and gate :



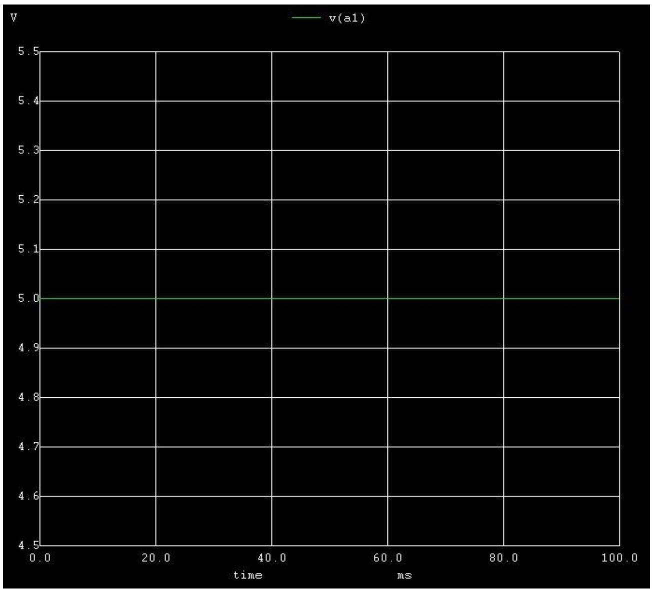
Simulation Results :-   Ngspice plots

Inputs to MUX 1

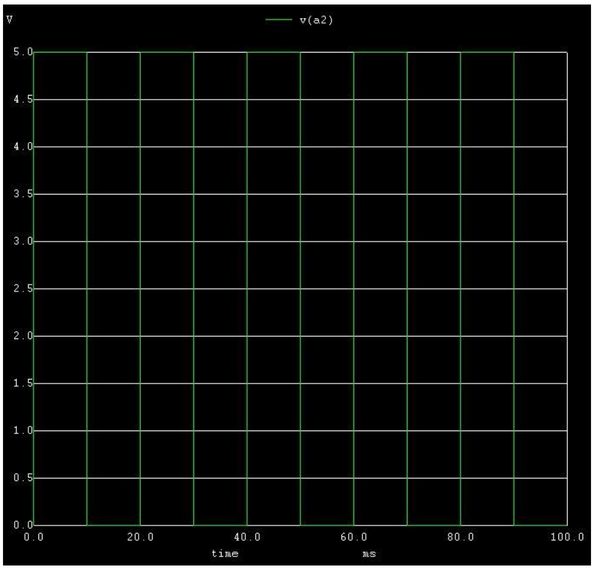
a0(v4)



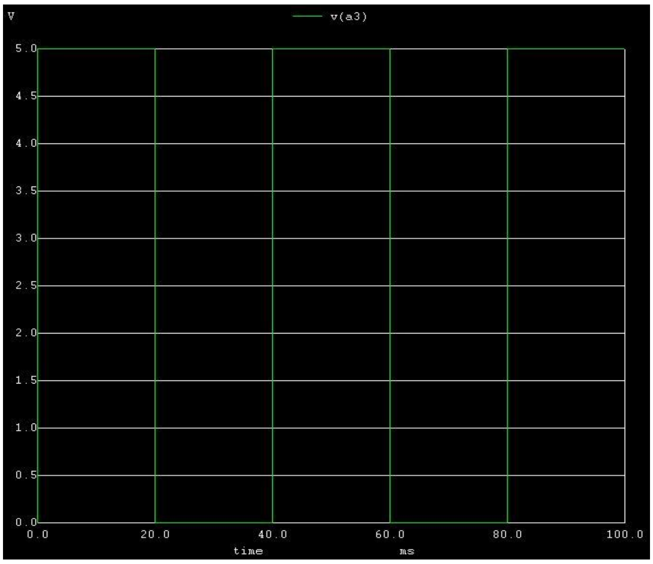
a1(v5)



a2(v6)

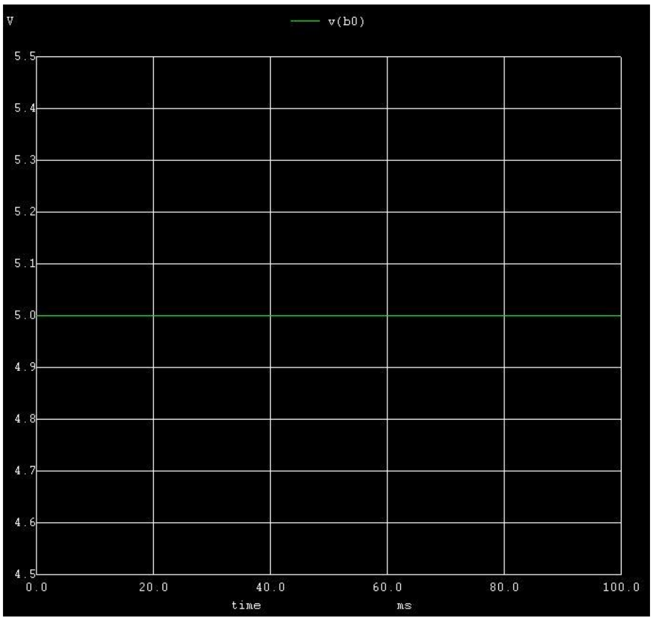


a3(v7)

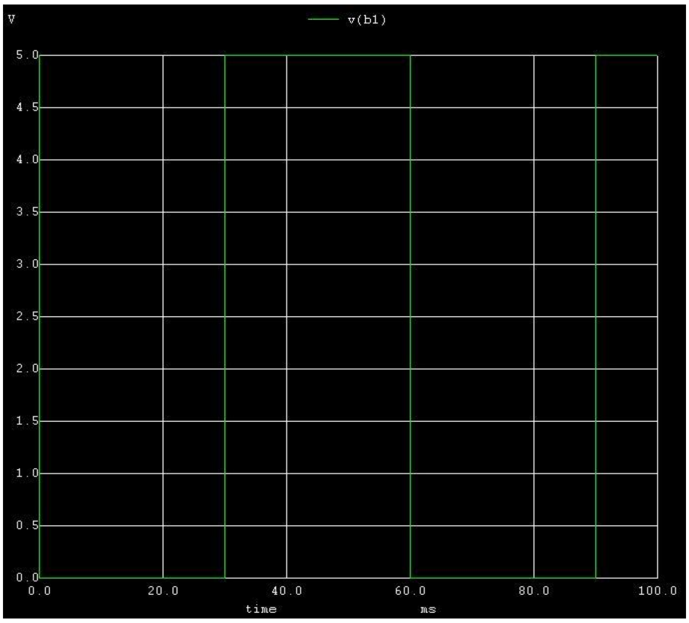


Inputs to MUX 2

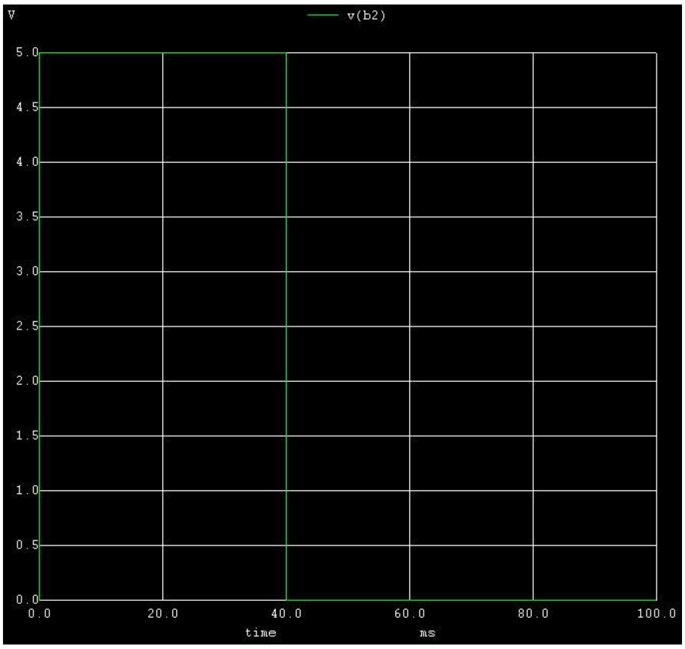
b0(v1   )



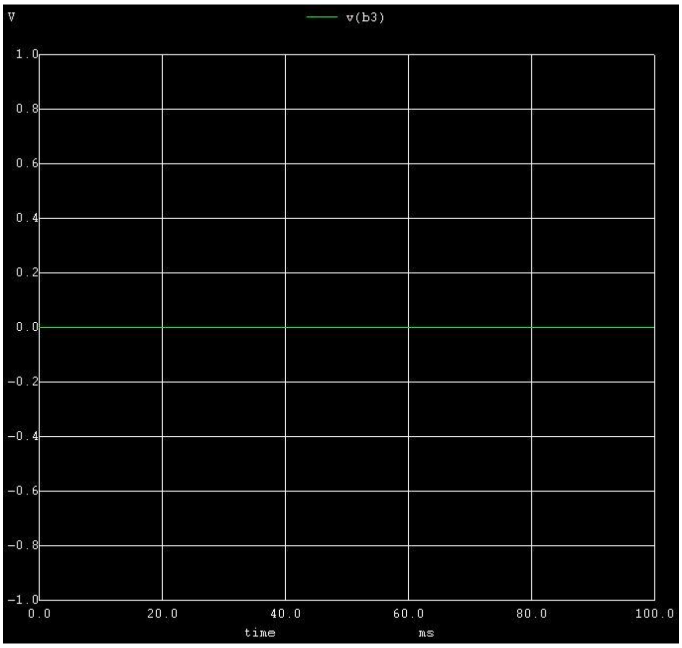
b1(v2)



b2(v3)

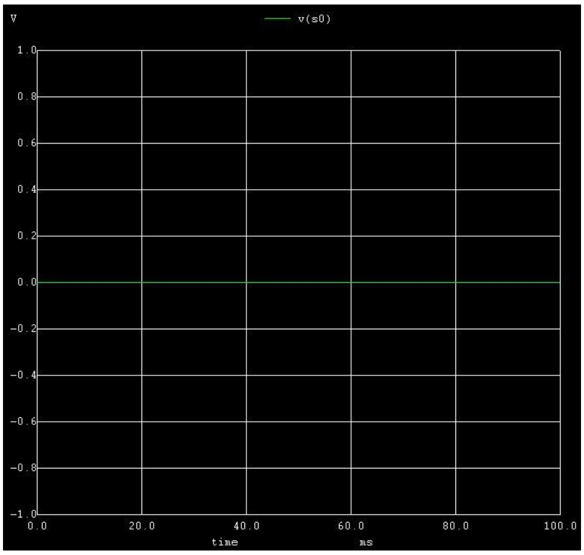


b3(v8)

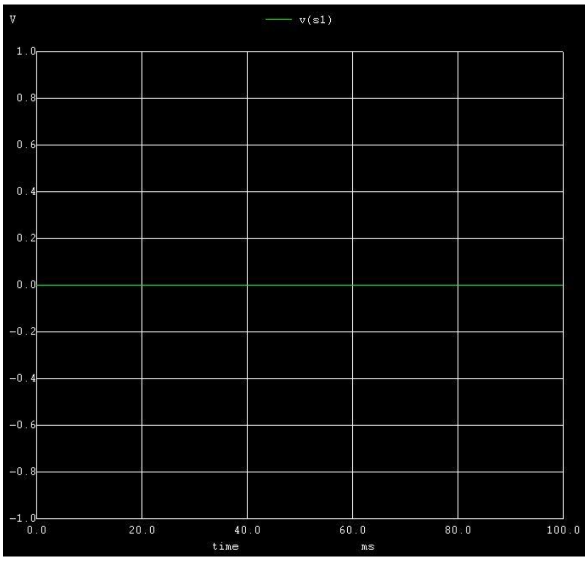


OUTPUTS when s0='0' and s1='0'

s0(v12=0v)



s1(v11=0v)



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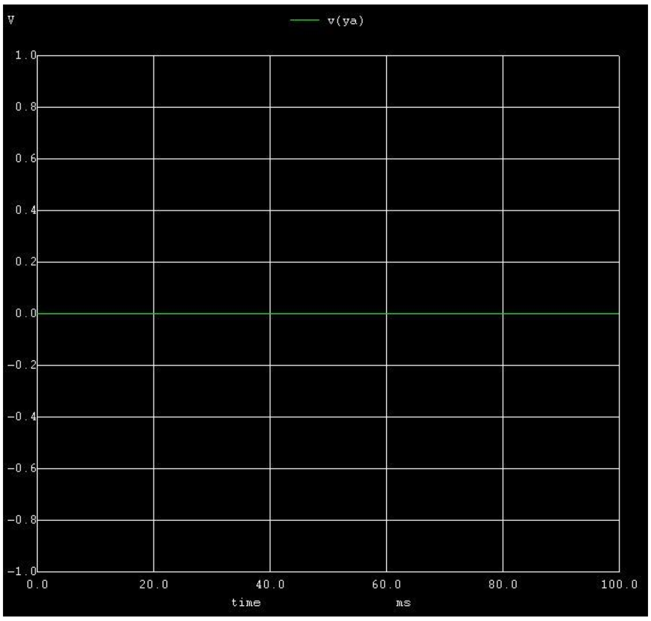
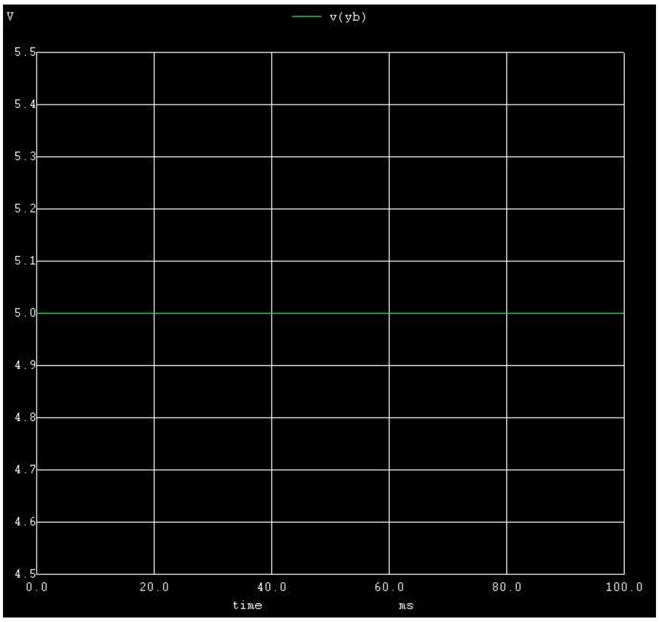
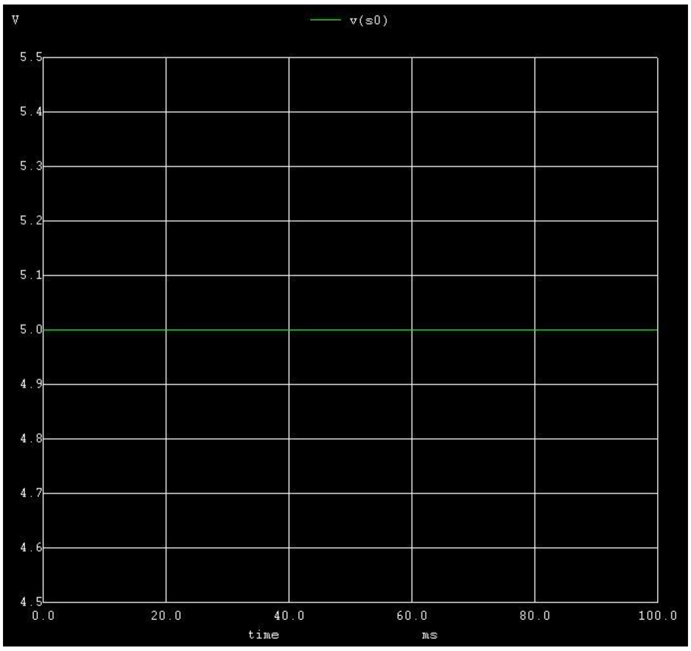


yb

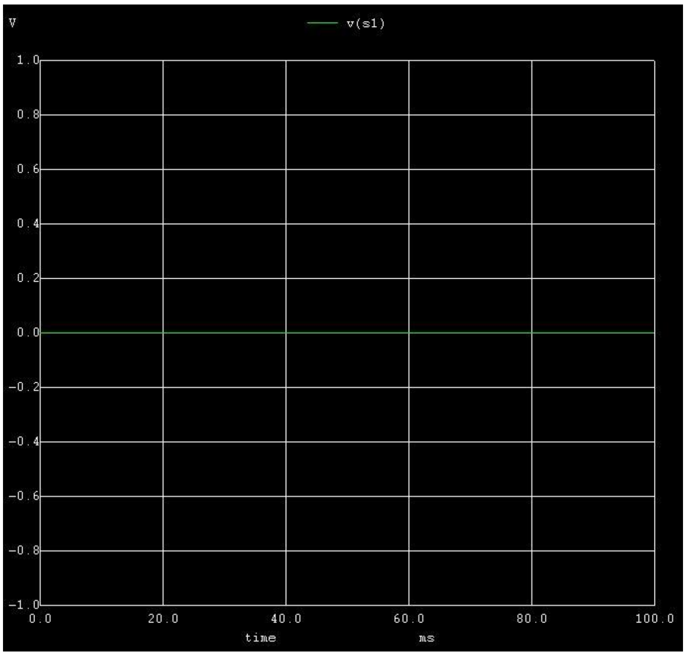


OUTPUTS when s0=’1’ and s1=’0’

s0(v12=5v)



s1(v11=0v)



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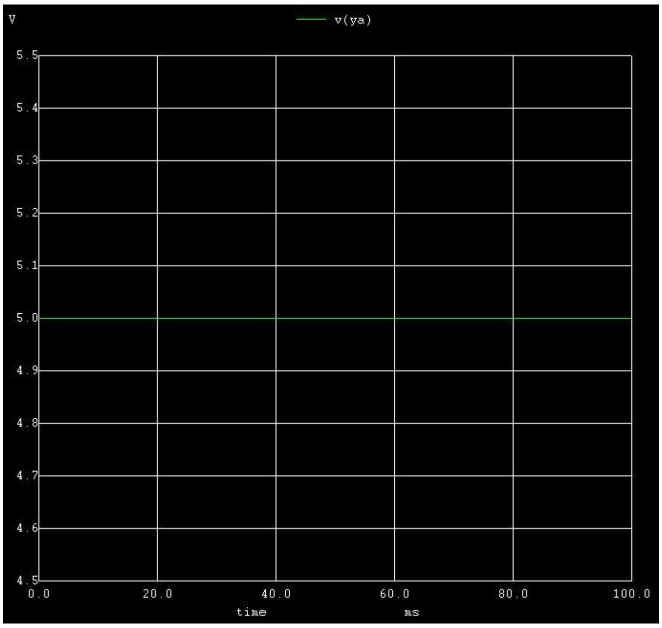

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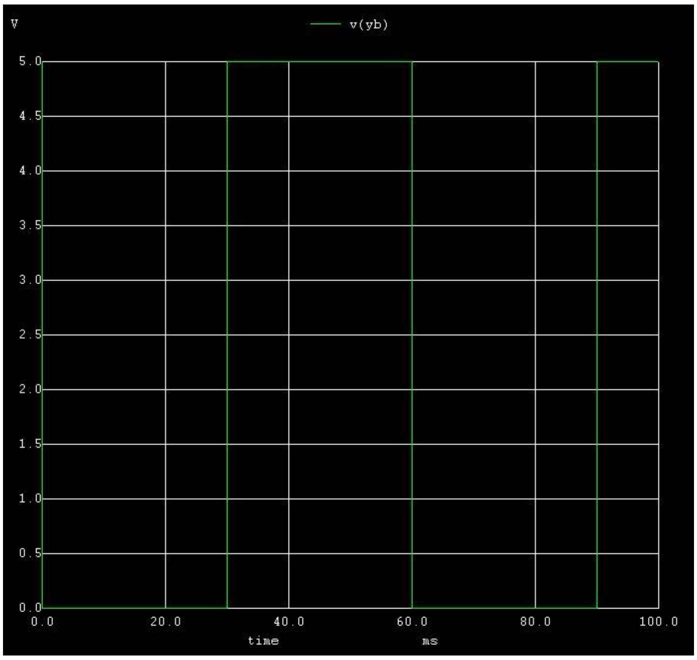
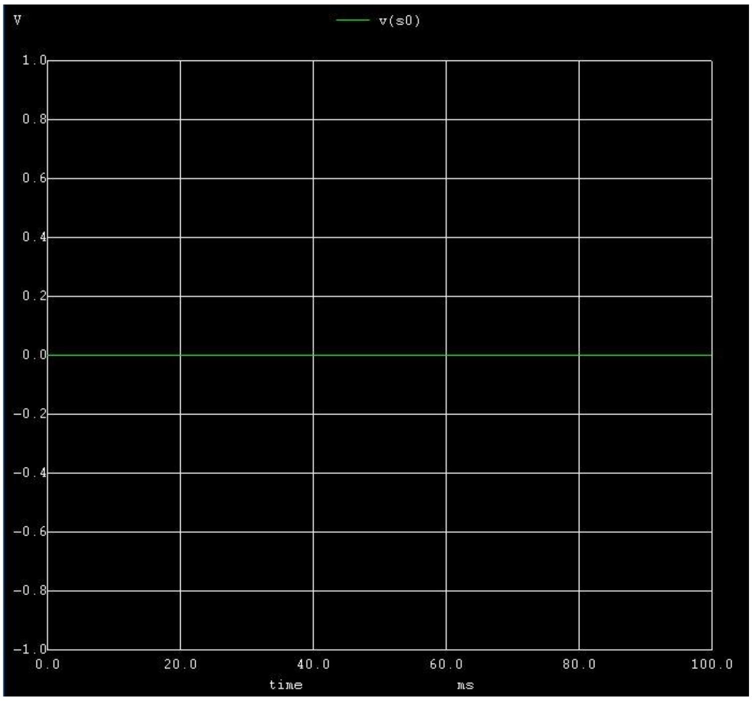
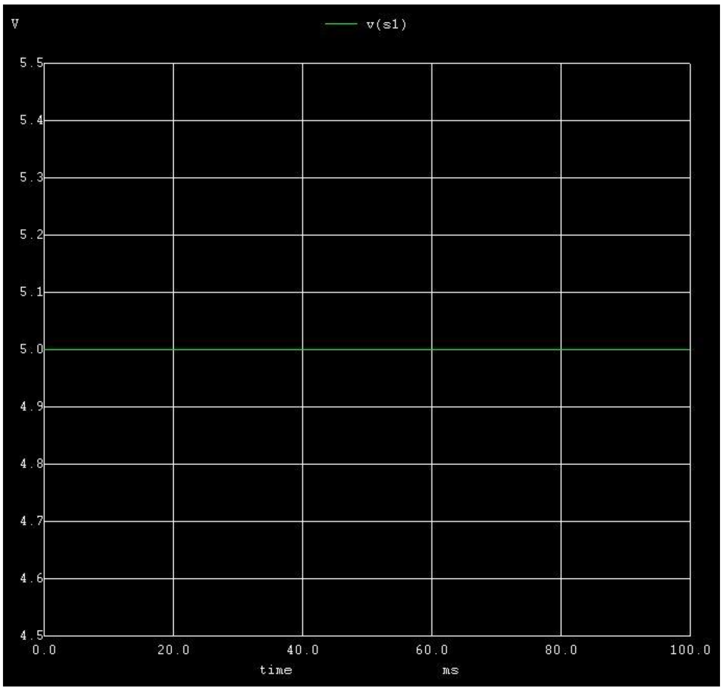


OUTPUTS when s0='0' and s1='1'

s0(v12=0v)



s1(v11=5v)



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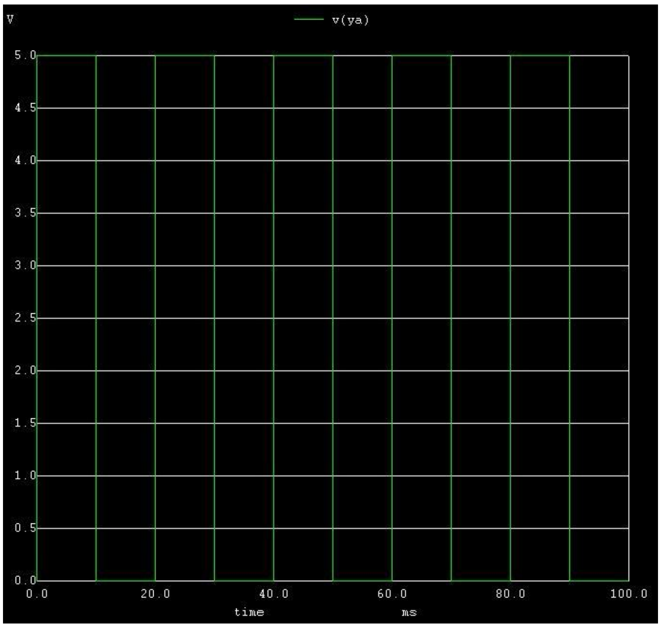

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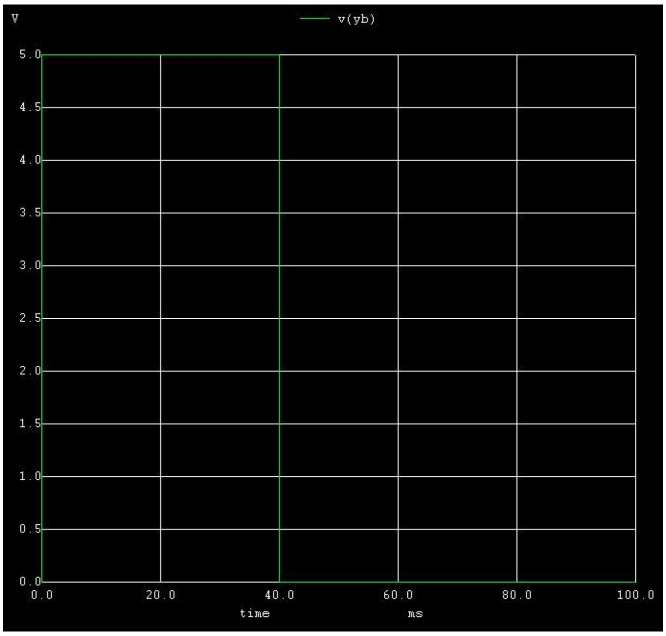
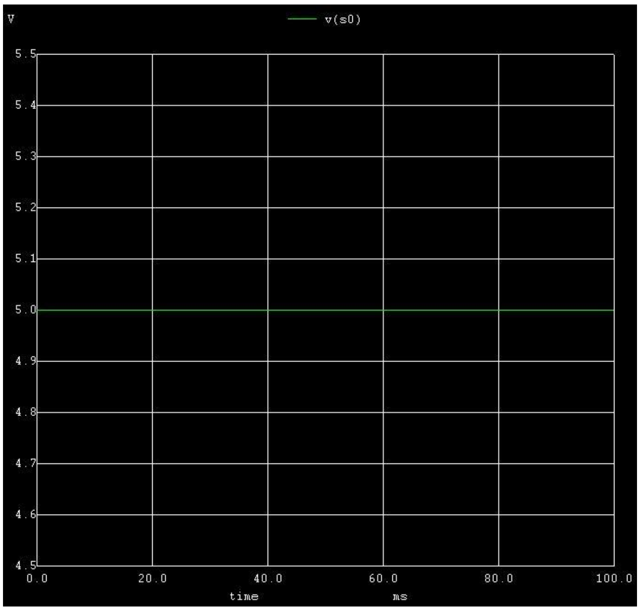
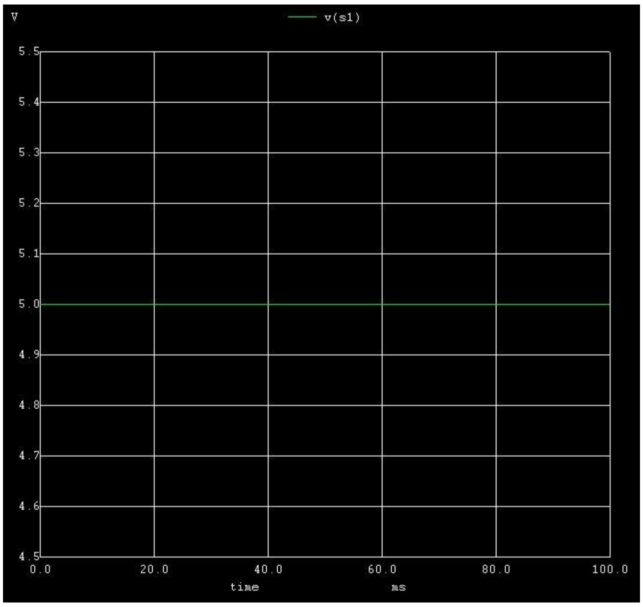


OUTPUTS when s0='1' and s1='1'

s0(v12=5v)



s1(v11=5v)



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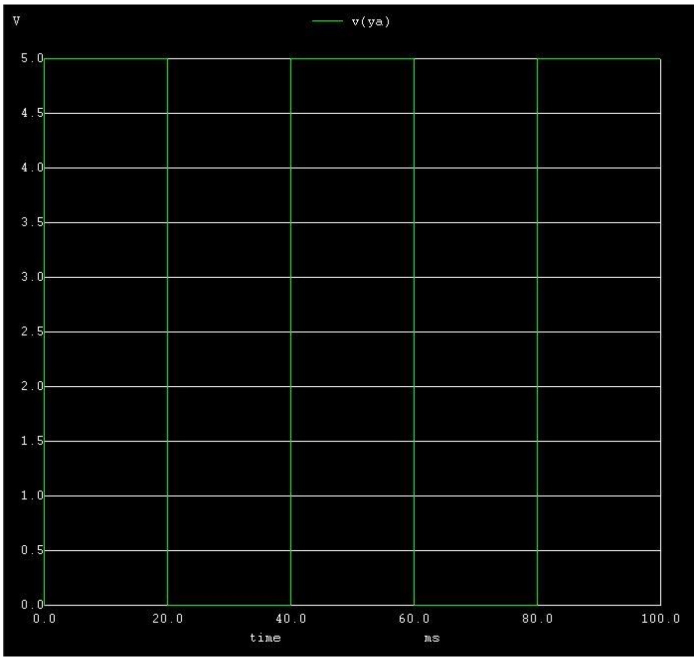

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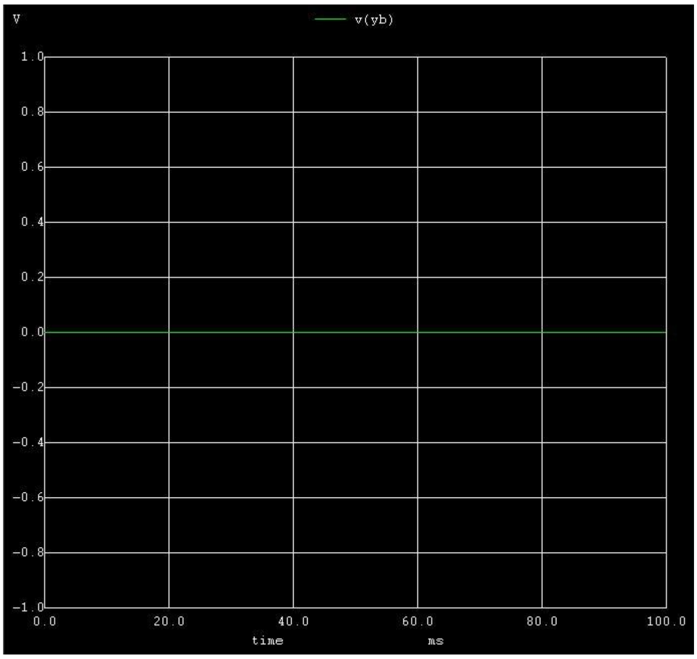
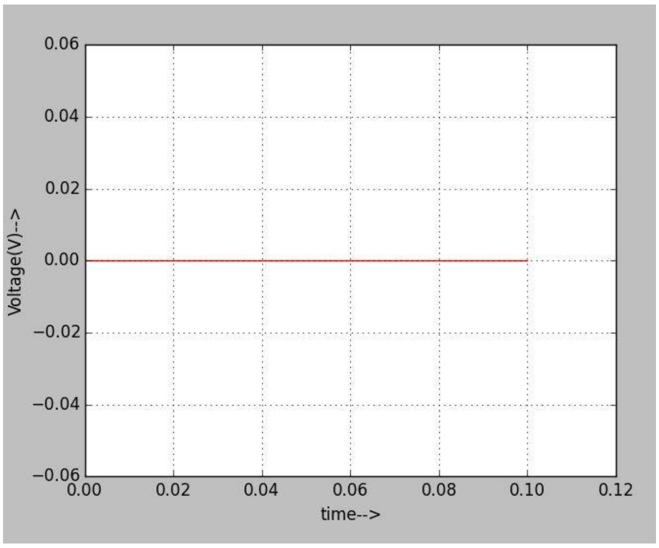


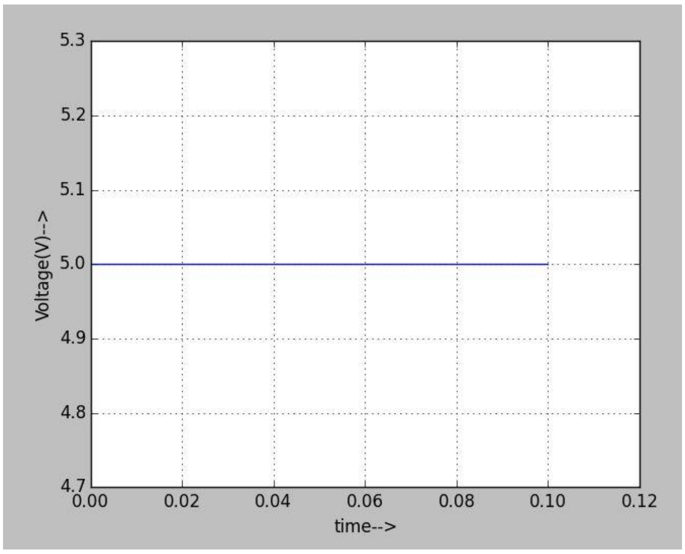
PYTHON PLOTS

Inputs to MUX 1

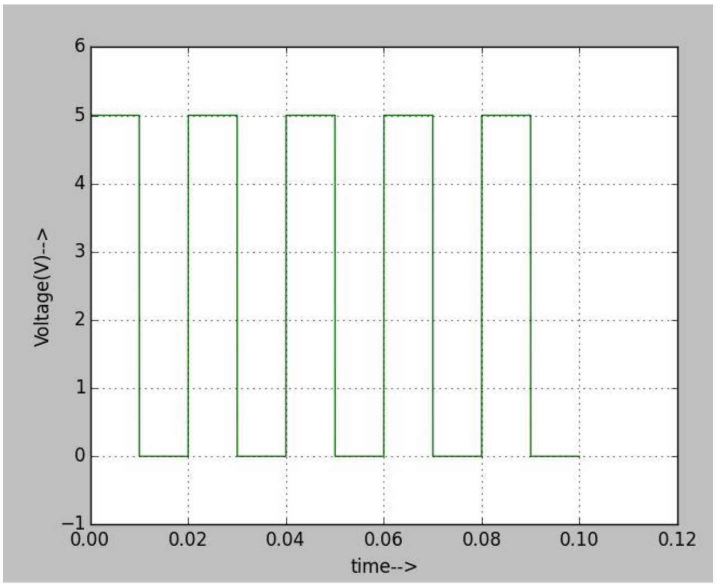
a0(v4)



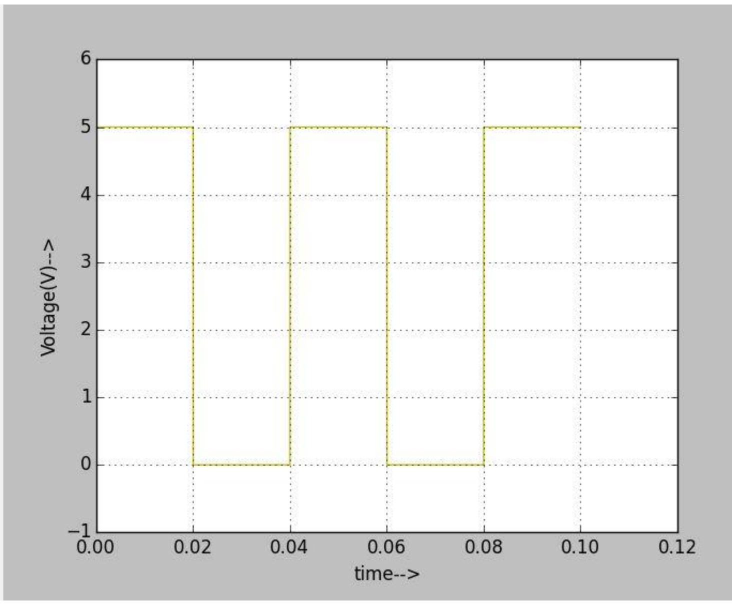
a1(v5)



a2(v6)

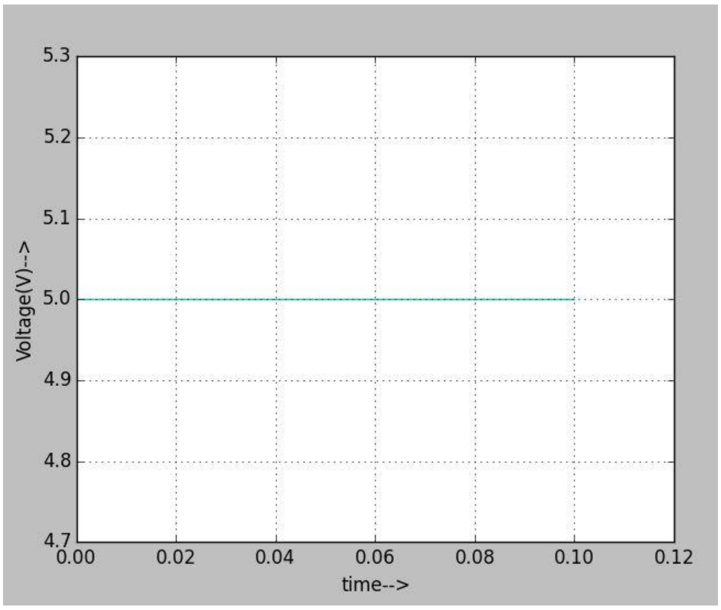


a3(v7)

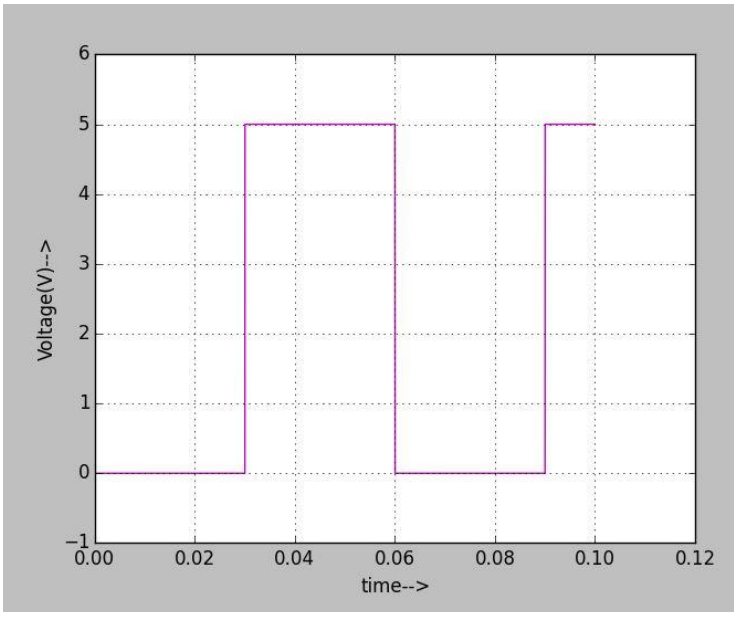


Inputs to MUX 2

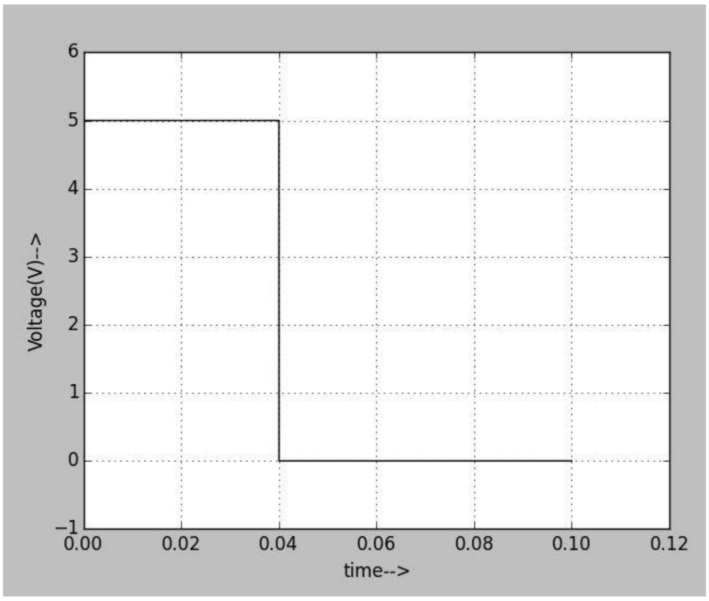
b0(v1)



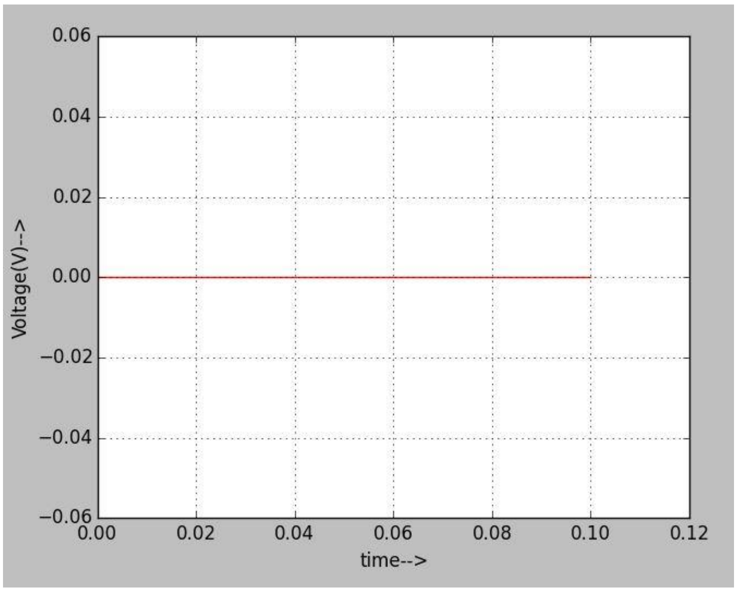
b1(v2)



b2 (v3)

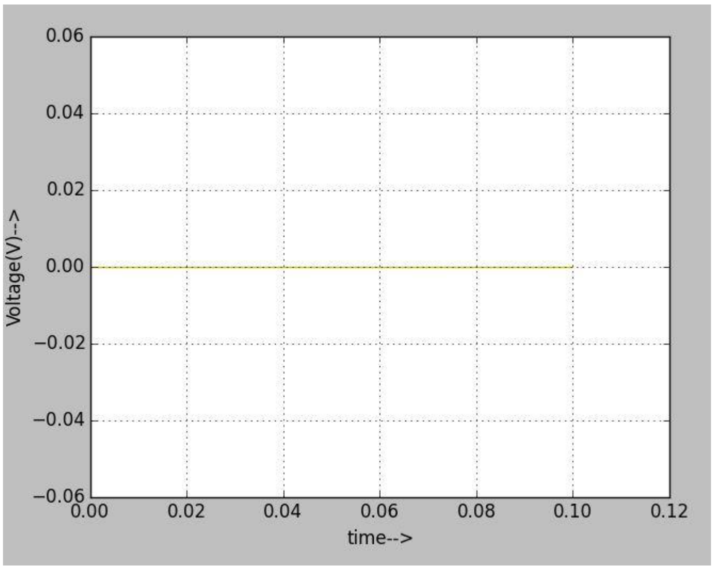


b3 (v8)

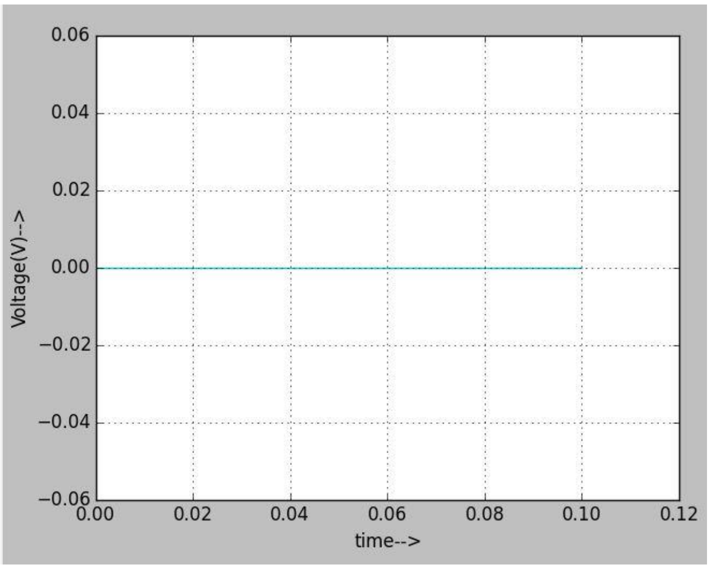


OUTPUTS when s0='0' and s1='0'

s0(v12=0v)



s1(v11=0v)



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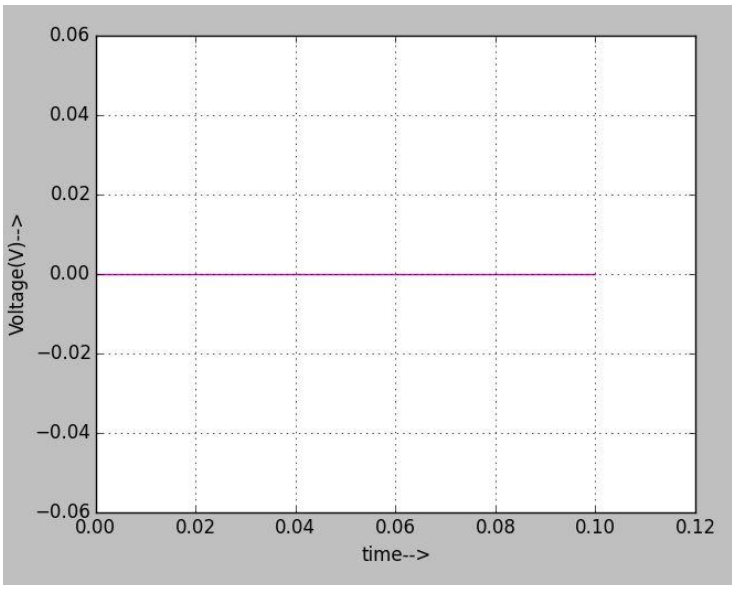

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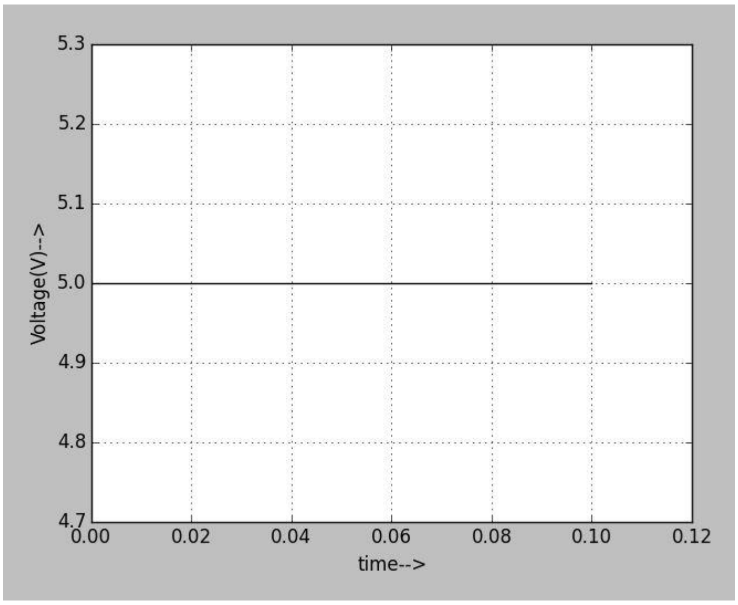
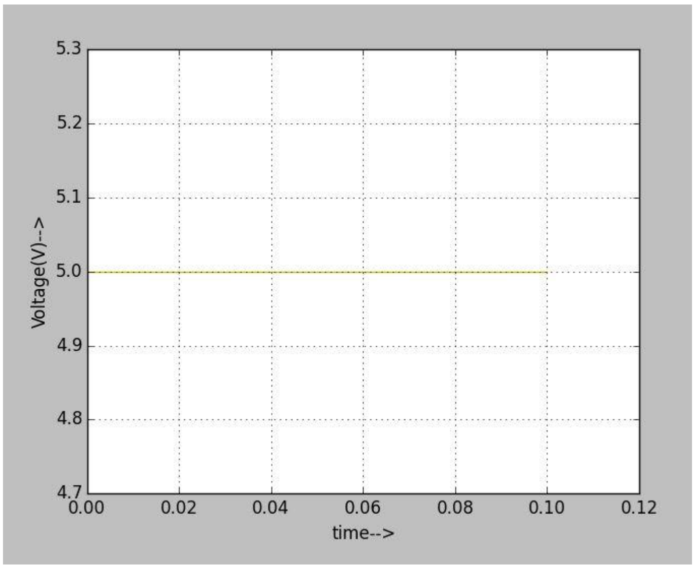


OUTPUTS when s0='0' and s1='1'

s0(v12=5v)



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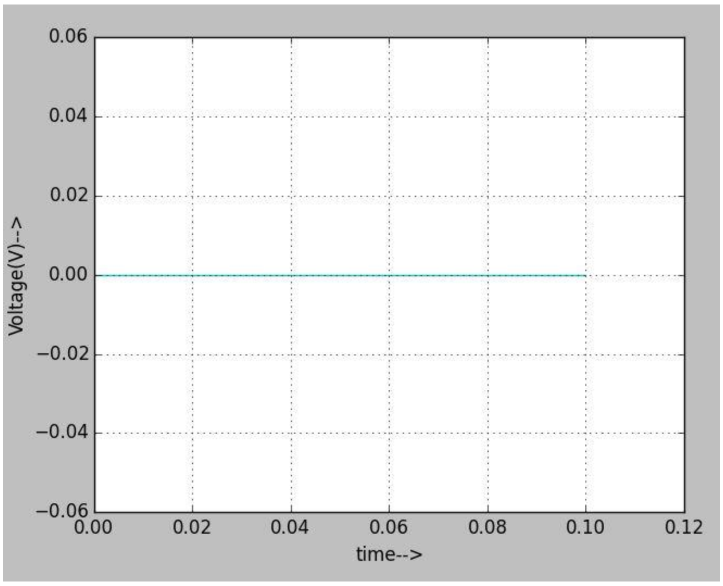

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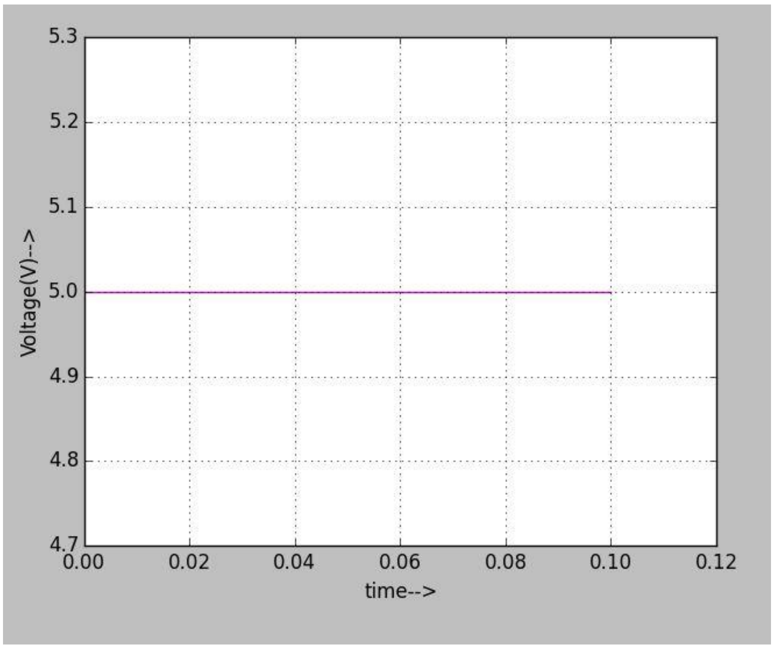

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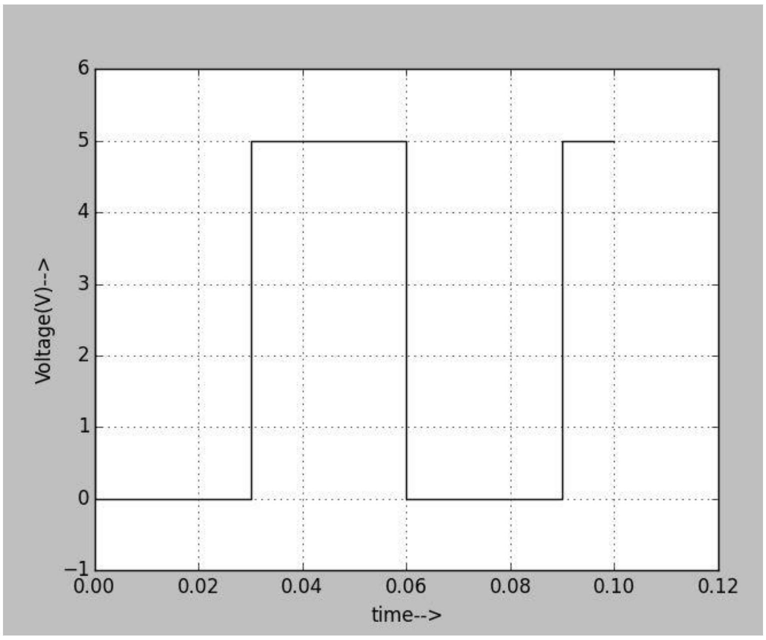
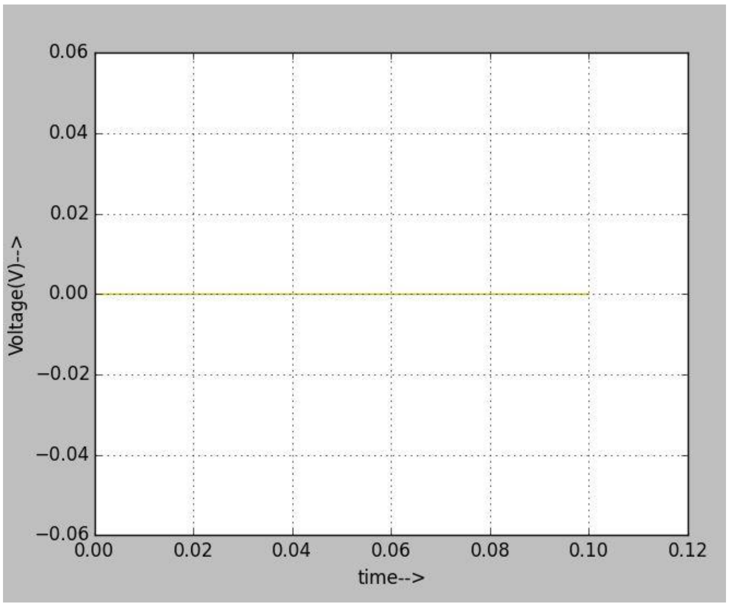


OUTPUTS when s0='0' and s1='1'

s0(v12=0v)



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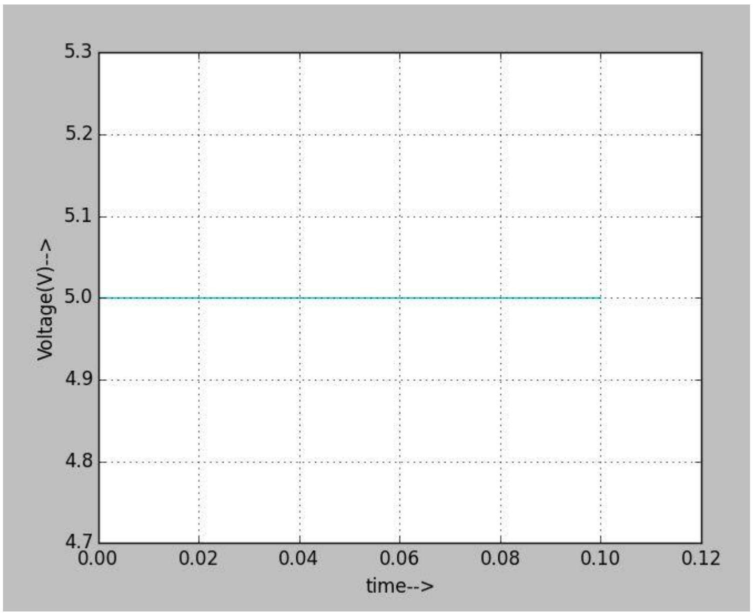

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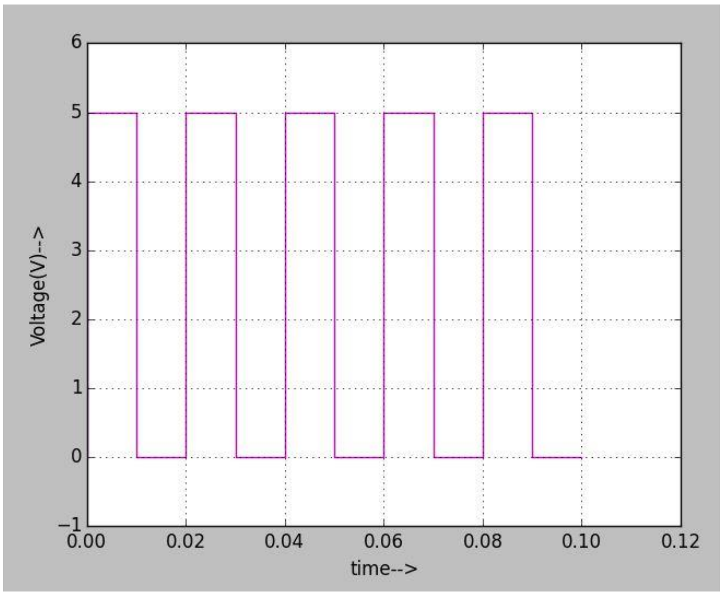

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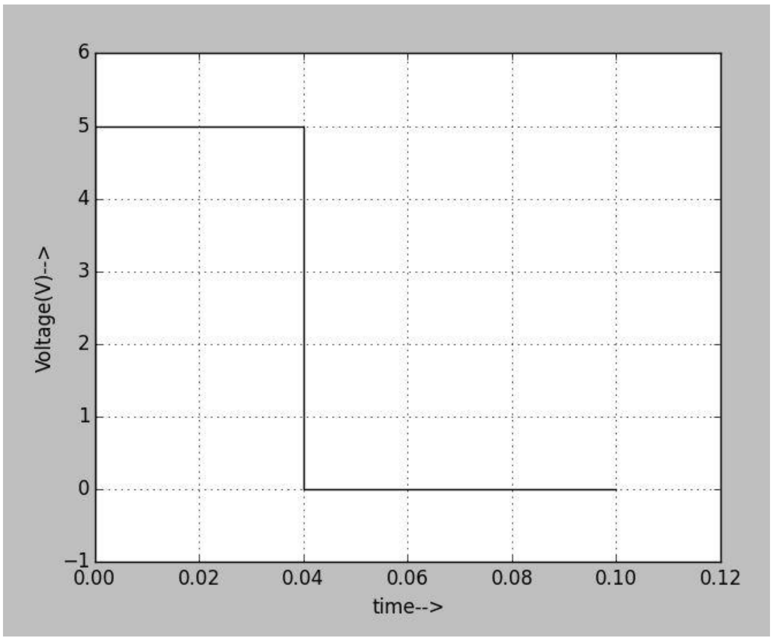
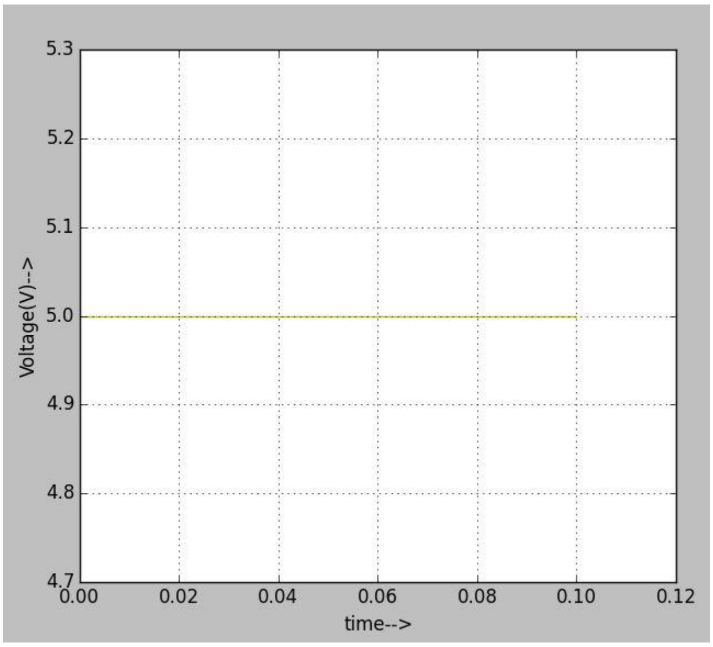


OUTPUTS when s0='1' and s1='1'

s0(v12=5v)



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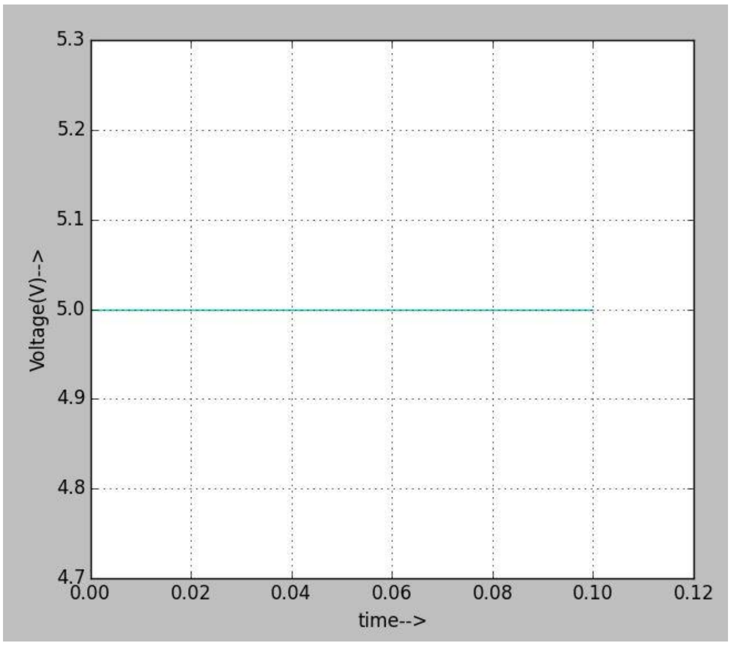

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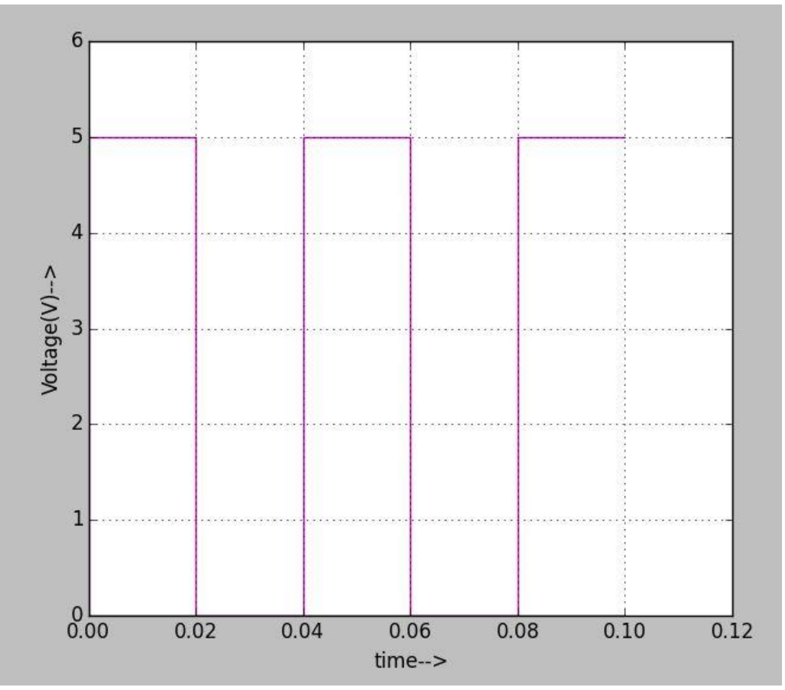

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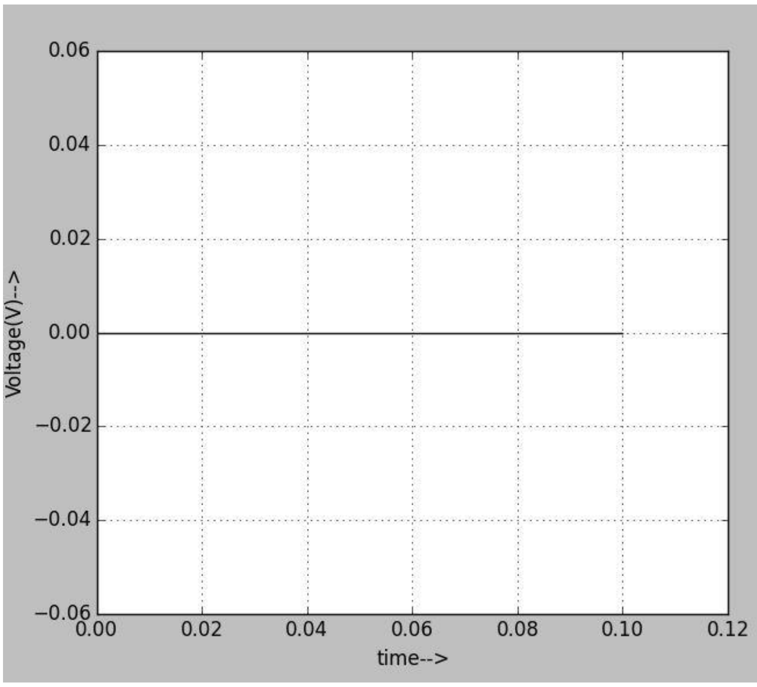

REFERENCES:-

1) https://www.electronicshub.org/multiplexerandmultiplexing/

2)https://www.ti.com/lit/ds/symlink/sn74ls153.pdf