RTL NOR Gate Design and Simulation

Atin Mukherjee, Lecturer, Dr.B.C.Roy Polytechnic
Debesh Choudhury, Founder, Infosensys Research & Engineering

1 Theory:

In this project, a two-input universal RTL NOR gate is designed and simulated using the eSim EDA tool. The behaviour of NOR gate is very simple, output goes to HIGH (logic '1') state when all the applied input signals are in LOW (logic '0') state and for other combinations of input signals, output goes to LOW (logic '0') state. For the RTL NOR circuit, BJTs are connected in parallel combinations. The collector of all the transistors are tied with collector supply voltage (V_{cc}) through a collector resistor (R_c) and emitters are directly connected with the ground. The base of every transistors are connected with the different applied Input voltage through base resistor (R_b).For the LOW input signal, BJT goes to the cut-off state and for the HIGH input signal, BJT goes to a saturation state. Table.1 shows the truth table of NOR gate.

Input		Output
V(a)	V(b)	V(Out)
0	0	1
0	1	0
1	0	0
1	1	0

Table 1: Truth Table of NOR Gate

2 Schematic Diagram:

The schematic diagram of two input RTL NOR gate in eSim is as shown below:

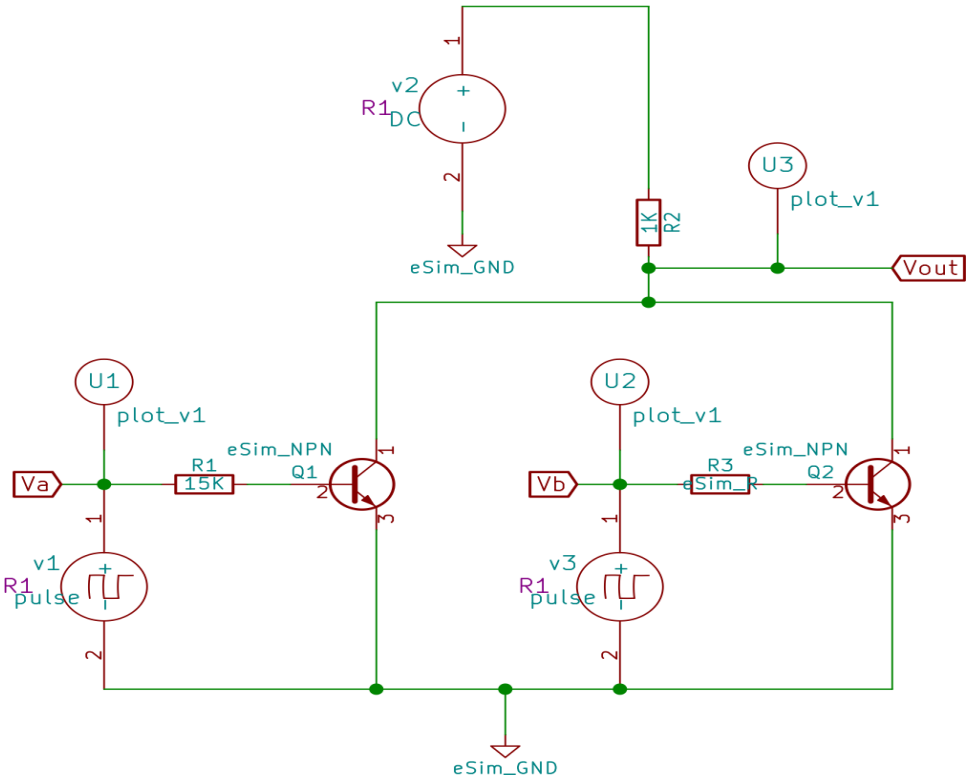

Figure 1: Schematic Diagram of RTL NOR Gate

3 Simulation Results

3.1 NgSpice Plots

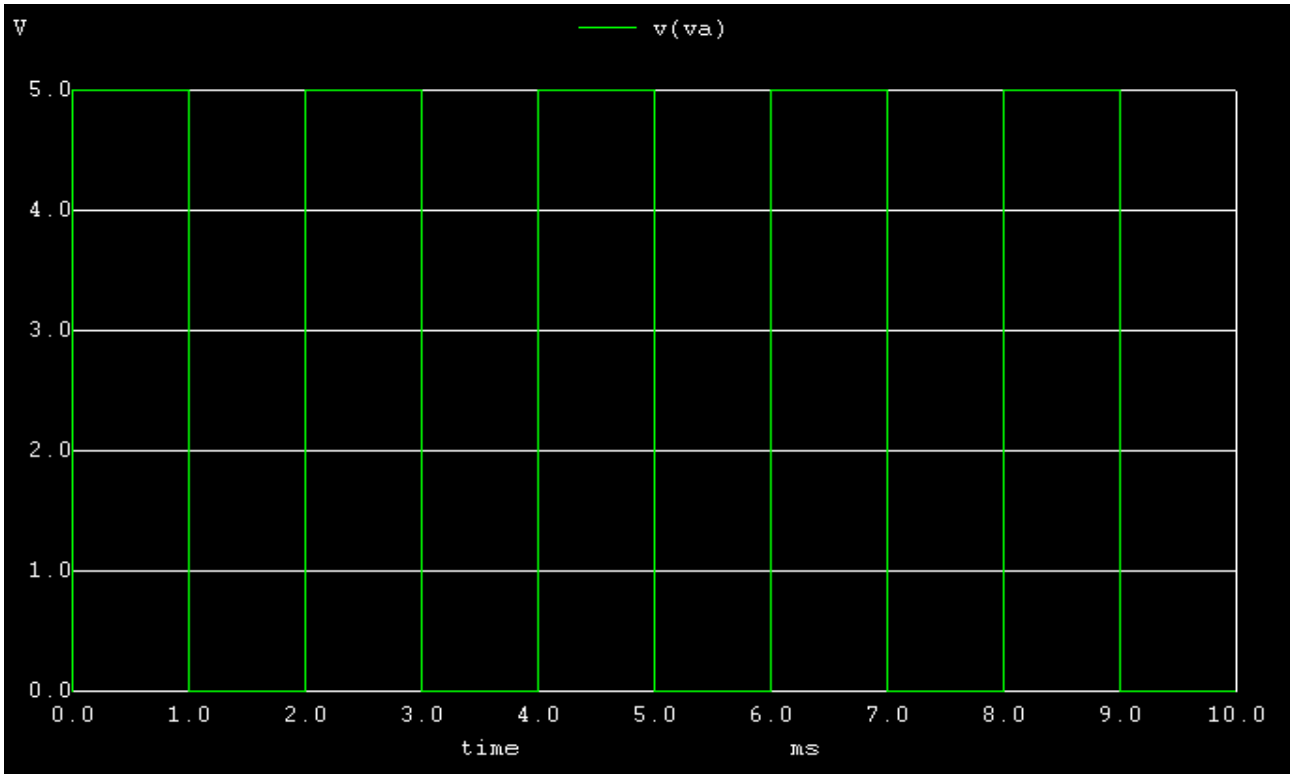

Figure 2: NgSpice Plot of Input Signal V(a)

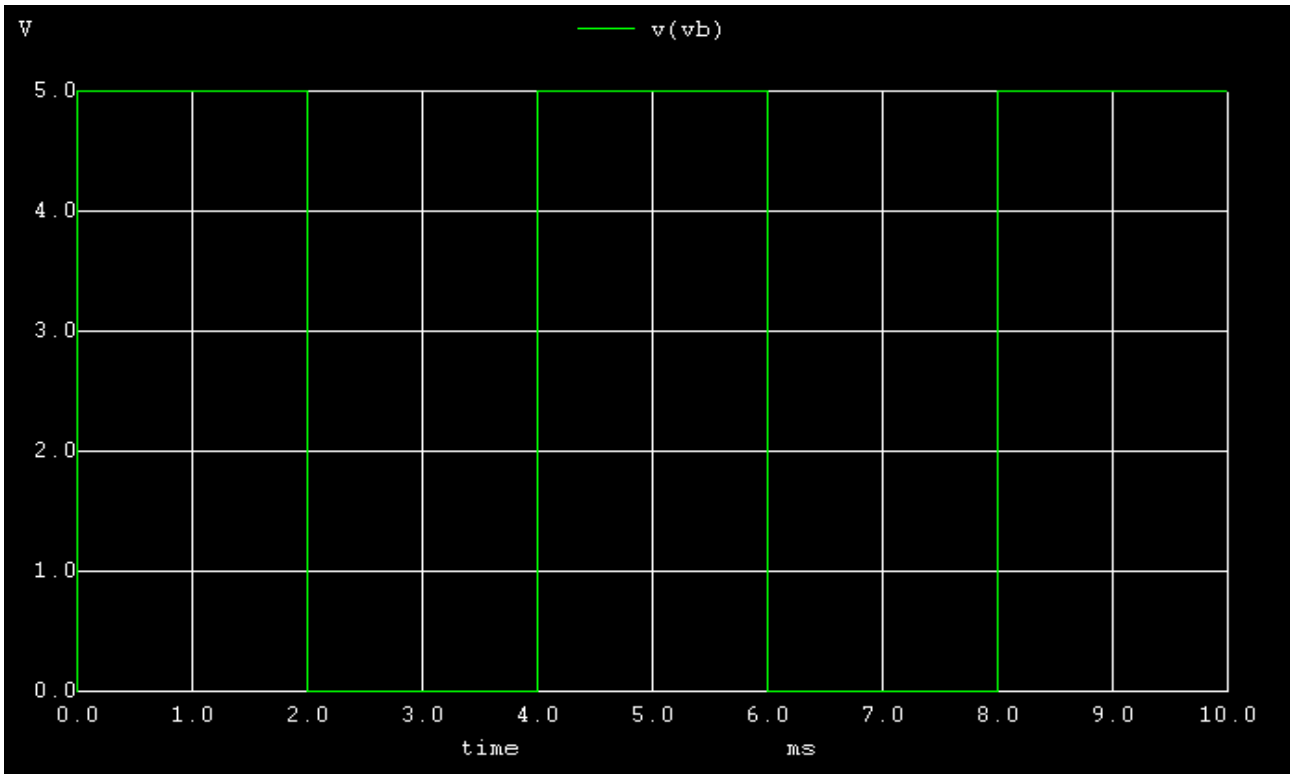

Figure 3: NgSpice Plot of Input Signal V(b)

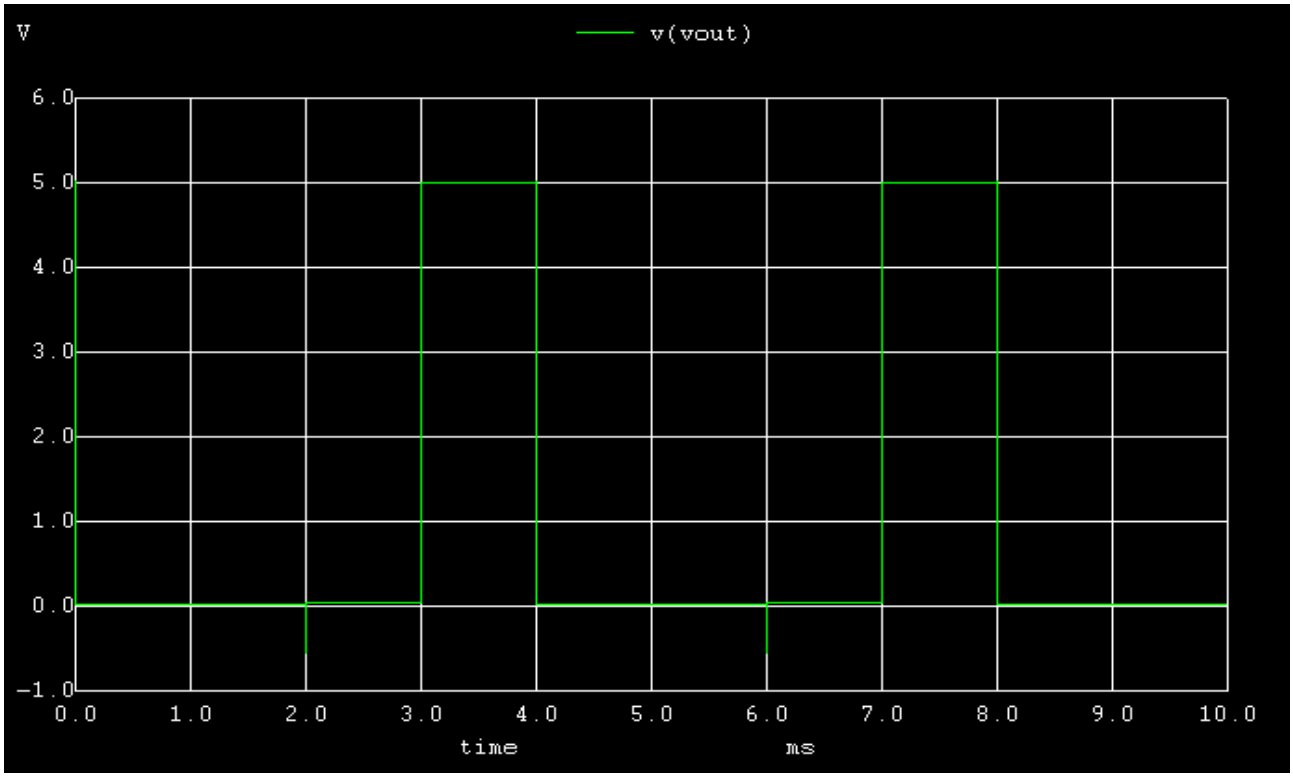

Figure 4: NgSpice Plot of Output Signal V(Out)

3.2 Python Plots

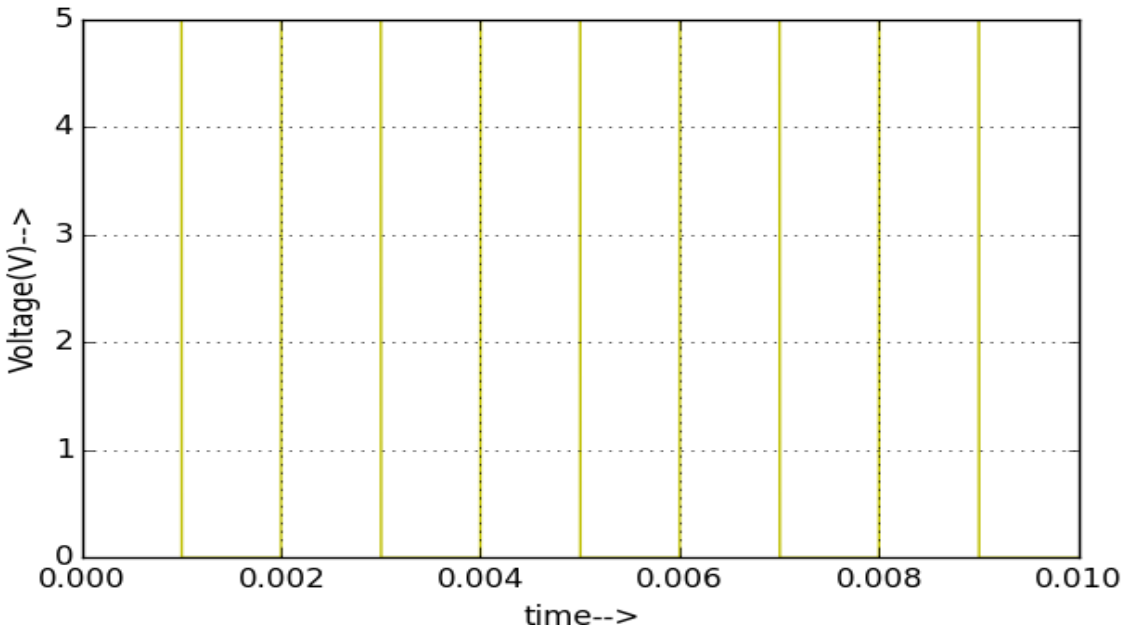

Figure 5: Python Plot of Input Signal V(a)

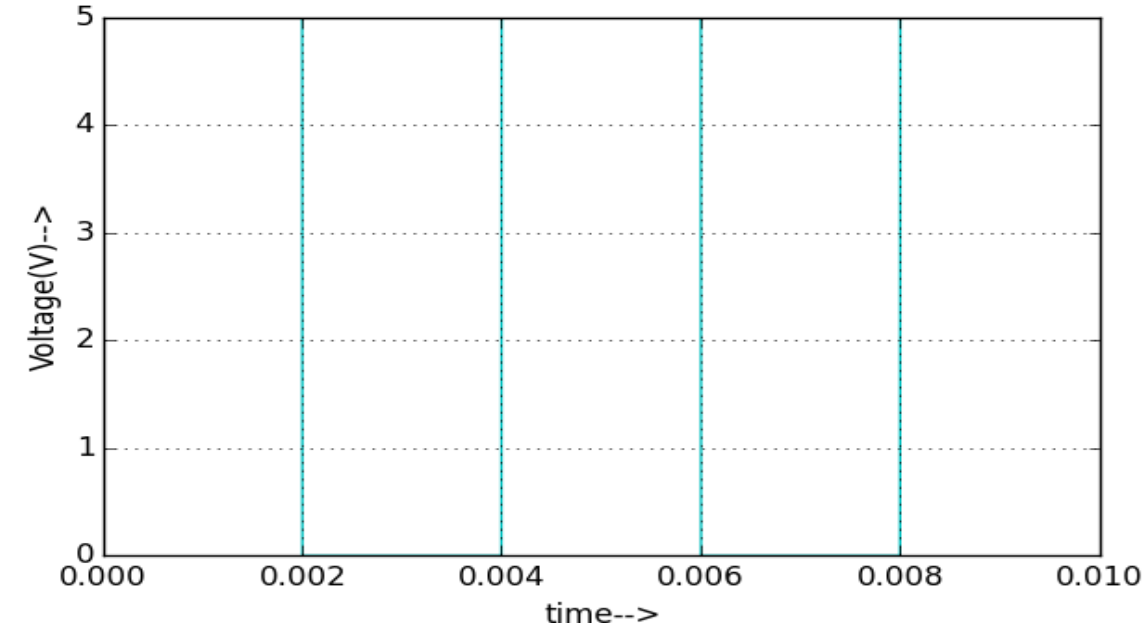

Figure 6: Python Plot of Input Signal V(b)

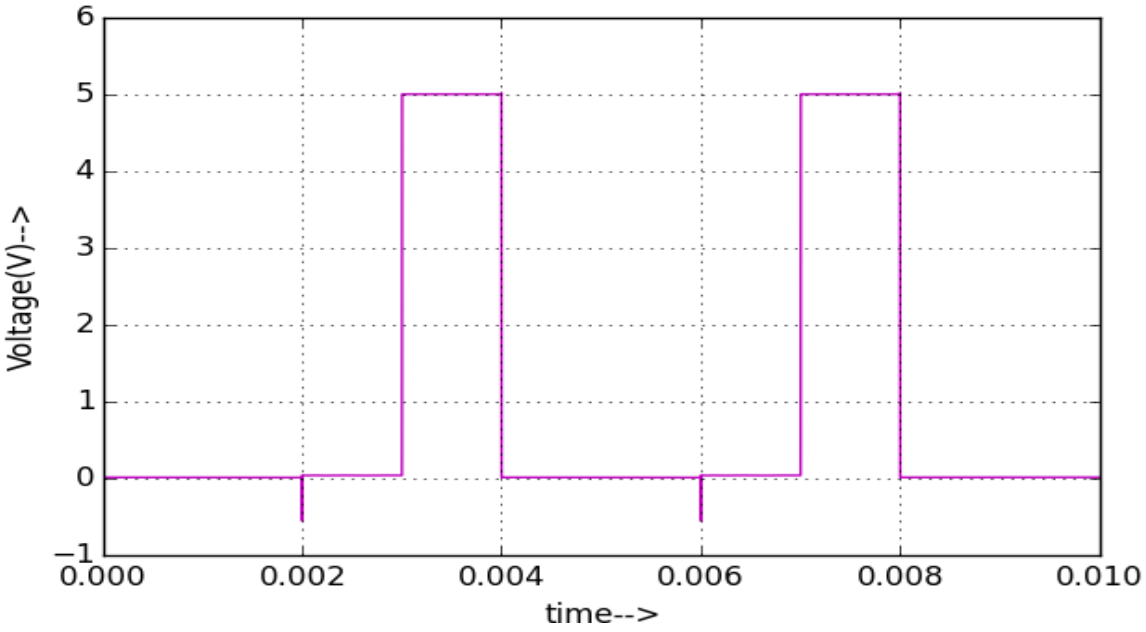

Figure 7: Python Plot of Output Signal V(Out)

4 Conclusion:

Thus, we have studied the transient response of the RTL NOR gate using eSim and we get the appropriate waveforms.

5 References:

https://www.electronics-tutorials.ws/logic/logic_6.html