RTL NAND Gate Design and Simulation

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1 Theory:

In this project, a two-input universal RTL NAND gate is designed and simulated using the eSim EDA tool. The behaviour of NAND gate is very simple, output goes to LOW (logic '0') state when all the applied input signals are in HIGH (logic '1') state and for other combinations of input signals, output goes to HIGH (logic '1') state. Output voltage level for HIGH state is almost equal to collector supply voltage V_{cc} and for LOW output state, the voltage level is equal to collector-emitter voltage (V_{ce}). For the RTL NAND circuit, BJTs are connected in series combinations. The emitter of the first transistor is directly connected with the collector of the next transistor and the emitter of the last transistor is connected to the ground. The collector of the first transistor is tied with the collector supply voltage (V_{cc}) through a collector resistor R_c. For the N number of inputs emitter of first transistor is connected with the collector supply and emitter of Nth number of transistor is connected with ground. The base of every transistor is connected to the different applied Input voltage through base resistor R_b. For the LOW input signal, BJT goes to the cut-off state and for the HIGH input signal, BJT goes to a saturation state.

2 Schematic Diagram:

The schematic diagram of two input RTL NAND gate in eSim is as shown below:

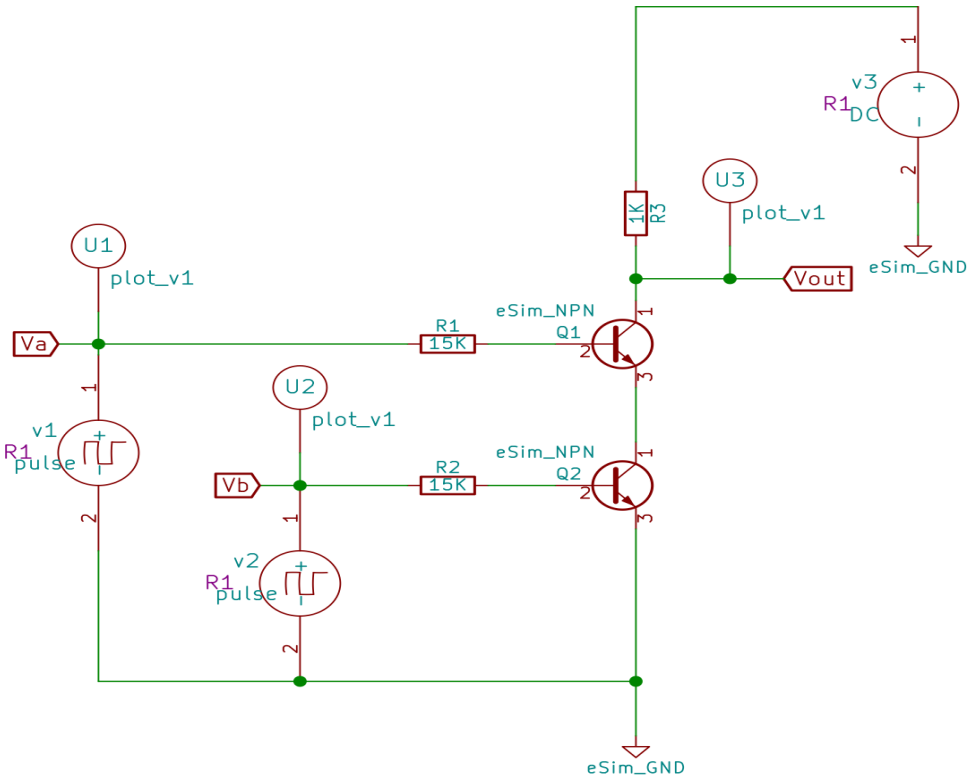

Figure 1: Schematic Diagram of RTL NAND Gate

3 Simulation Results

3.1 NgSpice Plots

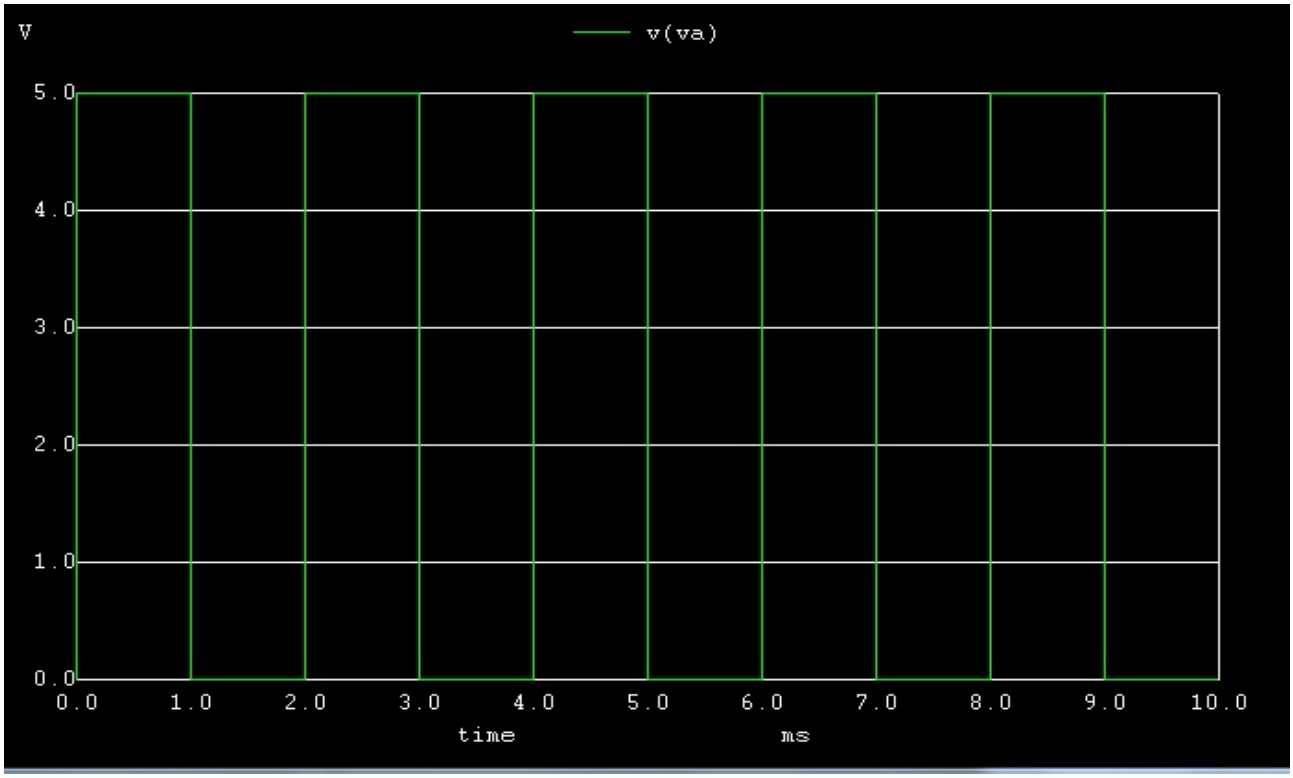

Figure 2: NgSpice Plot of Input Signal V(a)

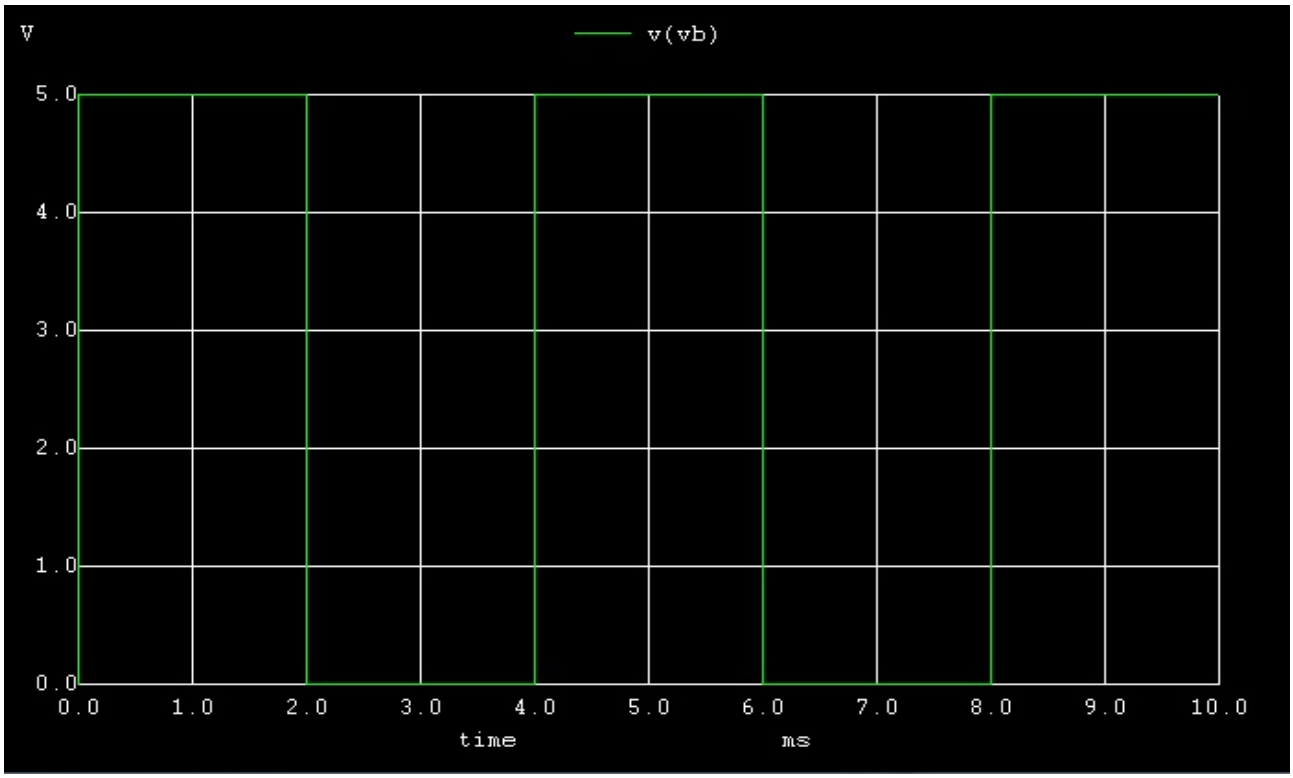

Figure 3: NgSpice Plot of Input Signal V(b)

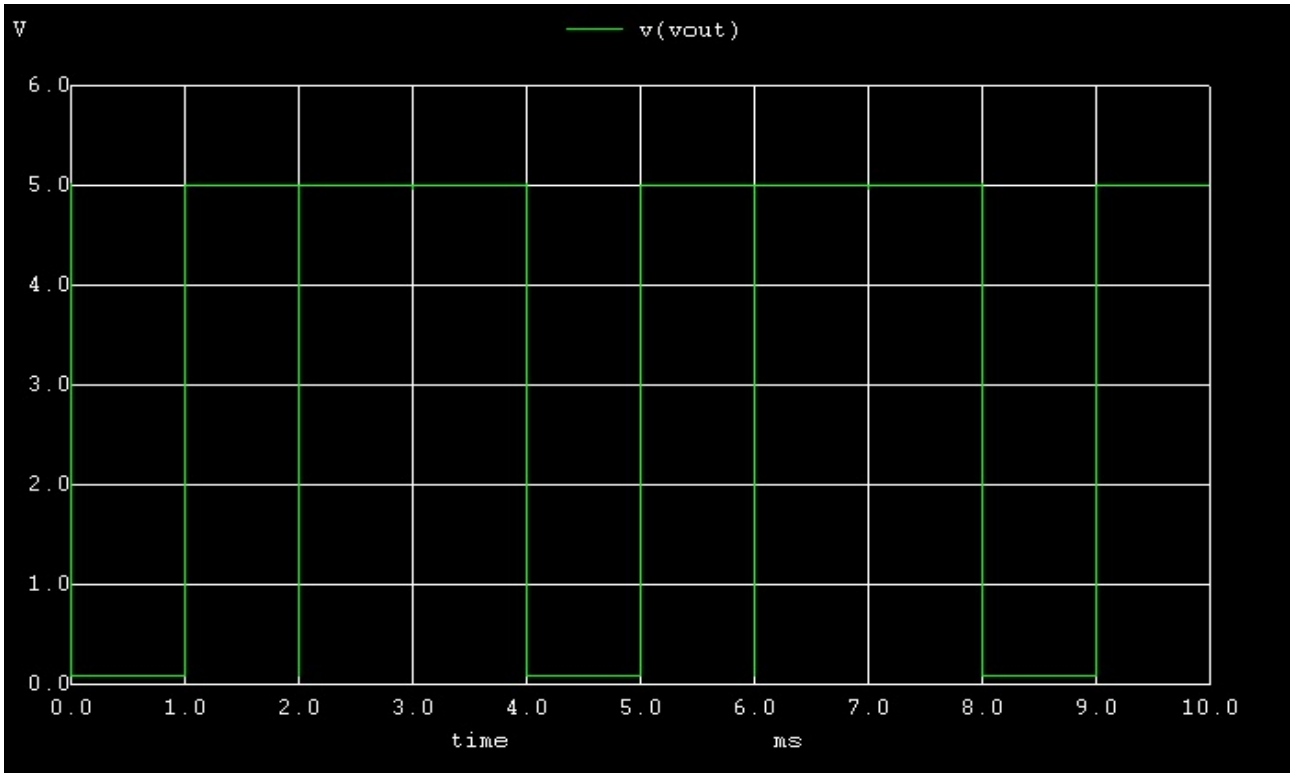

Figure 4: NgSpice Plot of Output Signal V(Out)

3.2 Python Plots

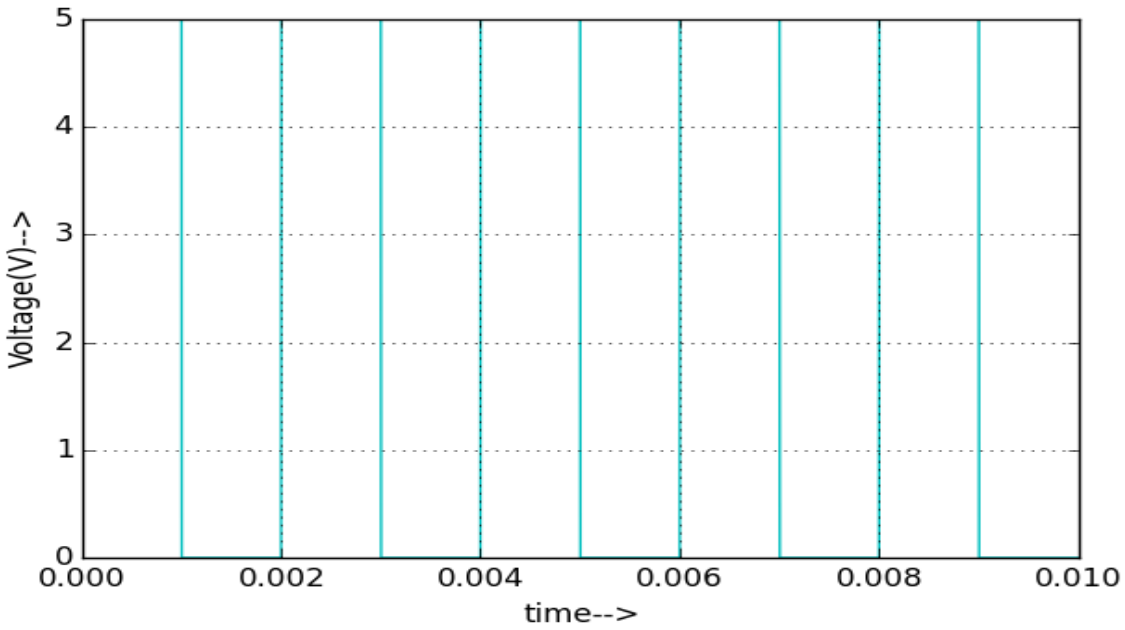

Figure 5: Python Plot of Input Signal V(a)

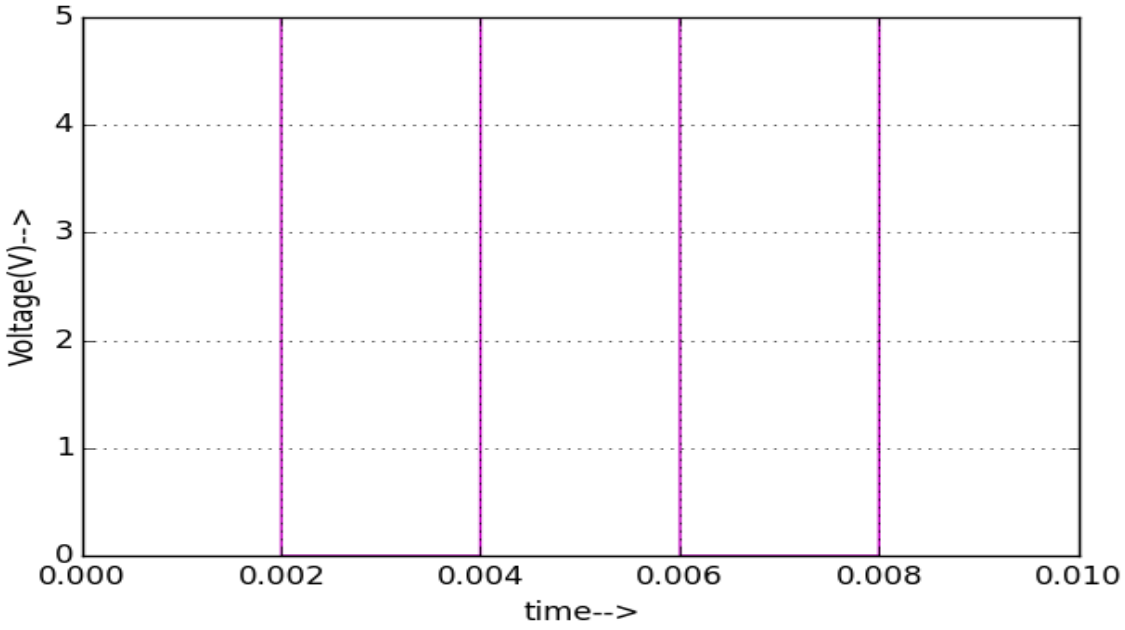

Figure 6: Python Plot of Input Signal V(b)

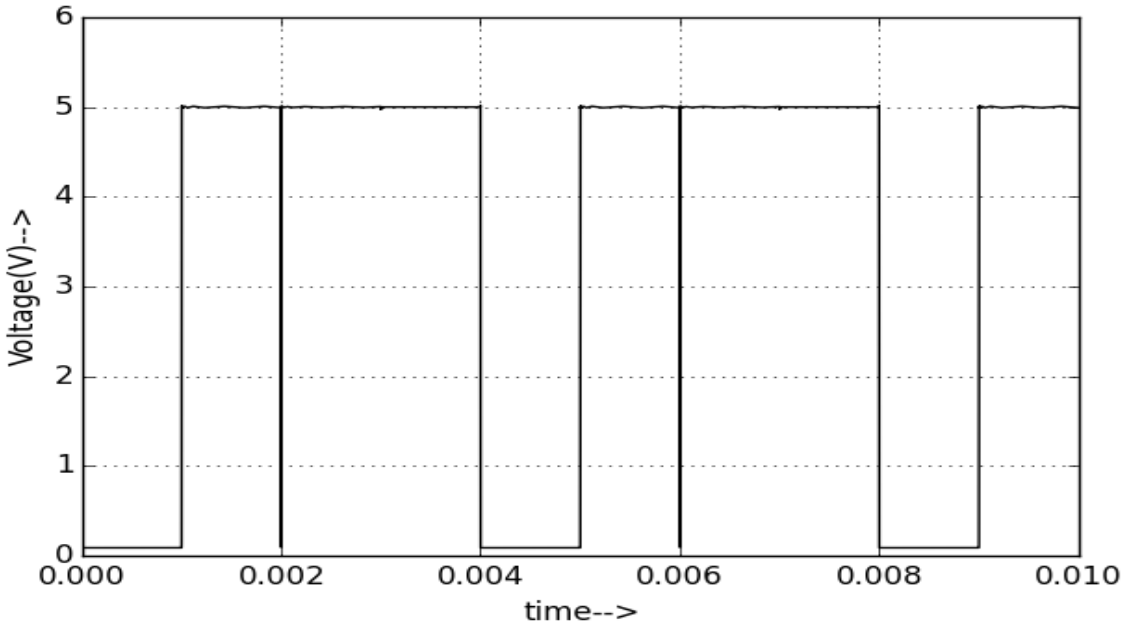

Figure 7: Python Plot of Output Signal V(Out)

4 Conclusion:

Thus, we have studied the transient response of the RTL NAND gate using eSim and we get the appropriate waveforms.

5 References:

https://www.electronics-tutorials.ws/logic/logic_5.html