TITLE OF THE EXPERIMENT

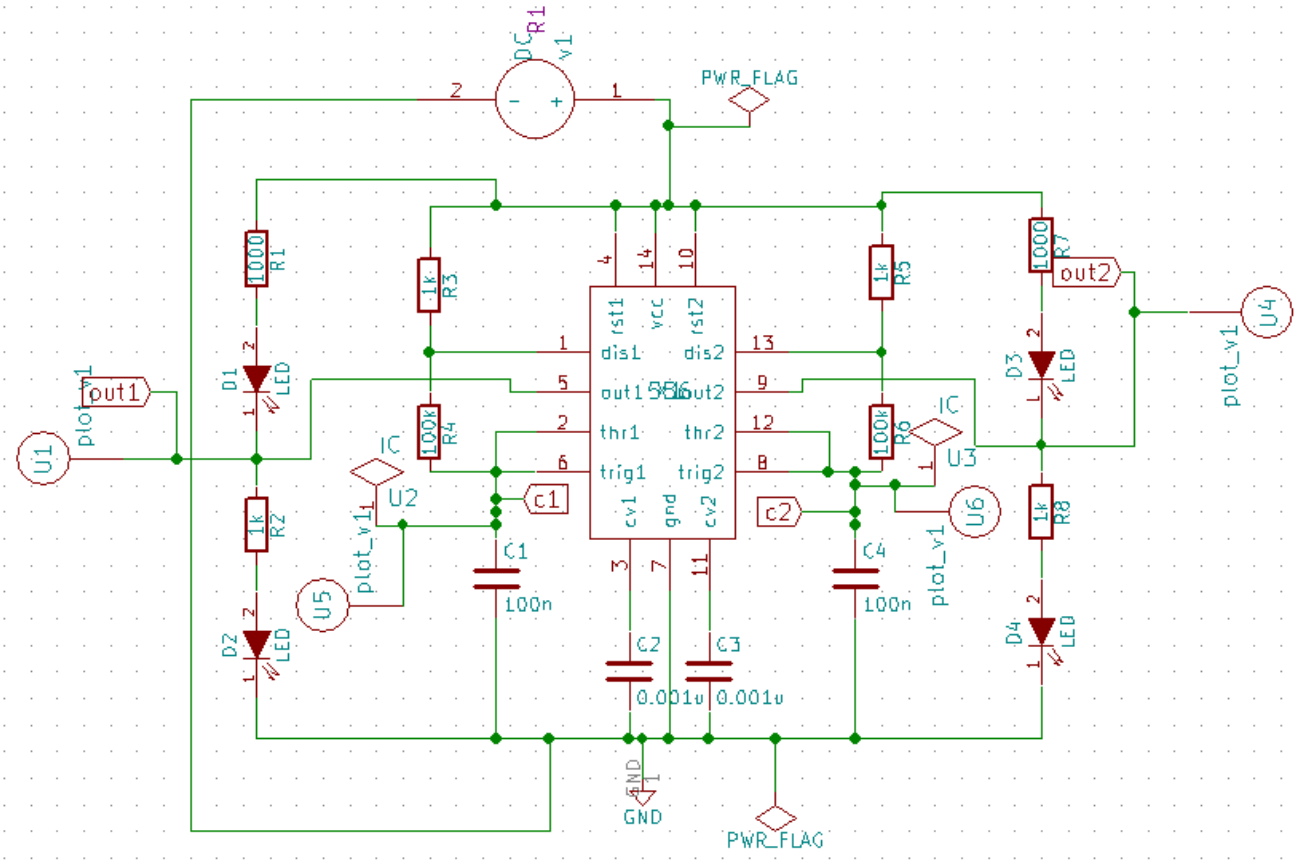
DESIGN OF TWO BIT MULTIPLIER USING SUBCIRCUIT BUILDER

THEORY

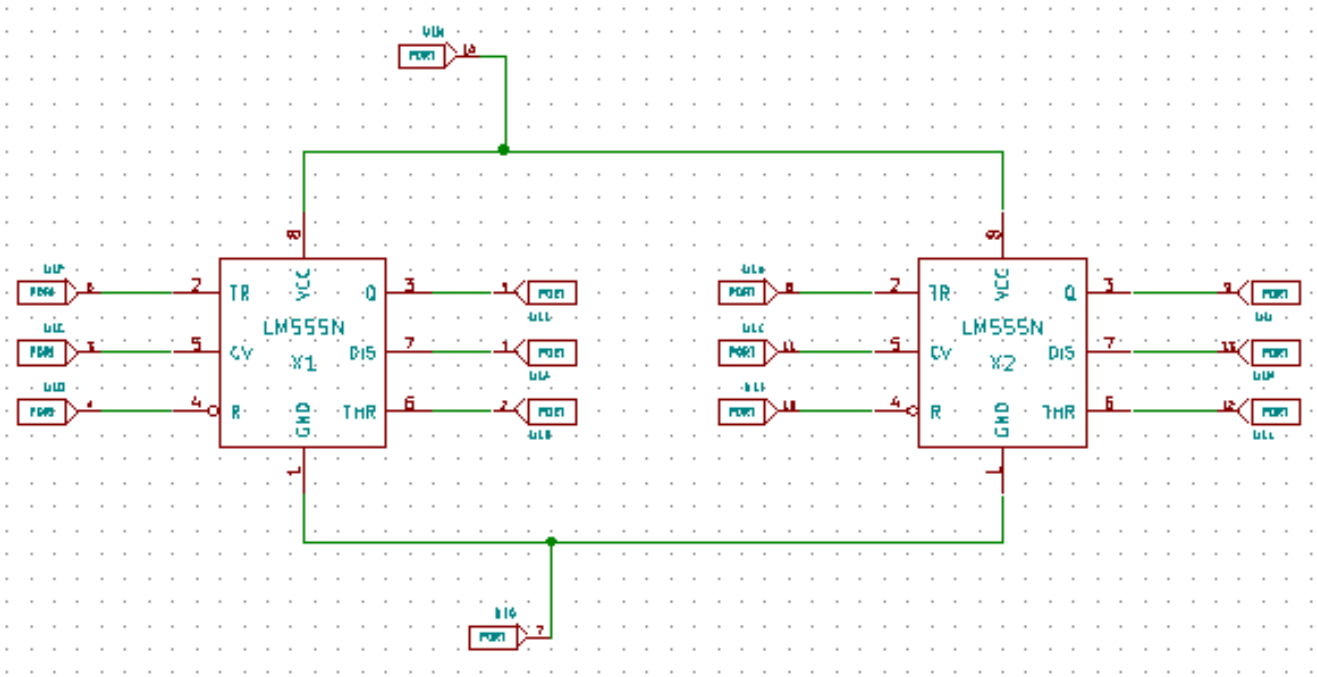
A 2-bit multiplier can be implemented as a straightforward combinational logic circuit using basic logic gates.It consists of 4 inputs and four outputs. The 4 inputs are the two pairs of two bits, call them A and B.

Schematic Diagram

The schematic diagram of dual timer IC circuit is shown below

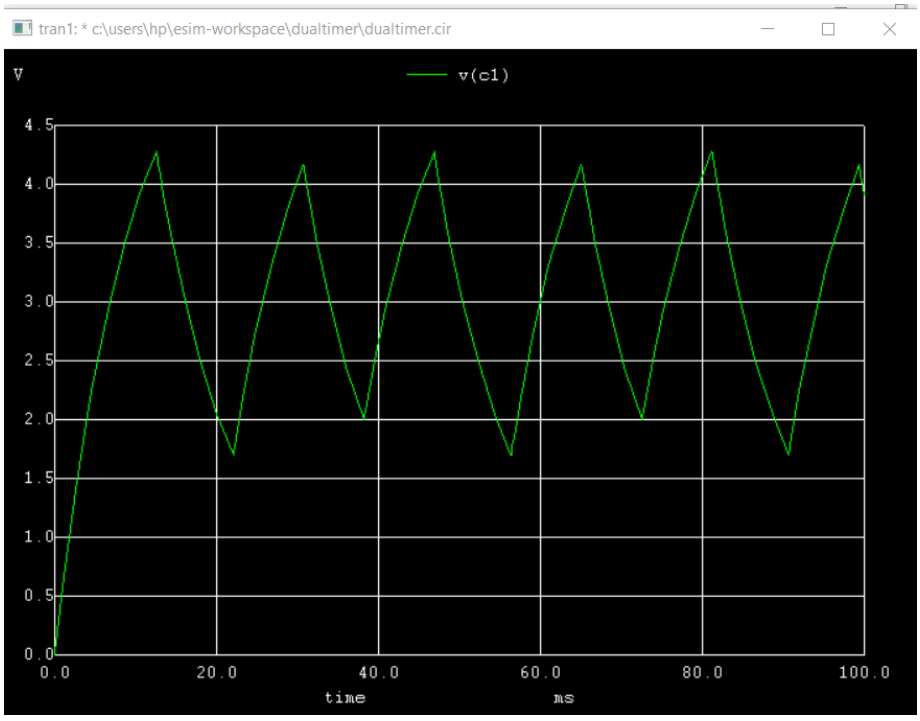


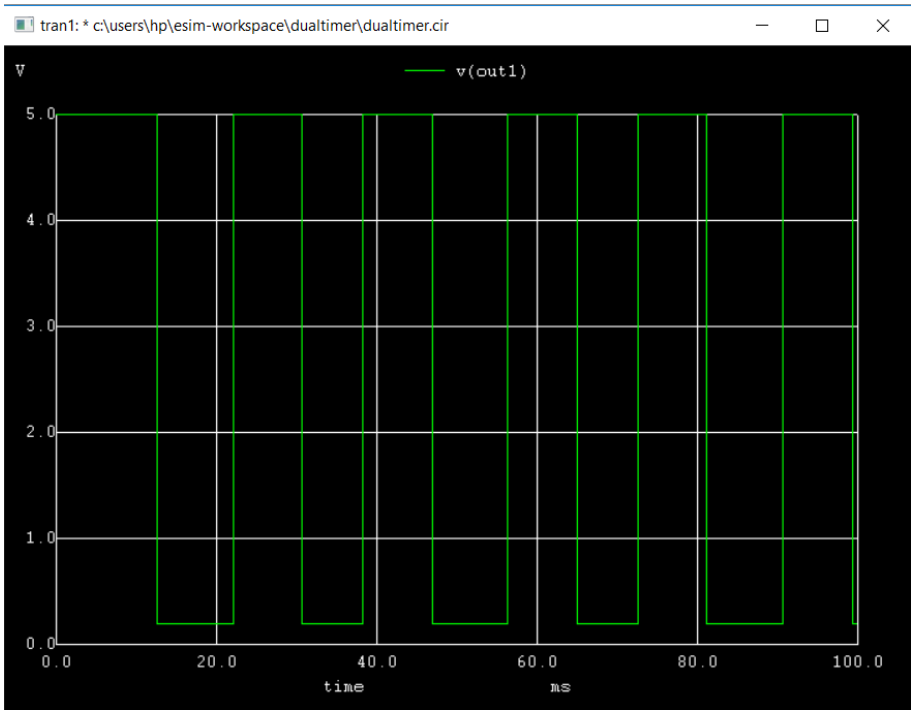
Here I used a subcircuit for IC556.The internal structure of IC556 is drawn using IC555.The diagram of subcircuit is shown below.



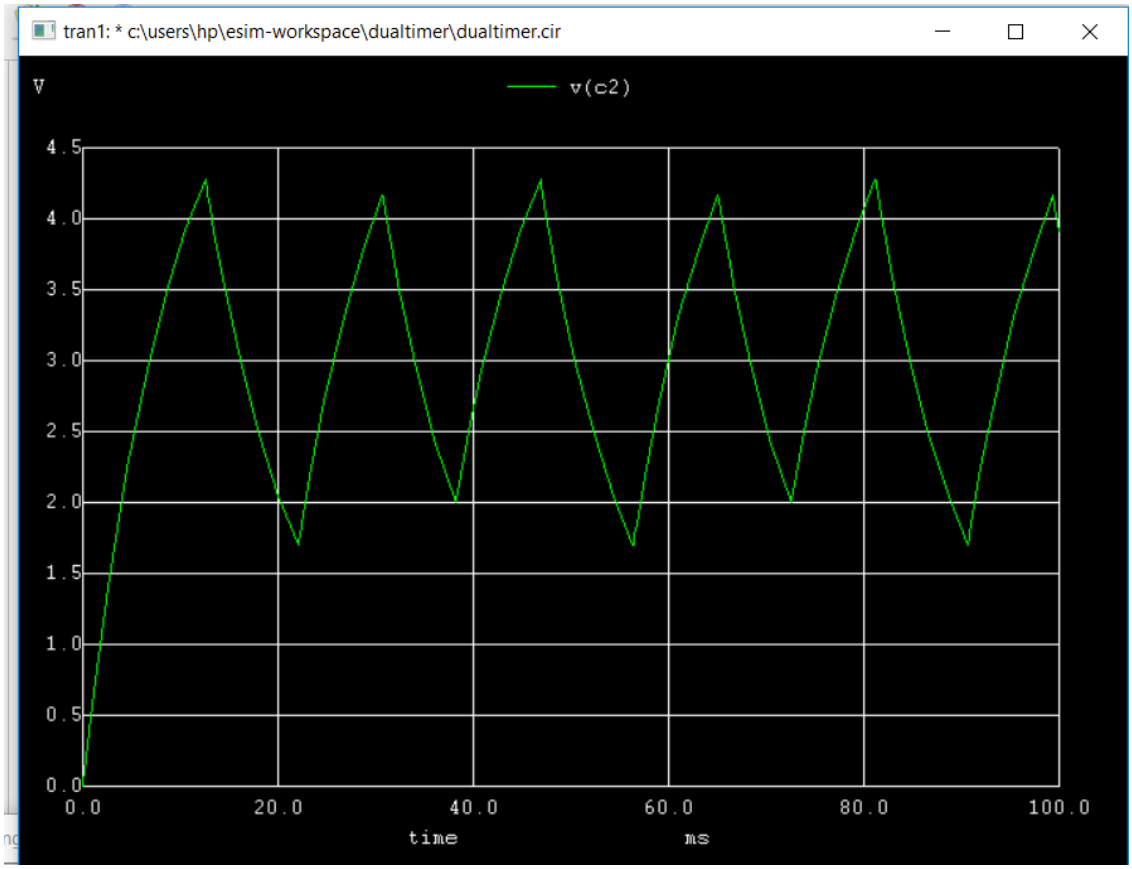
Output Ngspice Plots:

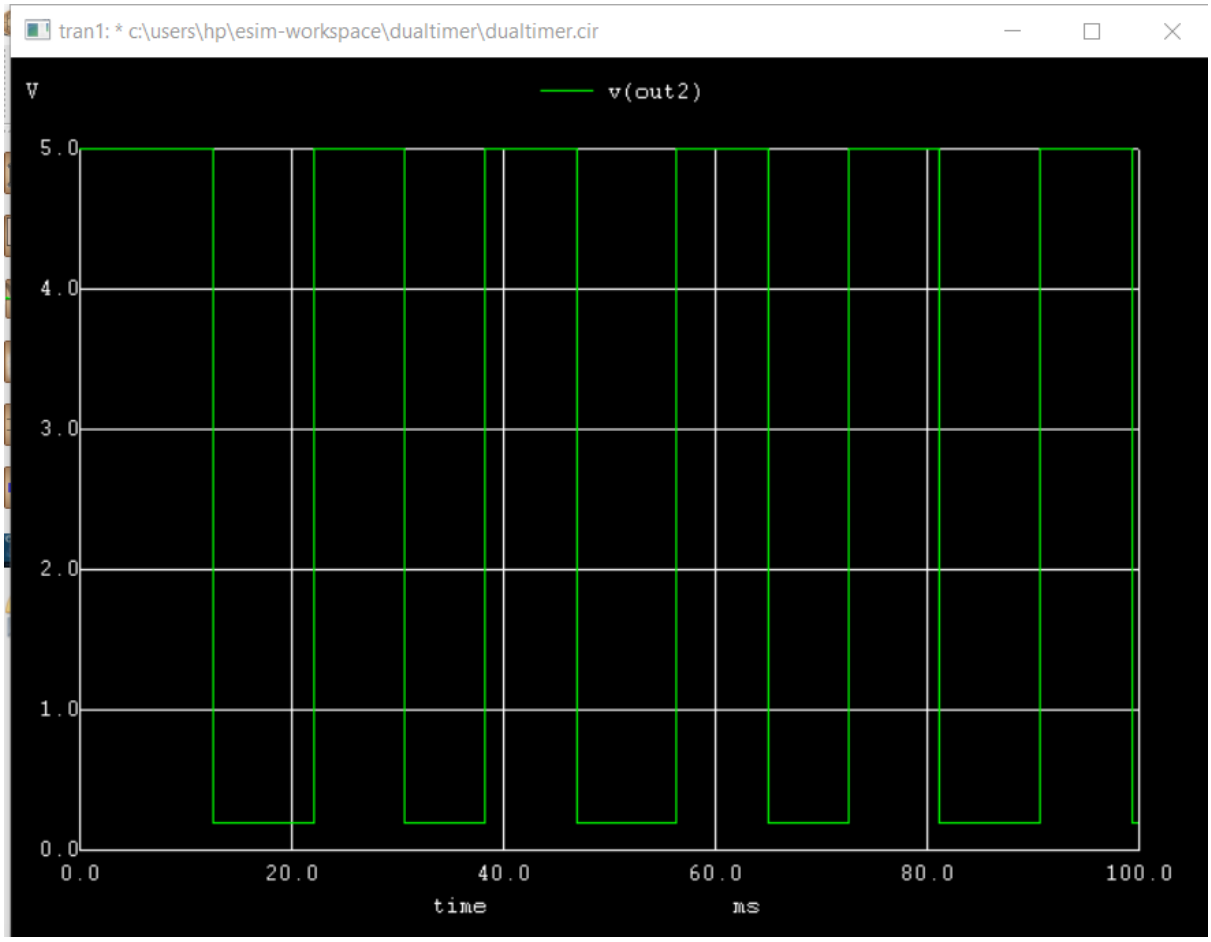
The output plots of First timer is shown below





The output plots of Second timer is shown below.

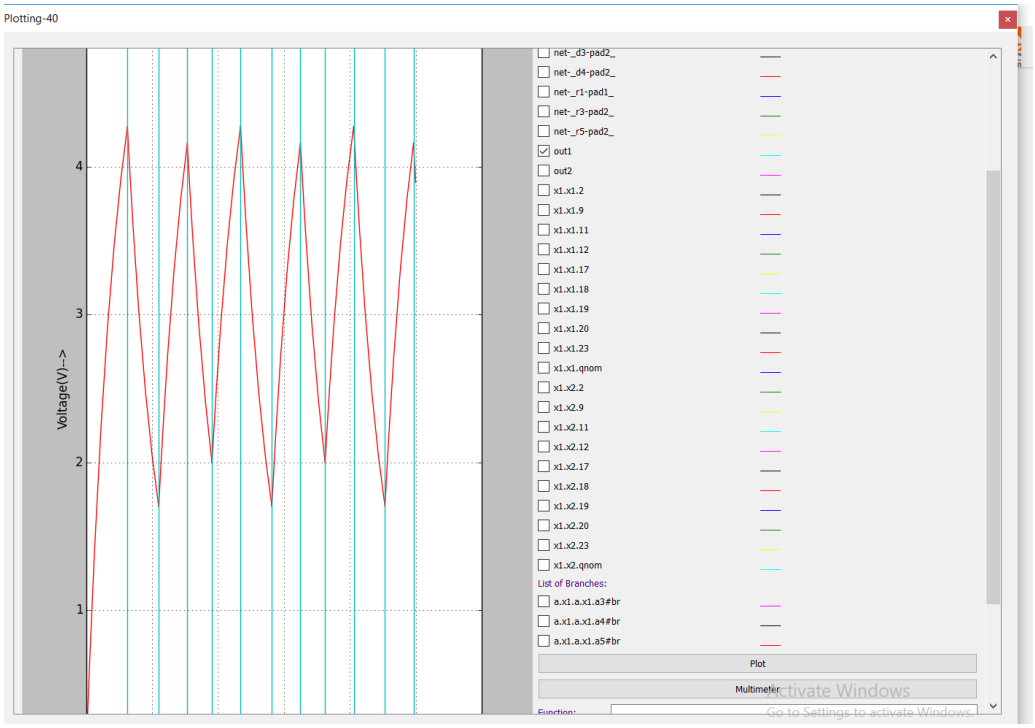




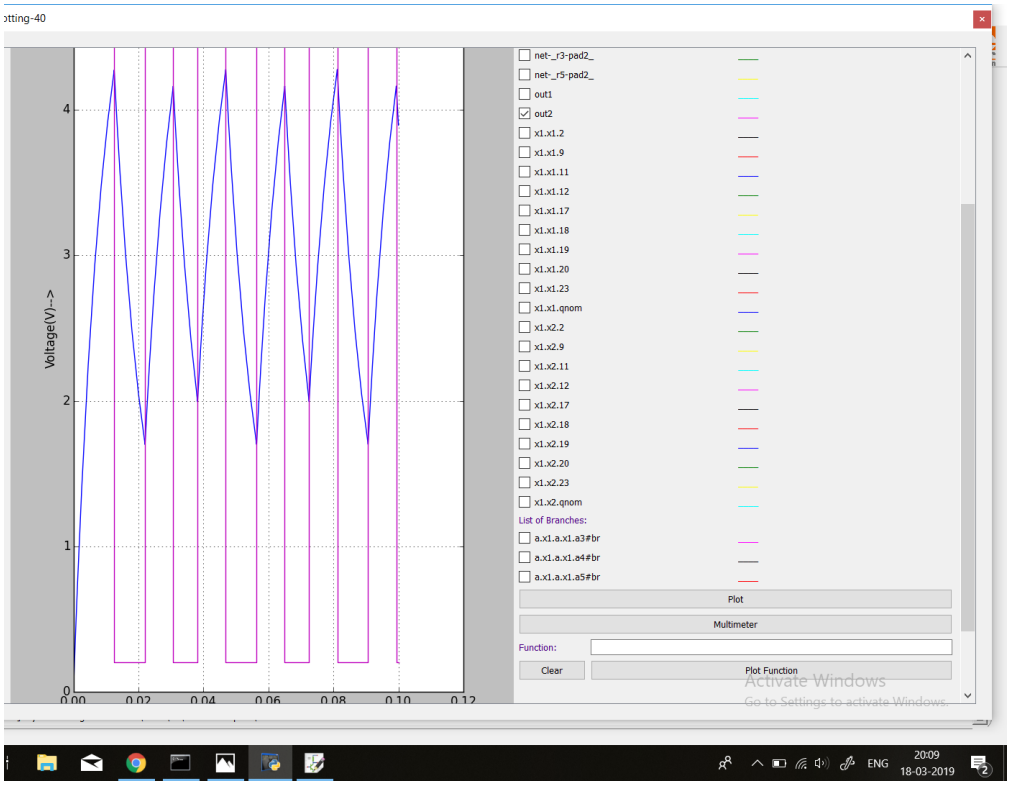
The outputs of two timers are similar.

Python Plot:

The python plot of first timer is



The python plot of second timer is



References: https://www.dummies.com/programming/electronics/components/electronics-components-double-up-with-the-556-dual-timer/